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Direct Integration of Metal Oxide Nanowire in Vertical Field-Effect Transistor

Pho Nguyen,[†] Hou T. Ng,*[,†] Toshishige Yamada, Michael K. Smith, Jun Li, Jie Han, and M. Meyyappan

Center for Nanotechnology, NASA Ames Research Center, Moffett Field, California 94035

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ABSTRACT

We demonstrate seamless direct integration of a semiconductor nanowire grown using a bottom-up approach to obtain a vertical field-effect transistor (VFET). We first synthesize single crystalline semiconductor indium oxide (In_2O_3) nanowires projecting vertically and uniformly on a nonconducting optical sapphire substrate. Direct electrical contact to the nanowires is uniquely provided by a self-assembled underlying In_2O_3 buffer layer formed in-situ during the nanowire growth. A controlled time-resolved growth study reveals dynamic simultaneous nucleation and epitaxial growth events, driven by two competitive growth mechanisms. Based on the nanowire-integrated platform, a depletion mode *n*-channel VFET with an In_2O_3 nanowire constituting the active channel is fabricated. Our unique vertical device architecture could potentially lead to tera-level ultrahigh-density nanoscale electronic, and optoelectronic devices.

Bottom-up nanofabrication approaches involving direct interfacing and integration of low-dimensional nanostructures, in particular vertically aligned one-dimensional (1D) nanowires, could potentially provide an attractive solution to attain ultrahigh-density advanced nanoscale devices and 3D nanocircuitries.[1] To realize and maximize the true potential of these nanostructures for advanced applications in nanoelectronics and optoelectronics, reproducible synthesis of 1D nanowires with controlled directionality and morphology is critical. Equally important, a means of providing ideal and direct electrical interface to the nanowires[2] without disrupting their structural integrity would facilitate subsequent nanoscale device integration and realization of good device performance.

Indium oxide is a direct wide band gap semiconductor ($E_g \sim 3.55-3.75$ eV) transparent oxide.[3] It finds several applications ranging from transparent conductive electrodes to electrochromic mirrors and gas sensors.[4] More recently, research has been conducted on indium oxide nanostructures, predominantly nanowires, for potential applications in high-sensitivity sensor, optoelectronic, field-emission, electronic, and memory devices.[5−7] Various synthesis approaches have been demonstrated, which include vapor transport[8] and laser ablation[9] on a variety of substrates. However, common to other nanowire syntheses, growth directionality control (with respect to the substrate) and direct integration (on the same substrate) into functional devices remain as two significant challenges. To avoid the usual pick-and-place methods of manipulating and aligning horizontally lying nanowires to fabricate prototype testing platforms,[10,11] a proposed solution is to grow single crystalline nanowires epitaxially on a lattice-matched substrate with the major nanowire growth direction orthogonal to the substrate plane and to use this integrated platform for direct device fabrication. Ideally, the substrate also should be electrically conductive; however, potential substrates that meet both requirements are not readily available. After experimenting with a variety of substrates and growth approaches, while taking into consideration the interfacial lattice matching between the unit cells' lattice constants of the substrates and In_2O_3, we found that In_2O_3 nanowires can be grown vertically on a self-assembled thin film of itself on a $(11\bar{2}0)$ optical sapphire (a-Al_2O_3).

Here we report a direct integration approach of incorporating 1D In_2O_3 nanowire on a device platform to fabricate a unique vertical field-effect transistor. Our device fabrication approach has significantly reduced the number of critical processing steps, allowed a lithography-free means of defining the vertical channel length by chemical mechanical polishing, and reduced the footprint of the device since the source, drain, and channel are stacked on top of one another.

We used a combination of carbothermal reduction and gold (Au) catalyst-mediated heteroepitaxial growth approach[2,12] to synthesize the vertically aligned In_2O_3 nanowires. Secondary electron images using a field-emission scanning electron microscope reveal the general structure to consist of a square columnar vertical body and a pyramidal base (Figure 1). An

* Corresponding author. E-mail: hng@mail.arc.nasa.gov.
[†] These authors contributed equally to this work.

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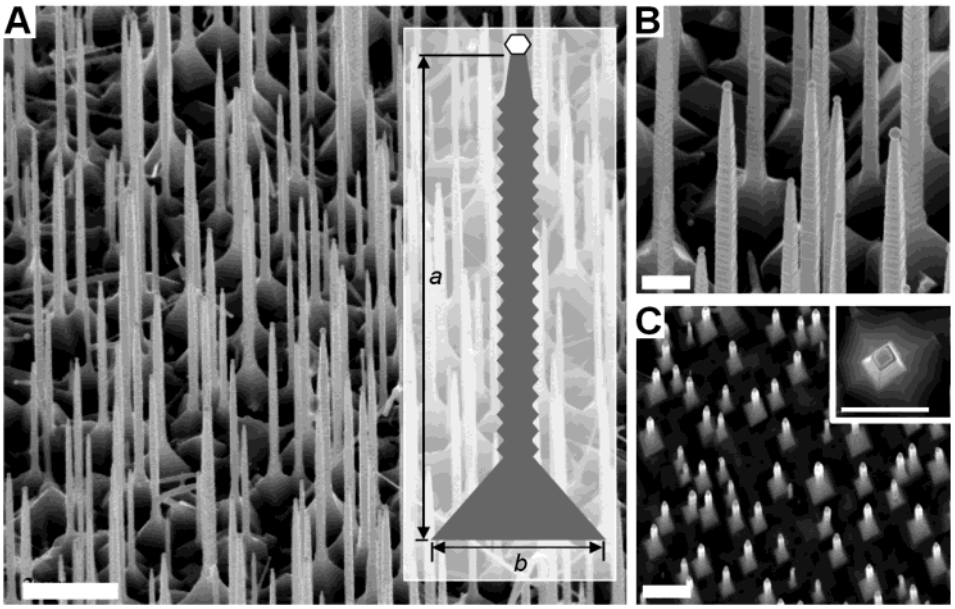

Figure 1. FE-SEM micrographs of vertical In_2O_3 nanowire arrays on single crystalline optical *a*-sapphire substrates. (A) A 45° perspective view of an array of nanowires on *a*-sapphire. The inset shows a schematic (not to scale) of a typical nanowire with an aspect ratio $a/b \sim 4$. (B) A zoom-in 45° perspective view of the nanowires showing orthogonal directionality, nanosized Au catalytic heads, and nanothread cladding along the square core of the nanowires. (C) A 5° perspective view of the array, revealing uniform growth over the surface of the substrate and the rectangular footprint of the pyramidal base. The inset shows a zoom-in top view of a square columnar nanowire with its pyramidal base. Scale bars: 2 μm, 0.25 μm, and 1 μm for A, B, and C respectively; 500 nm for the inset of C.

aspect ratio (a/b) of ~4 is typically found to be characteristic of the nanowires. Each nanowire is observed to taper gradually toward the growth front and terminate with a nanosized Au catalyst. Uniform coverage of the nanowires is typically observed on the entire substrate where the Au catalysts are present. Each as-synthesized nanowire resembles a pillar having "nanothreads" cladding it. These nanothreads reside along the nanowire main growth axis and resemble regularly spaced well-faceted triangular nanowedges. Figure 1C (5° perspective view) and its inset (top view) show the highly regular rectangular footprint of the pyramidal bases which appear to be anchored to a continuous thin film. The typical average diameter of the nanowires is 160 nm with a standard deviation of 45 nm. These dimensions describe the more predominant growth phenomenon, although nanowires with diameter of ~50 nm or less are also possible using the present method or hydrogen post-treatment. The average vertical growth rate is ~3 μm/hr.

Transmission electron microscopy (TEM) analysis provides further insight on the In_2O_3 nanowire structures. Figure 2A reinforces the SEM analysis that the nanowires grew parallel to each other and are orthogonal to the substrate plane. A typical nanowire (Figure 2B) has a uniform core diameter, beginning from the apex of its pyramidal base, but tapers gradually near the growth front, approximately 250−300 nm from a well-faceted Au alloyed nanocatalyst. A selected area electron diffraction (SAED) pattern (inset of Figure 2B), taken perpendicular to the longitudinal growth axis of the nanowire, reveals its high single crystallinity. The regular diffraction spots could be indexed to the [001] zone axis of cubic In_2O_3 with an estimated lattice constant $a \approx 10.1$ Å, in accord with that of bulk In_2O_3 (JCPDS 89-4595). The growth direction of the nanowires is determined to be [100]. The epitaxial single-crystal growth along the main nanowire axis is very well-maintained, as evident from the distinct interface between the nanowire and the Au alloyed nanocatalyst in Figure 2C. A high-resolution (HR) TEM image reveals sharp lattice fringes with an interplanar spacing of 7.04 Å, which corresponds to the {110} plane of In_2O_3, extending to the interfacial boundary. A lattice-resolved HRTEM image in Figure 2D further confirms its high single crystallinity.

It is interesting to note that the nanothreads as observed in the SEM images (Figure 1) are indeed well-defined wedge-like triangular facets residing along the exterior of the nanowire, as shown clearly in Figure 2E. We observed a majority of cross-sections of the nanothreads to assume an isosceles triangle. The typical angle between a side of the triangle (i.e., (111) plane) and its base (i.e., (110) plane) is ~35° (refer to Figure 2E), which is consistent with the calculated angle between the {111} and {110} planes of a cubic system. The average base width, d_b, of the facets is 5 nm while the average height of the triangular facets is 2 nm. This unique geometrical relationship identifies these triangular facets to be bounded by {111} planes.

X-ray photoemission spectroscopy (XPS) analyses reveal the compositions of the nanowires to be $InO_{1.463}$, which is very close to stoichiometric In_2O_3, suggesting minimal oxygen deficiency. There are no significant impurities visible within the detection limit of the instrument and the adventitious carbon contamination is less than 5 atomic percentages. The In ($3d_{5/2}$) peak is deconvoluted into two major components (see Supporting Information). A peak at 444.7 eV (fwhm = 1.42 eV) could be attributed to In_2O_3-like In, while

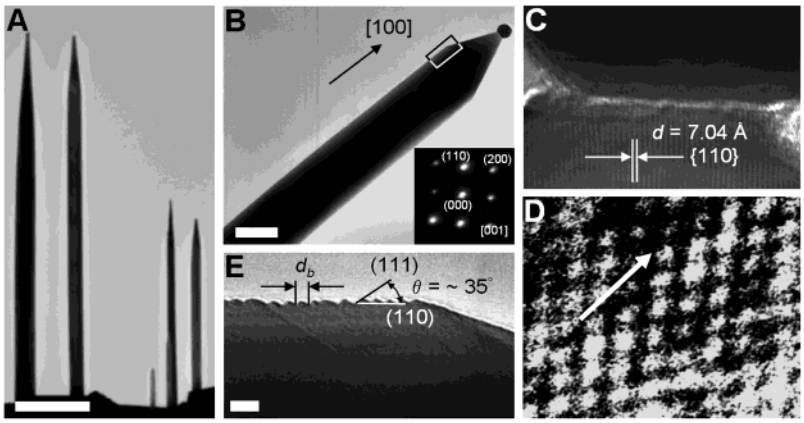

Figure 2. TEM and HRTEM images of In_2O_3 nanowires. (A) A low magnification image showing uniform vertical growth of nanowire arrays on an $(11\bar{2}0)$ optical sapphire. (B) A single nanowire with a uniform core which tapered toward the growth front and terminated with a Au alloyed catalyst. The inset shows a SAED pattern taken perpendicular to the stem of the nanowire. (C) A HRTEM image showing the distinct boundary between the nanowire and the catalyst. (D) A lattice-resolved HRTEM image. A green arrow indicating the nanowire growth direction. (E) A HRTEM image showing nanothreads residing along the exterior of a nanowire. Scale bars: 1 μm, 100 and 10 nm for A, B, and E.

the other at 445.6 eV (fwhm = 1.47 eV) could be attributed to surface hydroxide and/or oxy-hydroxide species.[13] The asymmetric O (1s) peak is deconvoluted into two major components with a peak at 530.3 eV (fwhm = 1.38 eV) attributable to oxygen in the In_2O_3 matrix and the other at 532.1 eV (fwhm = 2.41 eV) to hydroxide, oxy-hydroxide-like oxygen, physisorbed water, or loosely bound oxygen atoms on the surface of the nanowires.[13]

The consistent presence of an In_2O_3 underlayer (as confirmed by similar XPS results) with vertically aligned, catalyst-capped and sidewall nanothread-decorated nanowires atop pyramidal bases indicates a growth mechanism based not entirely on the classical vapor−liquid−solid (VLS) mechanism.[14] The latter is typically characterized by nanowires with a straight sidewall morphology and a uniform diameter. Other mechanisms such as the Volmer−Weber 3D island, Frank−Van der Merwe, and Stranski−Krastanov growth modes[15] also cannot fully explain the observed growth phenomena. A controlled time-sequenced growth study is, therefore, undertaken to shed light into various stages of the nanowire growth process.

Combinatorial thermodynamic analyses[16] of the feedstock sources (i.e., In_2O_3 and graphite) and gas-phase reactions suggest the following hypotheses. At the feedstock sources, In_2O_3 nanoparticles are reduced by graphite and carbon monoxide into indium vapor and metastable In_xO ($x = 1, 2$) vapor. Indeed, Gibbs free energies of the reducing reactions (ΔG_{rxn}) become negative only at a temperature higher than 1200 K. In duplicated control experiments, no growth is observed either using pure In_2O_3 source or at a temperature lower than 1200 K for a total reaction time of an hour. In the gas phase, ΔG_{rxn} of the oxidation reactions of indium and metastable In_xO vapor by carbon dioxide and residual molecular oxygen are highly negative at the operating temperature, suggesting a high probability of gas-phase oxidation in the reaction chamber. Repeated control experiments also confirm a positive dependence of indium oxide deposition rate with a separation distance (ca. 25−75 mm) between the feedstock sources and substrate, and gas phase formation of octahedron nucleates at a lower flow rate (ca. 10 sccm) of the argon carrier gas.

Four distinct growth phases, namely nucleation, 2D thin film formation, nanowire elongation and nanothread formation, as summarized in Figure 3 schematically and supported by SEM images, are identified. During the nucleation phase, indium oxide gaseous molecules (depicted as solid purple circles) dissolve into the gold nanoclusters (solid golden circles) which serve as preferential soft templates, as shown in Figure 3A. Formation of gold nanoclusters via coalescent grain enlargement from an original ultrathin (2 nm) gold film at an elevated temperature has been routinely observed. Upon reaching a critical supersaturation concentration, the solvated indium oxide molecules crystallize with their (100) plane heteroepitaxially onto the $(11\bar{2}0)$ plane of the sapphire substrate (Figure 3B) at the solid−liquid interface as a result of comparatively minimal lattice mismatch (and hence favorable interfacial surface energy).

Initially in the 2D thin film formation phase, due to interfacial surface energy minimization, the alloyed head elongates in the ⟨100⟩ direction horizontally along the *a*-sapphire plane and away from the parent alloy base, as shown schematically in Figure 3B (indicated by horizontal bold black arrows). As shown in Figures 3A′ and B′, simultaneous generation of multiple daughter alloyed heads and solvation/physical vapor deposition of metal oxide vapor into/onto the parent alloyed base and the trail of the daughter alloyed heads are observed with substrates that were subjected to a temperature ramp-up (1 °C/s to 1000 °C) and immediate ramp-down process ($T_{1000^\circ C} = 0$ min). As the base and the trail expand, they are likely to assimilate other gold nuclei or smaller nucleates in their paths. The newly amalgamated nuclei function as new growth fronts, resulting in a 2D heteroepitaxial expansion (Figure 3C′, $T_{1000^\circ C} = 2$ min). Although a film thickness of less than 100 nm is observed to almost completely cover the sapphire substrate within the first five minutes, as shown in Figure 3D′ ($T_{1000^\circ C}$

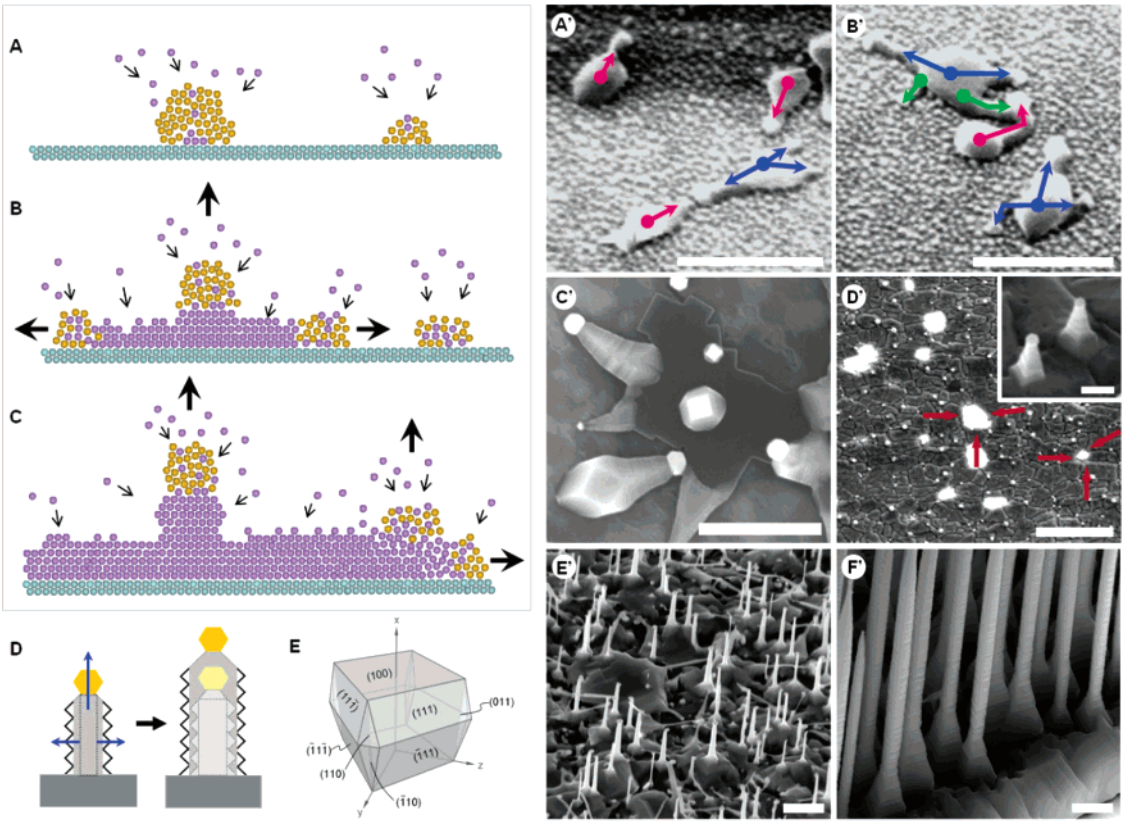

Figure 3. Dynamic nucleation and epitaxial In_2O_3 nanowire and thin film growth. (A−C). Schematics illustrating the competitive growth modes during the growth of the nanowires and underlying thin film. (D) An illustration depicting simultaneous catalyst-directed vertical nanowire growth and sidewall epitaxial deposition. (E) A pictorial 3D view showing the crystallographic relationships between the nanofacets and the growth plane of the nanowire. (A′−F′) A series of SEM images revealing various stages of the controlled time-sequenced growth process. (A′−B′) SEM images revealing generation of daughter alloyed catalytic heads (indicated by different colored arrows) from respective parent alloyed heads at $T_{1000}{}^{\circ}{}_{C} = 0$ min. (C′) A top view SEM image obtained at $T_{1000}{}^{\circ}{}_{C} = 2$ min, showing 2D epitaxial thin film formation and lateral expansion assisted by Au alloyed catalytic heads. (D′) An SEM image showing almost complete coverage of the sapphire substrate with an In_2O_3 thin film at $T_{1000}{}^{\circ}{}_{C} = 5$ min. The red arrows indicate circumferences of two exposed regions (bright spots) of the substrate. The inset shows initial formation of In_2O_3 nanowires with their pyramidal bases. (E′) An SEM image obtained at $T_{1000}{}^{\circ}{}_{C} = 20$ min showing evolution of a regular array of In_2O_3 nanowires with an underlying In_2O_3 thin film. (F′) An SEM image showing the regular pyramidal bases and bodies of the In_2O_3 nanowires at $T_{1000}{}^{\circ}{}_{C} = 60$ min. The underlying thin film has a thickness ~800 nm. All images except C′ are 45° perspective views. Scale bars: 500 nm for A′, B′, C′, and F′; 2 μm and 1 μm for D′ and E′, respectively, and 150 nm for the inset of D′.

= 5 min), the film continues to thicken due to both physical vapor deposition and lateral 2D growth catalyzed by the alloyed heads. Complete coverage is further confirmed by the absence of aluminum and oxygen peaks corresponding to elemental compositions of sapphire from the XPS analyses.

Nanowire elongation occurs on two occasions, as shown schematically in Figures 3B and C. During the nucleation phase, a larger parent alloyed droplet fragments into smaller daughter nuclei as it migrates along the substrate surface. The staying alloyed droplet could serve as a catalytic site for vertical nanowire growth (indicated by upward bold black arrows in Figure 3B). The second occasion occurs during the 2D thin film formation phase at the growth front of the film. The smaller alloyed droplets could coagulate into larger ones to minimize surface energy and reach the radius threshold for vertical nanowire growth. The lowest surface energy of the {110} planes, compared to the {100} and {111} planes of body-centered cubic In_2O_3, promotes nanowire elongation in the [100] direction with its body enclosed by the {110} planes (see Figure 2). It is also noted that as the nanowires reach a certain height (~1 μm), underlayer thickening ceases due most likely to limited mass-transfer of the indium oxide vapor.

A comparison of physical dimensions of the nanowires, in particular their pyramidal bases and bodies at various stages of the growth process, suggests sidewall epitaxial deposition. At $T_{1000}{}^{\circ}{}_{C} = 5$ min, the typical pyramidal base is approximately 150 nm while its body and catalytic head both have an average diameter of 50 nm, as shown in the inset of Figure 3D′. At $T_{1000}{}^{\circ}{}_{C} = 20$ min, the pyramidal base and body have expanded to ~300 and 100 nm, respectively (Figure 3E′). After an hour growth time, the pyramidal base and diameter of the body increase to ~500 and ~160 nm, respectively (Figure 3F′). However, the size of the catalytic head remains relatively constant throughout the growth process.

Formation of the uniform surrounding wedge-like nanothreads along the columnar square core of the nanowire suggests the nanothread formation phase to proceed simultaneously upon occurrence of the nanowire elongation phase

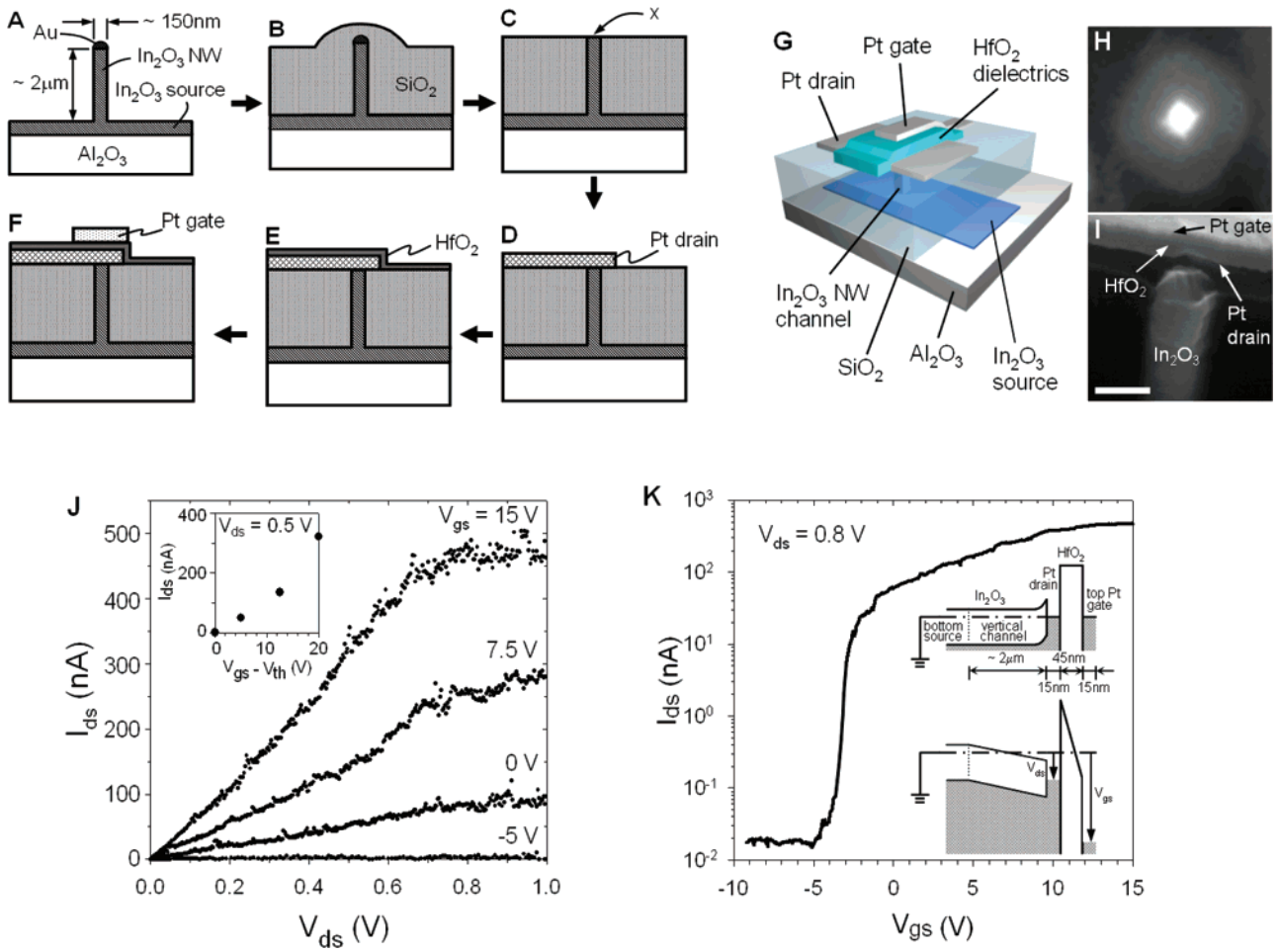

Figure 4. Vertical field-effect transistor (VFET) process flow and $I-V$ characteristics. (A−F) A schematic of a process flow showing the major steps taken to fabricate an $In_2O_3^-$ integrated VFET. Cross-sectional views are shown for the various fabrication stages. (A) A vertical In_2O_3 nanowire-integrated *a*-sapphire (Al_2O_3) substrate. The underlying In_2O_3 buffer layer serves as the bottom source while the vertical In_2O_3 nanowire acts as the active electron channel. (B) Conformal chemical vapor deposition of silicon dioxide (SiO_2) to encapsulate the nanowire completely. (C) Chemical mechanical polishing (CMP) to remove the excess SiO_2 and expose the tip of the nanowire (denoted by *x*). The Au alloyed head is also removed during the CMP process. (D) Formation of a top Pt drain electrode (150 Å thickness). (E) Selective patterning of HfO_2 dielectrics (450 Å thickness), which serves as the gate oxide. (F) Formation of a top Pt gate electrode (150 Å thickness). (G) A 3D schematic illustrating the various components of a completed VFET. (H) An SEM image showing the top view of an exposed square top of an In_2O_3 nanowire after the CMP step. The nanowire is cladded with the SiO_2 matrix. (I) A cross-sectional SEM view of a VFET showing the In_2O_3 nanowire with a top sandwiched structure consisting of a top Pt drain electrode (Pt 1), a HfO_2 thin film, and a top Pt gate electrode (Pt 2). Scale bar: 150 nm. (J) I_{ds} vs V_{ds} characteristics of a VFET with V_{gs} as a parameter. The inset shows a I_{ds} vs $V_{gs} - V_{th}$ plot. (K) Transfer characteristics of a VFET at $V_{ds} = 0.8$ V. The top inset shows a band diagram of the VFET in equilibrium with $V_{gs} = V_{ds} = 0$ V while the bottom inset shows that in operation with $V_{gs} \gg V_{ds} > 0$ V.

(Figure 3C and D). Although the most densely packed planes are the family of {110} planes, the atoms have close-packed direction along the cubic diagonals which are the ⟨111⟩ directions (Figure 3E). The dangling bonds on the family of {110} planes are likely to be minimized by adatom deposition, which could have resulted in sidewall epitaxial deposition in the ⟨110⟩ directions with formation of wedge-like triangular ridges having terminating {111} nanofacets. However, the average height of the nanothreads is self-limiting due likely to overall surface energy minimization. Such a "self-oscillatory" behavior is likely related to the partial vapor pressure (P) of active species which, in our case, is the In_2O_3 vapor. When P_{In2O3} is reduced at least a third by adjusting the initial ratio of the feedstock sources, no self-oscillatory behavior is observed.

The In_2O_3 nanowire-integrated substrate can potentially provide a versatile platform for direct integration to obtain functional nanodevices. Next, we demonstrated the fabrication of an In_2O_3-based vertical field-effect transistor (VFET). A regular array of In_2O_3 nanowires grown from pre-patterned Au catalysts was used. Figures 4A−F show schematically a process flow outlining the major steps leading to a functional VFET. We began with a nanowire-integrated substrate as shown in Figure 4A. The In_2O_3 nanowire functions as the active channel while the underlying continuous In_2O_3 thin film serves as the source electrode of the VFET. The diameter and height of the nanowire were respectively ~150 nm and ~2 μm. Note the Au alloyed head at the tip of the nanowire. Next, we subjected the platform to a silicon dioxide chemical vapor deposition process[16] (Figure 4B)

using tetraethyl orthosilicate as the precursor at an elevated temperature of 700 °C, whereby the In_2O_3 nanowire was conformally surrounded and encapsulated. This was followed by a chemical mechanical polishing step (Figure 4C) to planarize and fully expose the top of the nanowire (denoted *x*) as shown in Figure 4H. This planarization step also served to remove the Au alloyed head. Progressive variations in the size of the CMP slurry particles were used to ensure successful global planarization along with interim resist coating and reflow steps. A constant normal pressure of ~5 psi and wafer rotation speed of 200 rpm were maintained throughout the polishing process. A top platinum (Pt) electrode (150 Å thickness), which constitutes the drain electrode of the VFET, is lithographically patterned (Figure 4D) to provide an electrical contact to the exposed end of the nanowire. As shown in Figure 4E, a dielectric hafnium oxide (450 Å thickness), which forms the gate dielectrics, is introduced prior to laying down a Pt top gate electrode (150 Å thickness). A 3D schematic illustrating the various components of a completed VFET is shown in Figure 4G. A cross-sectional SEM image of the VFET illustrating a side view of the as-fabricated VFET is shown in Figure 4I, which reveals the active electron channel and the sandwiched Pt/HfO_2/Pt structure. The gate and the drain have a similar height, and this will be advantageous for circuit applications since the gate−drain connection is highly common in circuitry designs.

Figure 4J shows a set of typical drain current I_{ds} vs drain voltage V_{ds} profiles obtained with the as-fabricated In_2O_3 nanowire-integrated VFET for different gate bias V_{gs} at room temperature. The electrical conductance increases (decreases) with increasing positive (negative) V_{gs}. This is because our VFET has an unintentionally doped *n*-In_2O_3 channel due to the oxygen deficiency.[18] Our normally on VFET turns off at $V_{gs} = -5$ V, which is our threshold voltage V_{th}. For $V_{gs} \geq 0$ V, I_{ds} increases almost linearly up to an intermediate V_{ds} and reaches saturation at higher V_{ds}. Careful analyses of the I_{ds} vs V_{ds} profiles reveal absence of the typical parabolic pinch-off locus between linear and saturation regions, unlike the case of a standard metal-oxide-semiconductor field-effect transistor (MOSFET).[19,20] The saturated I_{ds} is not proportional to $(V_{gs} - V_{th})^2$, indicating that channel pinch-off[19] is not the saturation mechanism. In fact, our top gate VFET geometry will cause a higher electron density at the drain end of the nanowire channel, and this is against the pinch-off formation.

Relevant band diagrams of the VFET are shown as insets in Figure 4K where the critical components are labeled accordingly. The VFET has two unique features: there is a Schottky barrier at the drain with a built-in potential[21] of 0.7 eV and the top Pt gate is placed above the Pt drain. The band diagram for the VFET has a form in equilibrium with $V_{gs} = V_{ds} = 0$ V (as shown by the top inset) and in an operation condition with $V_{gs} \gg V_{ds} > 0$ V (the bottom inset).

In the present top-gate VFET design, the drain bias accelerates the electrons while the gate bias modulates the electron density and also accelerates the electrons. This is in contrast to a standard FET, where the drain bias exclusively accelerates the electrons and the gate bias exclusively modulates the electron density. Regardless of the unique gate structure in the present VFET, an appreciable electron density modulation due to the gate bias has been demonstrated by the monotone increase of I_{ds} as a function of $V_{gs} - V_{th}$ at $V_{ds} = 0.5$ V (inset of Figure 4J) before the VFET reaches saturation. A deviation from a straight line indicates a slight V_{gs} dependence of the nanowire capacitance. The saturated I_{ds} is roughly proportional to $V_{gs} - V_{th}$, indicating that the electron drift velocity saturation could be responsible for the I_{ds} saturation.[19] The onset electric field for the drift velocity saturation is approximately 1 V/2 μm = 5 kV/ cm.[22]

The transfer characteristic of the VFET is obtained from the I_{ds} vs V_{gs} curve as shown in Figure 4K. The on-to-off saturated current ratio is $I_{ON}/I_{OFF} \approx 2.83 \times 10^4$. Taking the dielectric constant of $\epsilon \approx 30$ (HfO_2), the cross-sectional area of the nanowire $A = 2.25 \times 10^4$ nm^2, and the distance (thickness) of the HfO_2 dielectric $d = 45$ nm in the parallel-plate capacitor model, we obtain the 1D electron density of $n_e = 2.07 \times 10^7$ cm^{-1} at $V_{gs} = 0$ V, neglecting the quantum capacitance.[23] An effective mobility averaged over the carrier concentration is $\mu_{eff} = 6.93$ cm^2/Vs in the VFET channel.[24] A subthreshold gradient $S = (\mathrm{d} \log I_{ds}/\mathrm{d}V_{gs})^{-1}$ is estimated to be ~350 mV per decade. This value is still five times larger than that of the state-of-the-art MOSFETs,[25] but is comparable to that of other nanotransistors such as carbon nanotube FETs.[26] Higher I_{ON}/I_{OFF} and lower *S* of the VFET can be achieved by reducing the gate oxide thickness, improving the channel transport, and the quality of the source/drain electrode contacts.

Our results demonstrate the importance of substrate engineering to grow vertically aligned nanowires and facilitate direct integration of the nanowires into current semiconductor processing technology, bridging the gap between microtechnology and nanotechnology. We have suggested a unique growth mechanism for the nanowire and underlying buffer layer growth process. Understanding the growth mechanism allows fine-tuning of the desirable structures for potential applications in nanoelectronics. The VFET can be fabricated with cell size comparable to the diameter of the nanowire, with the potential of achieving tera-level ultrahigh packing density, radiation harden devices, and all-transparent optoelectronic components.

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Supporting Information Available: XPS spectra reflecting the In ($3d_{5/2}$) and O (1s) core levels of In_2O_3 nanowires. This material is available free of charge via the Internet at http://pubs.acs.org.

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