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Direct loop gain and bandwidth measurement of phase-locked loop

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A simple and robust technique for directly measuring the loop gain and bandwidth of a phase-locked loop (PLL) is proposed. This technique can be used for the real-time measurement of the real loop gain in a closed PLL without breaking its locking state. The agreement of the measured loop gain and theoretical calculations proves the validity of the proposed measurement technique. This technique with a simple configuration can be easily expanded to other phase-locking systems whose loop gain and bandwidth should be measured precisely. [http://dx.doi.org/10.1063/1.4999648]

I. INTRODUCTION

Phase-locked loops (PLLs)[1,2] are widely used in a variety of applications including communication,[3,4] frequency synthesis,[5,6] clock generation,[7] and signal processing.[8,9] One of the main reasons for the widely adopted use of the PLL in most photonics/electronics systems is because it provides a powerful tool in synchronization between two frequency oscillations. Many studies have reported that highly stable and low noise PLLs can be designed by using different kinds of methods, ranging from an all-digital phase-locking technique[7] to an analog integrated phase-locking technique.[8,9] Among these PLL designs, the loop gain and bandwidth of a PLL are two key parameters which determine the PLL's locking performance. With the precise measurement of the loop gain and bandwidth of a PLL, we can characterize the real time jitter or phase noise of a PLL,[10–15] and we can also achieve the best PLL-based electronic and photonic system with low noise by dynamically adjusting the PLL's loop gain and bandwidth.[16–20] Therefore, it is significant that the real PLL's loop gain and bandwidth of the laser-based PLL can be measured precisely in the design of a phase-locking system with high locking performance.[18,19] In principle, the loop gain and bandwidth can be calculated based on the mathematical analysis model of the components in a PLL.[21] However, it is difficult to measure the real PLL's loop gain and bandwidth in an open loop because a PLL system is usually a high-order system,[2,21] and in this case, the error signal in an open loop is very large and cannot be tracked, especially in the low offset frequency.

Over the past years, there have been several studies on the measurement of loop gain and bandwidth of PLLs. A developed automatic bandwidth control (ABWC) embedded into a typical digital PLL scheme was proposed to estimate the gain of the cascade of digitally controlled oscillator (DCO) divider and time/digital converter.[22] With this ABWC, the loop gain of the PLL becomes independent of any analog variable and dependent only on the transfer function of the digital loop filter, which is perfectly predictable and repeatable. An all-digital PLL with a bang–bang phase-frequency detector (BBPFD) was proposed to track the optimum loop gain for minimum jitter.[23] In this PLL setup, an adaptive loop gain controller (ALGC) was designed to calibrate and adjust the loop gain by estimating the autocorrelation of the BBPFD output. For directly measuring the bandwidth of a PLL, a scheme by measuring the jitter transfer function of the system components was proposed.[24] In this scheme, the jitter transfer function of the device under test as a function of jitter frequency was used to estimate the bandwidth of the PLL. Beside these estimation and calibration methods of loop gain and bandwidth, another direct loop gain and bandwidth measurement technique by inserting an external modulation signal was developed.[25] With this technique, the loop gain can be measured precisely above the locking bandwidth.

Although these techniques proposed in the beforementioned studies can be used to estimate the loop gain and bandwidth of a PLL, they do not provide a tool to measure the real loop gain of the PLL precisely in the whole offset frequency due to the indirect estimation methods[22,23] or the bandwidth-limited schemes with the inserted modulation signal.[24,25] To overcome this problem, in this paper, a simple and robust technique for real-time measurement of the loop gain and bandwidth of a PLL over the whole offset frequency is proposed. This technique can be used to precisely measure the loop gain of a PLL in the whole offset frequency without breaking its locking state. The performance of the proposed technique is verified by theoretical simulations first, and then, it is assessed on a real PLL experimental system. In Sec. II, the scheme of the technique is presented. Section III is the theoretical analysis and simulation of the proposed scheme. Section IV gives the experimental results with the proposed technique, and the conclusion is given in Sec. V.

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II. SCHEME OF LOOP GAIN AND BANDWIDTH MEASUREMENT

A PLL is a loop system that causes a frequency source to track with another one. More precisely, a PLL is a circuit synchronizing an output signal generated by an oscillator with a reference or an input signal in frequency as well as in phase.[2,21] In Subsections II A and II B, we are first going to briefly review a typical analog PLL and its characteristics and then present the scheme of PLL's loop gain and bandwidth measurement with the added components in a closed loop.

A. Modeling analysis of a typical PLL and its loop gain

Figure 1 shows the simplified configuration of a typical analog PLL. Three basic functional blocks in the configuration such as a phase detector, a loop filter, and a voltage-controlled oscillator (VCO) form a PLL.[2,21] In a closed PLL, the oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the reference signal, adjusting the oscillator to keep the phases matched. Tracking the VCO's output signal to the reference signal for comparison in phase and frequency is called phase-locking. Here, a block diagram for the typical PLL is shown in Fig. 2. Next, we will briefly describe these blocks and explain how a PLL works.

A phase detector is a device capable of delivering an output signal that is proportional to the phase difference between its two input signals. In an analog PLL circuit, the mixer is mainly used as the phase detector. When the PLL is locked, the frequencies of the reference signal and VCO's output signal are identical. When the phase error signal generated from the phase detector is small, the sine function of the mixer can be replaced by its argument. In the complex frequency domain, the error signal can be expressed as

$$U_e(s) = k_d \Theta_e(s) = k_d(\Theta_i(s) - \Theta_o(s)), \tag{1}$$

where K_d is the detector gain. $U_e(s)$ is the phase error signal generated from the detector. $\Theta_e(s)$ is the phase argument of the error signal. $\Theta_i(s)$ and $\Theta_o(s)$ are the phase arguments of the input reference source and VCO's output signal, respectively. This equation represents the linearized model of the phase detector.

A loop filter, as a pure two-port electronic component, is crucial to the operation of the whole PLL. As shown in Fig. 1, the error signal $u_e(t)$ from the phase detector consists of a number of terms. In the locked state of the PLL, the first term is a DC component and roughly proportional to the phase error $\theta_i(t) - \theta_o(t)$. The remaining terms are AC components that

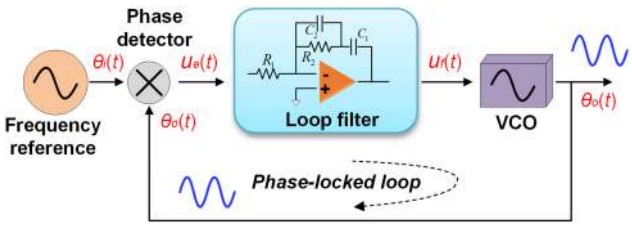

FIG. 1. Simplified configuration for a phase-locked loop. VCO: voltage-controlled oscillator.

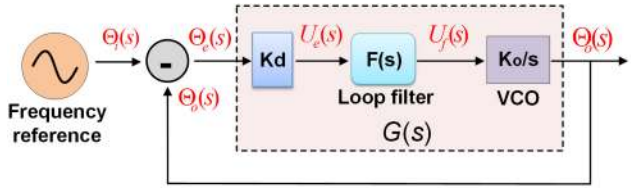

FIG. 2. Block diagram for a typical PLL.

have the harmonic frequencies. Since these higher harmonic frequencies are unwanted signals, they are filtered out by a loop filter. Usually, the loop filter is a simple passive low-pass filter or a sophisticated active filter with an integration (shown in Fig. 1) which can improve the stability of the PLL. Assuming the transfer function of the loop filter is $F(s)$, the filtered error signal is given by

$$U_f(s) = F(s)U_e(s), \tag{2}$$

where $U_f(s)$ is the error signal after the loop filter, and we would apply it to tune the VCO.

A VCO is a common single oscillator whose frequency can be controlled by a voltage input. In the time domain, the radian frequency ω_t of a VCO output signal is directly proportional to the control signal and is given by

$$\frac{d\theta_o(t)}{dt} = \varpi_t(t) = \varpi_0 + k_o u_f(t), \tag{3}$$

where k_o is the VCO gain and ω_0 is the center frequency of the VCO. This equation shows the linearity of a VCO. Converting Eq. (3) to the expression in the complex frequency domain, we have

$$\Theta_o(s) = \frac{k_o}{s} U_f(s). \tag{4}$$

If we assume that the VCO has been phase-locked, a linear mathematical PLL model can be developed. We define the transfer function $G(s)$ as the loop gain (shown in Fig. 2). Based on Eqs. (1), (2), and (4), $G(s)$ is given by[2]

$$G(s) = \frac{\Theta_o(s)}{\Theta_e(s)} = \frac{k_d k_o F(s)}{s}. \tag{5}$$

A PLL is a closed-loop system. Based on the control theory, we can define the closed-loop phase-transfer function $H(s)$. Generally, dynamic analysis of a control system can be normally performed by means of its closed-loop transfer function $H(s)$. $H(s)$ relates the input reference source and the VCO's output, which is[2]

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{G(s)}{1 + G(s)} = \frac{k_d k_o F(s)}{s + k_d k_o F(s)}. \tag{6}$$

Equations (5) and (6) describe the mathematical model of a typical PLL, and we can apply this model to design various kinds of PLLs in our phase-locked system.

B. Upgraded PLLs for direct loop gain and bandwidth measurement

The loop gain and bandwidth are two important parameters to determine the PLL's locking ability. In principle,

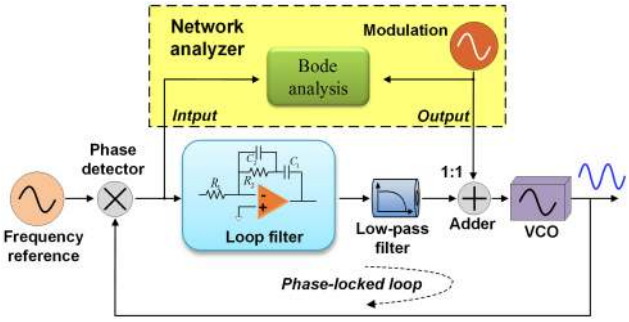

FIG. 3. Configuration of the technique for measuring the transfer function of the VCO and phase detector.

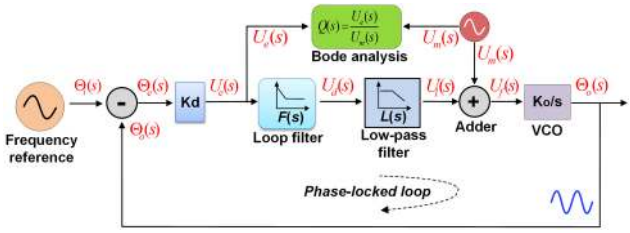

FIG. 4. Functional block of the upgraded PLL for measuring $T(s)$.

$G(s)$ can be calculated theoretically. However, it is difficult to directly measure the real loop gain in an open PLL because the open loop is a first order or second order system, which is described in Eq. (5) with consideration of $F(s)$. In this case, therefore, the loop gain is very large in the low offset frequency, which increases the difficulty to detect any error signal in the open loop. In order to directly measure a real loop gain, there is only a chance if we can detect the error signal in a closed loop. Here, based on Eq. (4), we rewrite the loop gain $G(s) = T(s) \cdot F(s)$, where $T(s) = K_d K_o/s$, which is called the transfer function of the VCO and phase detector. Our scheme for measuring the loop gain in this paper is to first measure $T(s)$ and $F(s)$ individually and then achieve the final $G(s)$ by multiplying them. $F(s)$, which is the transfer function of loop filter, can be measured directly. For measuring $T(s)$, a simple technique is proposed here.

This technique for measuring $T(s)$ is shown in Fig. 3. Two new components, a low-pass filter and a 1:1 electronic adder, are inserted into the original typical PLL. The low-pass filter after the loop filter is used to decrease the locking bandwidth, and the adder is used to introduce a modulation signal into the loop for comparing the input modulation and the error signal after the phase detector. When the PLL is in the locking state, the output modulation signal from a network analyzer will be delivered to the adder, and the error signal after the phase detector will be monitored by the network analyzer. With a Bode analysis between the modulation and error signals, a real loop gain (as a Bode plot) of modulation signal after passing through the VCO and phase detector can be achieved. Based on this measured Bode plot of in-loop gain, $T(s)$ can be fitted out precisely. Here, the use of the low-pass filter is inspired from Ref. 25. We add a low-pass filter in the loop to limit the locking bandwidth of the PLL. In this case, there is enough space for out of bandwidth where the inserted modulation signal would not be suppressed by the loop gain. Consequently, the lower the locking bandwidth is, the easier $T(s)$ is fitted. In Sec. III, the mechanism of the $T(s)$ measurement will be theoretically analyzed, and the details of fitting $T(s)$ will be demonstrated.

III. THEORETICAL ANALYSIS AND SIMULATION OF THE LOOP GAIN MEASUREMENT TECHNIQUE

As described in Sec. II B, the proposed technique can be used to directly measure $T(s)$. Here, we simplify the configuration of this technique to a functional block (shown in Fig. 4). Assuming the added low-pass filter has a transfer function $L(s)$, the adder has a 1×1 input gain ratio, and the network analyzer outputs a modulation signal $U_m(s)$, then we have,

$$U_f(s) = U_m(s) + U_l(s), \quad U_l(s) = U_e(s)F(s)L(s), \tag{7}$$

where $U_f(s)$ is the voltage signal to drive the VCO, $U_m(s)$ is the voltage signal from the modulation source in the network analyzer, and $U_l(s)$ is the voltage signal from the added low-pass filter. Here, in order to calculate the transfer function of the VCO and phase detector, the gain of the modulation signal passing though the VCO and phase detector in a closed loop should be obtained, which is defined as $Q(s) = U_e(s)/U_m(s)$.

When the upgraded PLL is closed, the modulation signal will be treated as a noise signal because a PLL will stabilize the input voltage of the loop filter to a constant, for synchronizing the VCO's phase to that of frequency reference. In our analysis, without loss of generality, we assume the fixed phase of frequency reference is zero, which is also convenient for us to calculate the gain of the modulation signal in the closed PLL. With this assumption, we have

$$U_e(s) = k_d(\Theta_i(s) - \Theta_o(s)) = -k_d\Theta_o(s). \tag{8}$$

Based on Eqs. (4), (7), and (8), the gain of the modulation signal passing through the VCO and phase detector [defined as $Q(s)$] can be calculated as

$$Q(s) = \frac{U_e(s)}{U_m(s)} = -\frac{k_d k_o}{s + k_d k_o F(s)L(s)}, \tag{9}$$

where $F(s)$ and $L(s)$ is the transfer function of the loop filter and the inserted low-pass filter, respectively, as described before. The loop filter can be either an active filter or a passive filter, and there is no difference on the analysis of the transfer function between using an active filter and a passive filter, because the loop filter does not affect the gain of modulation passing though the VCO and phase detector. Therefore, without loss of generality, a common active loop filter is adopted here, whose transfer functions can be expressed as $F(s) = k_p(1/T_i s + 1)$,[26] where k_p is the gain of the loop filter and T_i is the integration time of the loop filter. Here, a common first-order passive low-pass filter is used as the inserted low-pass filter, and its transfer function is given by $L(s) = 1/(\tau s + 1)$,[27] where τ is the time delay of the low-pass filter. Their circuits are shown in Fig. 5.

We put the two expressions $F(s)$ and $L(s)$ into Eq. (9), and then the final expression of $Q(s)$ is given by

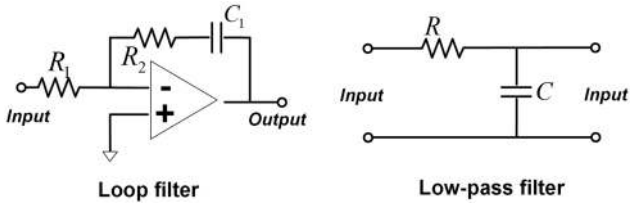

FIG. 5. Common active first-order loop filter and low-pass filter.

$$Q(s) = \frac{k_d k_o T_i \tau s^2 + k_d k_o T_i s}{T_i \tau s^3 + T_i s^2 + k_d k_o k_p T_i s + k_d k_o k_p}. \quad (10)$$

Based on the theoretical $Q(s)$ demonstrated in Eq. (10), a simulation for $Q(s)$ is performed with an actual PLL, whose parameters are as follows: the center frequency of VCO is 1 GHz, k_o is 10^3 Hz/V, k_d is 0.5 V/rad, k_P is 10, T_i is 1×10^{-3} s, and τ is 5×10^{-3} s. The simulation result is shown as Curve (i) in Fig. 6. We found that the simulated Bode plot Curve (i) has a corner due to the bandwidth of the closed loop. This corner separates the Bode plot into two sections: in the bandwidth and out of the bandwidth. Bode plot which is in the bandwidth indicates how much the modulation signal is suppressed by the loop gain of the PLL. This is because the PLL treats the modulation signal as a noise in the locking bandwidth. By contrast, the Bode plot which is out of the bandwidth presents the gain of the modulation signal when it passes through the VCO and phase detector without the suppression of the gain of the PLL. In this case, therefore, the gain of modulation signal is equal to the gain provided by the VCO and phase detector, which means $Q(s)$ in this section (out of bandwidth) is the same as $T(s)$. Furthermore, this analysis can also be explained mathematically by the simplification of $Q(s)$ in Eq. (9), when the offset frequency is too large to omit the term $F(s)L(s)$. In this case (out of bandwidth), $Q(s)$ is degenerated to $T(s)$ due to the approximate zero term $F(s)L(s)$. Therefore, with the analysis above, $T(s)$ can be fitted via the Bode plot of $Q(s)$ out of bandwidth. Note that a servo hike appears around the corner in our simulation. This is because that the gain of the modulation signal is about 1 and the phase lag is close to −180°, which increases the gain of the positive feedback in the loop of the modulation signal.

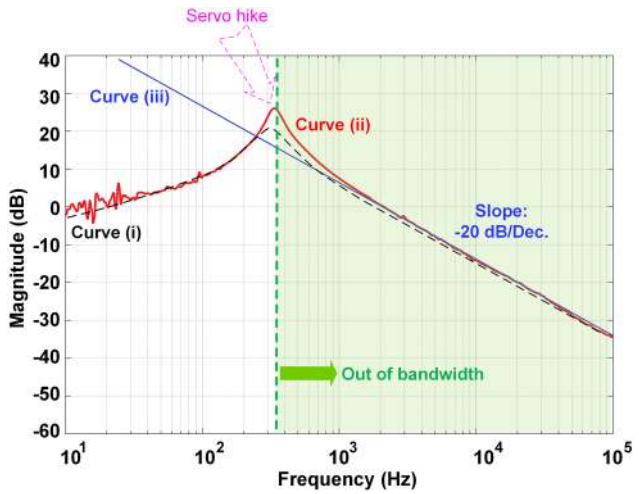

FIG. 6. Simulation and measurement results of the transfer function of the VCO and phase detector. Curve (i): theoretical gain of the modulation signal passed through the VCO and phase detector. Curve (ii): measured gain of the modulation signal passed through the VCO and phase detector. Curve (iii): T(s) by fitting slope.

The analysis above is for an analog PLL with an analog phase detector. However, there have been various kinds of PLLs, ranging from analog PLLs to digital PLLs. For a typical digital PLL which consists of a digital phase-frequency detector and a DCO, its loop gain and bandwidth can also be measured precisely by our proposed technique, because the digital PLL has a similar transfer function,[28] and the analysis discussed in this section can also be applied to the transfer function of the digital PLL. The only difference between the analog and digital PLLs with the proposed technique for loop gain measurement is that the transfer functions of the inserted components should be analyzed in the digital complex frequency domain. Therefore, without loss of generality, a typical analog PLL is just discussed in this paper. In Sec. IV, we will build an actual analog PLL with the same parameters adopted in the simulation, to experimentally verify our technique for measuring the loop gain.

IV. EXPERIMENT RESULT AND DISCUSSION

A real loop gain of an actual PLL was measured with the proposed technique. Here, a VCO with a center frequency of 1 GHz was locked to a highly stable microwave generator (Agilent, E4421B), and the Proportional-Integral (PI) controller (as a loop filter, shown in Fig. 5) has one integration. In our case, the actual PLL has the following parameters: k_o is 10^3 Hz/V, k_d is 0.5 V/rad, k_P is 10, T_i is 1×10^{-3} s, and τ is 5×10^{-3} s. All the parameters are almost the same as our simulation descripted in Sec. III. When the loop was closed, we measured $T(s)$ with our scheme, and the Bode plot measurement results are shown in Fig. 6.

Curve (i) in Fig. 6 is the theoretical gain of the modulation signal passing through the VCO and phase detector, which is described as $Q(s)$ in Eq. (10). This curve has a corner, which indicates the locking bandwidth of the PLL after inserting the low-pass filter (shown in Fig. 3). In bandwidth, the modulation signal will be treated as a noise signal and suppressed by the loop. The less frequency is, the stronger the suppression is. This is because the loop has a larger gain in the low offset frequency. For out of bandwidth, the loop will not act on the modulation signal because the loop gain is not enough to affect the modulation signal in the loop. Therefore, Curve (i) should coincide with $T(s)$ out of locking bandwidth. Curve (ii) is the measured gain of the modulation signal $Q(s)$ passing through the VCO and phase detector. Figure 6 shows that both Curve (i) and Curve (ii) are nearly the same and have similar servo hikes appeared around the corner frequency in the two curves. This is because the gain of the modulation signal is larger than 1 and the phase lag is close to −180°, which increases the gain of the positive feedback in our measuring system slightly. With fitting Curve (ii) out of locking bandwidth, we got a real $T(s)$ which is shown in Fig. 6 as Curve (iii). The slope of Curve (iii) is −20 dB/decade. This is also in agreement with the theoretical expression of $T(s) = K_d K_o/\text{s}$.

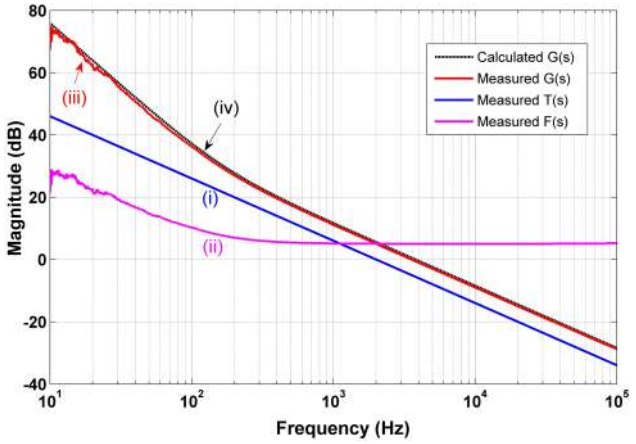

FIG. 7. Simulation and measurement results of final gain of the PLL. Curve (i): measured gain of the modulation signal passed through the PLL and phase detector. Curve (ii): measured transfer function of the loop filter F(s). Curve (iii): measured loop gain of the PLL. Curve (iv): calculated loop gain of the PLL.

After achieving $T(s)$ by fitting the measured $Q(s)$, we measured the transfer function of the loop filter $F(s)$ directly. Here, the gain of the loop filter is set to 5 and the integration cutoff frequency of the loop filter is ~200 Hz. By multiplying $T(s)$ and $F(s)$, we got the final loop gain of the actual PLL. Figure 7 shows the measured final loop gain $G(s)$ and bandwidth of the PLL. Curve (i) is the measured $T(s)$ which is also shown in Fig. 6. The slope is nearly −20 dB/decade at full frequency. Curve (ii) is the measured transfer function of the loop filter $F(s)$. Curve (iii) is the loop gain $G(s)$ by multiplying $T(s)$ and $F(s)$, and this curve indicates the bandwidth of the PLL is about 3 kHz because the loop gain is less than 1 above 3 kHz. For verifying the loop gain measured by our technique, a calculated loop gain is also demonstrated in Fig. 7 as Curve (iv). It can be seen from Fig. 7 that the measured loop gain shown as Curve (iii) is in agreement with the calculated plot shown as Curve (iv). Therefore, the agreement of the two curves proves that our technique for measuring the loop gain is correct and reasonable.

V. CONCLUSION

A simple and robust technique for measuring the loop gain and bandwidth of a PLL is proposed in this paper. This technique provides a powerful tool in precisely measuring the loop gain and bandwidth of a PLL in a whole offset frequency (ranging from DC to the highest frequency just limited by the circuit response). With this technique, the real transfer function of a VCO and phase detector $T(s)$ can be measured directly. By multiplying $T(s)$ and the transfer function of the loop filter $F(s)$, the real loop gain $G(s)$ and bandwidth of a PLL can be achieved finally. The theoretical analysis and simulation of our technique for measuring the loop gain is presented in detail, and an experiment is also carried out to verify this technique. The agreement of the measurement results and theoretical calculations proves that our proposed technique is correct and reliable. Furthermore, the scheme of this technique can be easily extended to other locking systems whose loop gains should be measured precisely.

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