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Direct Power Control of Pulse Width Modulated Rectifiers without DC Voltage Oscillations under Unbalanced Grid Conditions

***Abstract*—Direct power control with space vector modulation (DPC-SVM) features simple structure, fast dynamic performance and little tuning work. However, conventional DPC-SVM can not achieve accurate power control under unbalanced grid conditions. A modified DPC-SVM is thus proposed for accurate power control under both ideal and unbalanced grid conditions. Though power control accuracy is improved when compared with conventional DPC-SVM, it still suffers highly distorted grid current and DC voltage oscillations with an unbalanced network. Therefore, a power compensation method is subsequently derived aiming at the following targets: eliminating DC voltage oscillations, achieving sinusoidal grid current and obtaining unity power factor. To that end, average grid-side reactive power and oscillations in converter-side active power are controlled as zero by simply adding a compensation to original power reference. Additionally, the proposed method does not require extraction of positive sequence or negative sequence component of grid voltage. Compared with conventional DPC-SVM in ideal grid, only additional compensation of power reference is required. As a result, control performance can be significantly improved without substantial increase of complexity. The superiority of the proposed method over the prior DPC-SVM is validated by both simulation and experimental results obtained on a two-level PWM voltage source rectifier.**

***Index Terms*—Predictive power control, power compensation, unbalanced grid**

I. Introduction

Owing to the merits of bidirectional power flow, sinusoidal grid currents and controllability of DC-link voltage, PWM rectifiers are widely used in grid-tied renewable energy applications such as wind turbine generation and solar power system [1]–[4]. In practical application, unbalanced grid voltages may occur due to poor stiffness of a weak grid, faults, unbalanced load, etc. As a consequence, control of PWM rectifiers should be designed to guarantee proper operation not only under ideal but also unbalanced grid conditions [3]–[5].

For the control of PWM rectifier, the voltage oriented control (VOC) is a popular strategy due to its simplicity and satisfactory steady-state performance. In VOC, two proportional-integral (PI) controllers are usually implemented in the synchronous reference frame for current regulation [6]. However, dynamic performance of PI controller is usually limited due to the compromise among noise immunity, stability margin and overshoot during transient process [7], [8]. Direct power control (DPC) was also widely investigated for PWM rectifier [9]–[12]. Compared to VOC, conventional table-based DPC is much simpler and more robust against parameter variation with very fast dynamic performance. By further introducing space vector modulation (SVM) into DPC, better steady state performance can be obtained than that of table-based DPC [13]–[16]. Among various DPC methods with SVM, the one based on the concept of deadbeat control is preferable for its simple principle and easy implementation [13], [15].

In the design of most control schemes, three-phase grid voltages are assumed to be balanced. Conventional methods designed for ideal grid suffer from several shortcomings under unbalanced grid conditions, such as distorted grid currents and oscillations in the DC voltage [15], [17]. To solve these issues, many improved current control schemes and power control schemes have been developed. Current control schemes are better by producing lower current distortions, while power control schemes are superior in reducing power ripples. To improve current waveform and enhance rejection ability against voltage harmonics, grid voltages are fed forward to the main controller in [18], [19] aiming at achieving balanced and sinusoidal grid currents. To avoid phase detection of grid voltage and rotating transformation, current references for achieving different control objectives are derived in stationary reference frame in [17]. Then, a proportional-resonant (PR) controller is adopted to achieve current regulation. In [20], the performance between PR controller and conventional PI controllers implemented in dual synchronous reference frame are compared. It is shown that dynamic performance of conventional PI controllers are greatly influenced by delay resulting from decomposition of positive-sequence component (PSC) and negative-sequence component (NSC). To enable flexible selection of different control objectives (i.e., elimination of negative sequence current, elimination of active power ripples and elimination of reactive power ripples), a generalized current reference is derived in [21] with voltage sensorless operation.

Apart from current control mentioned above, various power control methods are also investigated under unbalanced grid condition. In [15], constant active power and sinusoidal grid currents are achieved by DPC-SVM utilizing extended power theory [22]. However, oscillations in DC-link voltage still exist. In [23], a compensation is added to the original power reference to eliminate the negative sequence current. The principle of power compensation in [23] can be extended to achieve other control targets, such as active power ripple elimination and reactive power ripple elimination, as shown in [24]. However, sequence decomposition of grid voltage is required in the calculation of compensation. The relationship between employing extended power theory and power compensation is further evaluated in [25]. It is shown that two schemes are the same under specific circumstance. Unlike current control under unbalanced grid conditions, which has been comprehensively studied, power control schemes still

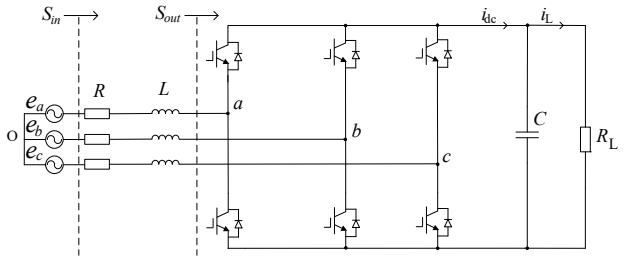


Fig. 1. Topology of a two-level PWM rectifier.

need to be further investigated. For PWM rectifier, one of the main control objectives is to obtain constant DC voltage, even if under unbalanced grid conditions. So far, existing power compensation method has not considered eliminating ripple component in DC voltage caused by unbalanced network.

To satisfy the requirement of obtaining a ripple free DC voltage, unity power factor and sinusoidal grid currents, this paper proposes a power compensation method, which works well under both balanced and unbalanced grid conditions. One contribution of this paper is that the proposed compensation scheme takes elimination of DC voltage ripple into account. Furthermore, the sequence decomposition of converter and grid voltages/ currents are no longer required. After obtaining power reference, conventional DPC-SVM is modified so that actual power can accurately track its reference when grid voltages are unbalanced. Compared with DPC-SVM presented in [13], which can only work effectively under ideal grid, the modified DPC-SVM further extend its application to unbalanced grid condition. The merits of the whole control system include: 1) no ripple in DC-link voltage; 2) sinusoidal grid currents; 3) fast dynamic response; 4) no requirement of tuning work and 5) accurate power regulation under both ideal and unbalanced grid conditions. The effectiveness of the proposed DPC-SVM is confirmed by simulation and experimental results obtained on a two-level PWM rectifier.

The remaining parts of this paper are organized as follows. Section II briefly introduces the model of PWM rectifier under unbalanced grid conditions. In Section III, a modified DPC-SVM is proposed which can achieve accurate power regulation under both ideal and unbalanced grid conditions. Additionally, a power compensation strategy is subsequently derived to obtain constant DC-link voltage and sinusoidal grid currents. Meanwhile, the average reactive power at grid-side is kept as zero. To verify the effectiveness of the proposed method, simulation and experimental results are elaborated and analyzed in Section IV. Finally, the conclusion is made in Section V.

II. Model of PWM Rectifier Under Unbalanced Network

A circuit diagram of two-level PWM rectifier is shown in Fig.1, where e_a, e_b, e_c stand for three phase grid voltages, L and R are parameters of interconnecting reactor. The model of two-level PWM rectifier can be expressed in the $\alpha\beta$ reference frame as

$$\boldsymbol{e}_{\alpha\beta} = R\boldsymbol{i}_{\alpha\beta} + L\frac{d\boldsymbol{i}_{\alpha\beta}}{dt} + \boldsymbol{v}_{\alpha\beta} \tag{1}$$

where $\boldsymbol{e}_{\alpha\beta} = e_\alpha + je_\beta$ stands for grid voltage vector, $\boldsymbol{i}_{\alpha\beta} = i_\alpha + ji_\beta$ is grid current vector and $\boldsymbol{v}_{\alpha\beta} = v_\alpha + jv_\beta$ is output voltage vector of rectifier.

According to the instantaneous power theory [26], the grid-side complex power $\boldsymbol{S}_{in}$ (AC side) and converter-side complex power $\boldsymbol{S}_{out}$ (DC side) can be expressed as

$$\boldsymbol{S}_{in} = P_{in} + jQ_{in} = 1.5\boldsymbol{i}^*_{\alpha\beta}\boldsymbol{e}_{\alpha\beta} \tag{2}$$

$$\boldsymbol{S}_{out} = P_{out} + jQ_{out} = 1.5\boldsymbol{i}^*_{\alpha\beta}\boldsymbol{v}_{\alpha\beta} \tag{3}$$

where $*$ indicates the conjugate of a complex vector.

The instantaneous input power P_{in}, Q_{in} under unbalanced grid voltage can be expressed as [15], [24], [27]

$$\begin{cases} P_{in} &= \bar{P}_{in} + \tilde{P}_{in,c}\cos(2\omega t) + \tilde{P}_{in,s}\sin(2\omega t) \\ Q_{in} &= \bar{Q}_{in} + \tilde{Q}_{in,c}\cos(2\omega t) + \tilde{Q}_{in,s}\sin(2\omega t) \end{cases} \tag{4}$$

where,

$$\begin{cases} \bar{P}_{in} &= 1.5\left(\boldsymbol{i}^+_{dq}\odot\boldsymbol{e}^+_{dq} + \boldsymbol{i}^-_{dq}\odot\boldsymbol{e}^-_{dq}\right) \\ \bar{Q}_{in} &= 1.5\left(\boldsymbol{i}^+_{dq}\otimes\boldsymbol{e}^+_{dq} + \boldsymbol{i}^-_{dq}\otimes\boldsymbol{e}^-_{dq}\right) \\ \tilde{P}_{in,c} &= 1.5\left(\boldsymbol{i}^+_{dq}\odot\boldsymbol{e}^-_{dq} + \boldsymbol{i}^-_{dq}\odot\boldsymbol{e}^+_{dq}\right) \\ \tilde{Q}_{in,c} &= 1.5\left(\boldsymbol{i}^+_{dq}\otimes\boldsymbol{e}^-_{dq} + \boldsymbol{i}^-_{dq}\otimes\boldsymbol{e}^+_{dq}\right) \\ \tilde{P}_{in,s} &= 1.5\left(\boldsymbol{i}^+_{dq}\otimes\boldsymbol{e}^-_{dq} - \boldsymbol{i}^-_{dq}\otimes\boldsymbol{e}^+_{dq}\right) \\ \tilde{Q}_{in,s} &= 1.5\left(\boldsymbol{i}^-_{dq}\odot\boldsymbol{e}^+_{dq} - \boldsymbol{i}^+_{dq}\odot\boldsymbol{e}^-_{dq}\right) \end{cases} \tag{5}$$

$\boldsymbol{e}^+_{dq} = e^+_d + \mathrm{j}e^+_q$ and $\boldsymbol{i}^+_{dq} = i^+_d + \mathrm{j}i^+_q$ denote the PSC of grid voltage and grid current in the positive-sequence synchronous reference frame; $\boldsymbol{e}^-_{dq} = e^-_d + \mathrm{j}e^-_q$ and $\boldsymbol{i}^-_{dq} = i^-_d + \mathrm{j}i^-_q$ represent the NSC of grid voltage and grid current in the negative-sequence synchronous reference frame; the superscript "+" and "−" represent PSC and NSC of a vector respectively; the subscript "c" and "s" denote cosine and sine components of power ripples respectively; the hat "$\bar{}$" and "$\tilde{}$" denote DC component and ripple component of the power respectively; $\odot$ and $\otimes$ represent dot product and cross product of two complex vectors respectively.

Similarly, the instantaneous output power P_{out}, Q_{out} as shown in (3) can be expressed as

$$\begin{cases} P_{out} &= \bar{P}_{out} + \tilde{P}_{out,c}\cos(2\omega t) + \tilde{P}_{out,s}\sin(2\omega t) \\ Q_{out} &= \bar{Q}_{out} + \tilde{Q}_{out,c}\cos(2\omega t) + \tilde{Q}_{out,s}\sin(2\omega t) \end{cases} \tag{6}$$

where,

$$\begin{cases} \bar{P}_{out} &= 1.5\left(\boldsymbol{i}_{dq}^{+}\odot\boldsymbol{v}_{dq}^{+}+\boldsymbol{i}_{dq}^{-}\odot\boldsymbol{v}_{dq}^{-}\right)\\ \bar{Q}_{out} &= 1.5\left(\boldsymbol{i}_{dq}^{+}\otimes\boldsymbol{v}_{dq}^{+}+\boldsymbol{i}_{dq}^{-}\otimes\boldsymbol{v}_{dq}^{-}\right)\\ \tilde{P}_{out,c} &= 1.5\left(\boldsymbol{i}_{dq}^{+}\odot\boldsymbol{v}_{dq}^{-}+\boldsymbol{i}_{dq}^{-}\odot\boldsymbol{v}_{dq}^{+}\right)\\ \tilde{Q}_{out,c} &= 1.5\left(\boldsymbol{i}_{dq}^{+}\otimes\boldsymbol{v}_{dq}^{-}+\boldsymbol{i}_{dq}^{-}\otimes\boldsymbol{v}_{dq}^{+}\right)\\ \tilde{P}_{out,s} &= 1.5\left(\boldsymbol{i}_{dq}^{+}\otimes\boldsymbol{v}_{dq}^{-}-\boldsymbol{i}_{dq}^{-}\otimes\boldsymbol{v}_{dq}^{+}\right)\\ \tilde{Q}_{out,s} &= 1.5\left(\boldsymbol{i}_{dq}^{-}\odot\boldsymbol{v}_{dq}^{+}-\boldsymbol{i}_{dq}^{+}\odot\boldsymbol{v}_{dq}^{-}\right) \end{cases} \tag{7}$$

It can be found from (4)-(7) that the PSC and NSC of grid voltage and grid current are required. To simplify the calculation process, original vector and its delayed value will be used in the following derivation. According to [28], [29], we can obtain PSC and NSC of $\boldsymbol{e}_{\alpha\beta}$, $\boldsymbol{v}_{\alpha\beta}$ and $\boldsymbol{i}_{\alpha\beta}$ as

$$\begin{bmatrix} \boldsymbol{e}_{dq}^{+}\\ \boldsymbol{e}_{dq}^{-}\end{bmatrix}=\frac{1}{2}\begin{bmatrix} e^{-j\omega t} & je^{-j\omega t}\\ e^{j\omega t} & -je^{j\omega t}\end{bmatrix}\begin{bmatrix} \boldsymbol{e}_{\alpha\beta}\\ \boldsymbol{e}_{\alpha\beta}^{'}\end{bmatrix} \tag{8}$$

$$\begin{bmatrix} \boldsymbol{v}_{dq}^{+}\\ \boldsymbol{v}_{dq}^{-}\end{bmatrix}=\frac{1}{2}\begin{bmatrix} e^{-j\omega t} & je^{-j\omega t}\\ e^{j\omega t} & -je^{j\omega t}\end{bmatrix}\begin{bmatrix} \boldsymbol{v}_{\alpha\beta}\\ \boldsymbol{v}_{\alpha\beta}^{'}\end{bmatrix} \tag{9}$$

$$\begin{bmatrix} \boldsymbol{i}_{dq}^{+}\\ \boldsymbol{i}_{dq}^{-}\end{bmatrix}=\frac{1}{2}\begin{bmatrix} e^{-j\omega t} & je^{-j\omega t}\\ e^{j\omega t} & -je^{j\omega t}\end{bmatrix}\begin{bmatrix} \boldsymbol{i}_{\alpha\beta}\\ \boldsymbol{i}_{\alpha\beta}^{'}\end{bmatrix} \tag{10}$$

where $\boldsymbol{e}_{\alpha\beta}^{'}$, $\boldsymbol{v}_{\alpha\beta}^{'}$ and $\boldsymbol{i}_{\alpha\beta}^{'}$ denote their quadrature values that lag $\boldsymbol{e}_{\alpha\beta}$, $\boldsymbol{v}_{\alpha\beta}$ and $\boldsymbol{i}_{\alpha\beta}$ by 90 electrical degrees, respectively.

Substituting (8), (9) and (10) into (5) and (7), the DC component of input power and the gains of ripple component of output power can be obtained as

$$\begin{cases} \bar{P}_{in} &= \frac{3}{4}(\boldsymbol{i}_{\alpha\beta}\odot\boldsymbol{e}_{\alpha\beta}+\boldsymbol{i}_{\alpha\beta}^{'}\odot\boldsymbol{e}_{\alpha\beta}^{'})\\ \bar{Q}_{in} &= \frac{3}{4}(\boldsymbol{i}_{\alpha\beta}\otimes\boldsymbol{e}_{\alpha\beta}+\boldsymbol{i}_{\alpha\beta}^{'}\otimes\boldsymbol{e}_{\alpha\beta}^{'}) \end{cases} \tag{11}$$

$$\begin{cases} \tilde{P}_{out,c} &= \frac{3}{4}\left(k_1\cos(2\omega t)+k_2\sin(2\omega t)\right)\\ \tilde{P}_{out,s} &= \frac{3}{4}\left(-k_2\cos(2\omega t)+k_1\sin(2\omega t)\right) \end{cases} \tag{12}$$

where,

$$\begin{cases} k_1 = & \boldsymbol{i}_{\alpha\beta}\odot\boldsymbol{v}_{\alpha\beta}-\boldsymbol{i}_{\alpha\beta}^{'}\odot\boldsymbol{v}_{\alpha\beta}^{'}\\ k_2 = & \boldsymbol{i}_{\alpha\beta}\odot\boldsymbol{v}_{\alpha\beta}^{'}+\boldsymbol{i}_{\alpha\beta}^{'}\odot\boldsymbol{v}_{\alpha\beta} \end{cases} \tag{13}$$

III. DPC-SVM with Elimination of DC Voltage Oscillations

A. DPC-SVM Under Unbalanced Grid Conditions

Since

$$\boldsymbol{e}_{\alpha\beta}=\boldsymbol{e}_{\alpha\beta}^{+}+\boldsymbol{e}_{\alpha\beta}^{-}, \tag{14}$$

the derivative of grid voltage can be solved as

$$\begin{aligned}\frac{d\boldsymbol{e}_{\alpha\beta}}{dt}&=j\omega\boldsymbol{e}_{\alpha\beta}^{+}-j\omega\boldsymbol{e}_{\alpha\beta}^{-}=-\omega\left(-j\boldsymbol{e}_{\alpha\beta}^{+}+j\boldsymbol{e}_{\alpha\beta}^{-}\right)\\&=-\omega\boldsymbol{e}_{\alpha\beta}^{'}.\end{aligned} \tag{15}$$

Similarly, the derivative of $\boldsymbol{e}_{\alpha\beta}^{'}$ can be obtained as

$$\frac{d\boldsymbol{e}_{\alpha\beta}^{'}}{dt}=\omega\boldsymbol{e}_{\alpha\beta} \tag{16}$$

According to (1), (2) and (15), the derivative of grid side complex power can be deduced as

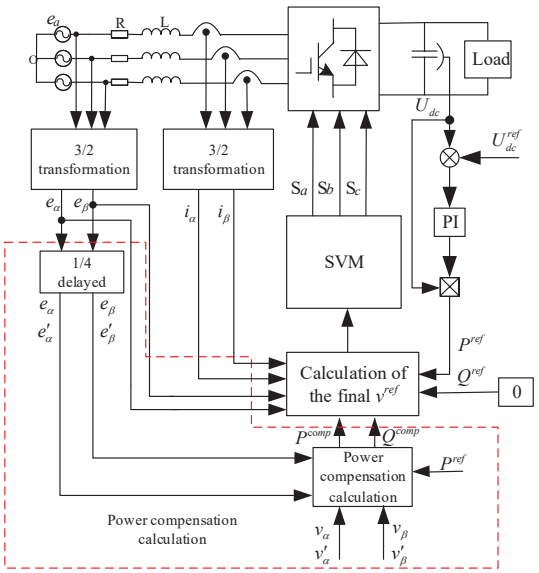


Fig. 2. Control diagram of the proposed DPC-SVM.

$$\frac{d\boldsymbol{S}_{in}}{dt}=\frac{1}{L}[\frac{3}{2}(|\boldsymbol{e}|^2-\boldsymbol{v}^{*}\boldsymbol{e})-(R+J\omega L)\boldsymbol{S}_{in}] \tag{17}$$

where

$$J=\frac{\boldsymbol{e}_{\alpha\beta}^{'}}{\boldsymbol{e}_{\alpha\beta}} \tag{18}$$

Applying first order Euler discretization to (17), the following equation can be obtained

$$\boldsymbol{S}_{in}^{k+1}=\boldsymbol{S}_{in}^{k}+\frac{T_s}{L}[\frac{3}{2}(|\boldsymbol{e}^{k}|^2-(\boldsymbol{v}^{k})^{*}\boldsymbol{e}^{k})-(R+J\omega L)\boldsymbol{S}_{in}^{k}], \tag{19}$$

where T_s is the control period. For deadbeat power control, actual power should equal the reference at the next sampling instant, i.e.,

$$\boldsymbol{S}_{in}^{k+1}=\boldsymbol{S}^{ref}. \tag{20}$$

Solving (20) based on (19), the desired voltage vector nullifying the tracking error of complex power in the next control period is obtained as

$$\boldsymbol{v}^{ref}=\boldsymbol{e}^{k}-\frac{2}{3}\left(\frac{(R+J^{k}\omega L)\boldsymbol{S}_{in}^{k}}{\boldsymbol{e}^{k}}\right)^{*}-\frac{2L}{3T_s}\left(\frac{\boldsymbol{S}^{ref}-\boldsymbol{S}_{in}^{k}}{\boldsymbol{e}^{k}}\right)^{*}. \tag{21}$$

For a ideal grid, $J=\boldsymbol{e}_{\alpha\beta}^{'}/\boldsymbol{e}_{\alpha\beta}=-j$ holds. In this case, $\boldsymbol{v}^{ref}$ in (21) is the same as that of conventional DPC-SVM presented in [15], which is a special case of (21) in this paper. It will be shown in Section IV that conventional DPC-SVM can not achieve accurate power regulation with unbalanced grid voltages while the modified DPC-SVM in this paper can work properly under both ideal and unbalanced grid conditions.

B. Reference Compensation for Eliminating DC Voltage Ripples

Though the DPC-SVM in Section III-A can achieve accurate power tracking with unbalanced grid voltages, it suffers from highly distorted current and oscillations in the DC-link voltage if power references are kept the same as that derived under ideal grid voltage. In this paper, a power compensation scheme will be proposed to obtain sinusoidal grid current and unity power factor while eliminating the oscillation in DC-link voltage under unbalanced network. As DC voltage oscillation is related to the active power ripple in the converter side, the control targets can be mathematically expressed based on (11) and (12) as:

$$\begin{cases} \bar{P}_{in} = \frac{3}{4}(\boldsymbol{i}_{\alpha\beta} \odot \boldsymbol{e}_{\alpha\beta} + \boldsymbol{i}'_{\alpha\beta} \odot \boldsymbol{e}'_{\alpha\beta}) & = P^{ref} \\ \bar{Q}_{in} = \frac{3}{4}(\boldsymbol{i}_{\alpha\beta} \otimes \boldsymbol{e}_{\alpha\beta} + \boldsymbol{i}'_{\alpha\beta} \otimes \boldsymbol{e}'_{\alpha\beta}) & = 0 \\ \tilde{P}_{out,c} = \frac{3}{4}(k_1 \cos(2\omega t) + k_2 \sin(2\omega t)) & = 0 \\ \tilde{P}_{out,s} = \frac{3}{4}(-k_2 \cos(2\omega t) + k_1 \sin(2\omega t)) & = 0 \end{cases} \tag{22}$$

From (13) and (22), the final current reference vector can be calculated as

$$\begin{aligned} \begin{bmatrix} i_\alpha^{ref} \\ i_\beta^{ref} \end{bmatrix} =& \frac{4P^{ref}}{3\triangle} \begin{bmatrix} (v_\alpha v'_\beta - v_\beta v'_\alpha)e_\alpha \\ (v_\alpha v'_\beta - v_\beta v'_\alpha)e_\beta \end{bmatrix} \\ &+ \frac{4P^{ref}}{3\triangle} \begin{bmatrix} (v_\alpha v_\beta + v'_\beta v'_\alpha)e'_\alpha \\ -(v_\alpha v_\beta + v'_\beta v'_\alpha)e'_\beta \end{bmatrix} \\ &+ \frac{4P^{ref}}{3\triangle} \begin{bmatrix} (v_\beta^2 + v_\beta'^2)e'_\beta \\ -(v_\alpha^2 + v_\alpha'^2)e'_\alpha \end{bmatrix} \end{aligned} \tag{23}$$

where $\triangle = (v_\alpha v'_\beta - v_\beta v'_\alpha)(e_\alpha^2 + e_\alpha'^2 + e_\beta^2 + e_\beta'^2) + (e_\alpha e'_\beta - e'_\alpha e_\beta)(v_\alpha^2 + v_\alpha'^2 + v_\beta^2 + v_\beta'^2)$. The new complex power reference can then be calculated from current reference as

$$\boldsymbol{S}_{new}^{ref} = 1.5\boldsymbol{i}^{ref*}\boldsymbol{e} \tag{24}$$

where $\boldsymbol{i}^{ref} = i_\alpha^{ref} + j i_\beta^{ref}$.

As the original power reference $\boldsymbol{S}^{ref}$ is known, a more straightforward and natural solution is to add an appropriate compensation term to original power reference. The power compensation value $\boldsymbol{S}^{comp}$ is calculated as $\boldsymbol{S}^{comp} = \boldsymbol{S}_{new}^{ref} - \boldsymbol{S}^{ref}$ and its components can be expressed as follows.

$$\begin{aligned} P^{comp} = \frac{P^{ref}}{\triangle} \Big[& (e_\alpha^2 + e_\beta^2 - e_\alpha'^2 - e_\beta'^2)(v_\alpha v'_\beta - v_\beta v'_\alpha) \\ & - (v_\alpha^2 + v_\alpha'^2 - v_\beta^2 - v_\beta'^2)(e_\alpha e'_\beta + e_\beta e'_\alpha) \\ & + 2(e_\alpha e'_\alpha - e_\beta e'_\beta)(v_\alpha v_\beta + v'_\alpha v'_\beta) \Big] \end{aligned} \tag{25}$$

$$\begin{aligned} Q^{comp} = \frac{P^{ref}}{\triangle} \Big[& 2e_\alpha e'_\alpha (v_\alpha^2 + v_\alpha'^2) + 2e_\beta e'_\beta (v_\beta^2 + v_\beta'^2) \\ & + 2(e_\alpha e'_\beta + e_\beta e'_\alpha)(v_\alpha v_\beta + v'_\alpha v'_\beta) \Big] \end{aligned} \tag{26}$$

The control diagram of the proposed DPC-SVM with power compensation is shown in Fig. 2. Compared with the structure of conventional DPC-SVM under ideal grid conditions, there is only a additional power compensation block. After obtaining power compensation according to (25) and (26), the reference voltage $\boldsymbol{v}^{ref}$ that can force actual power to follow their references is calculated according to (21). Finally, the SVM is used to generate switching signals for the converter to synthesize the calculated $\boldsymbol{v}^{ref}$.

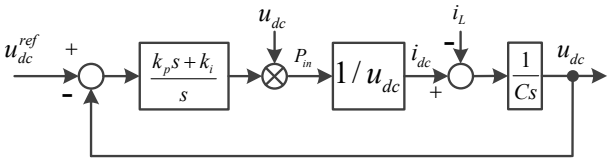


Fig. 3. Control diagram of DC voltage regulation loop.

C. Design of DC Voltage Controller

The dynamics of DC voltage can be described as

$$C\frac{dU_{dc}}{dt} = i_{dc} - i_L \tag{27}$$

where C denotes DC-link capacitor; i_{dc} represents rectifier-side DC current as shown in Fig. 1 and i_L is load current. Neglecting power losses, the DC-side output power should equal AC-side input power, i.e.,

$$P_{in} = U_{dc} i_{dc}. \tag{28}$$

Based on (27) and (28), the following equation can be derived

$$C\frac{dU_{dc}}{dt} = \frac{P_{in}}{U_{dc}} - i_L. \tag{29}$$

From the above equations, the control diagram of DC voltage regulation loop can be depicted in Fig. 3. It should be noted that PI output is multiplied by U_{dc} to cancel the gain $1/U_{dc}$ in (29). In this way, PI gains can be tuned independent of U_{dc}. The transfer function can be easily derived as

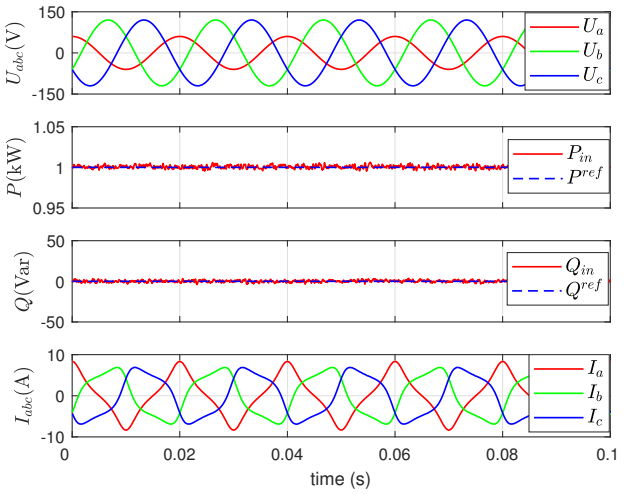
$$\frac{U_{dc}}{U_{dc}^{ref}} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \tag{30}$$

where $\xi = k_p/(2\sqrt{k_i C})$ and $\omega_n = \sqrt{k_i/C}$; k_p and k_i are PI gains needs to be designed, which can be solved as

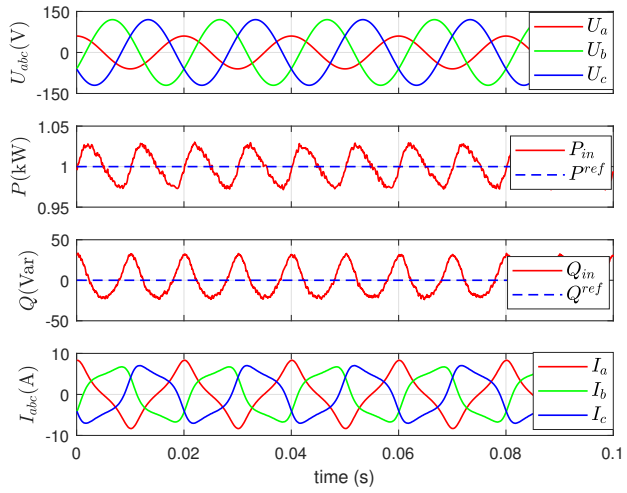
$$k_p = 2C\xi\omega_n \tag{31}$$

$$k_i = C\omega_n^2 \tag{32}$$

It is seen from (30) that DC voltage regulation loop is a second-order system. In this paper, the damping ratio ξ is set as $\xi = \sqrt{2}/2$ which is usually selected for acceptable overshoot during transient process. And ω_n is chosen as $\omega_n = 100$ rad/s for the compromise between dynamic responses and immunity against noises and harmonics. Experimental results shown in Section IV-B can confirm the effectiveness of the selected PI gains.

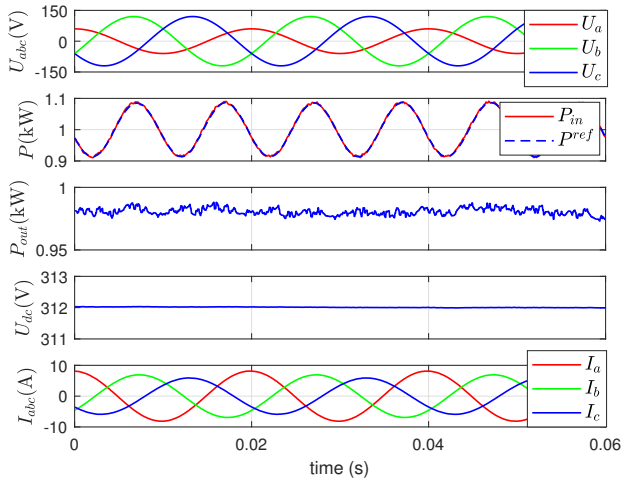


(a)

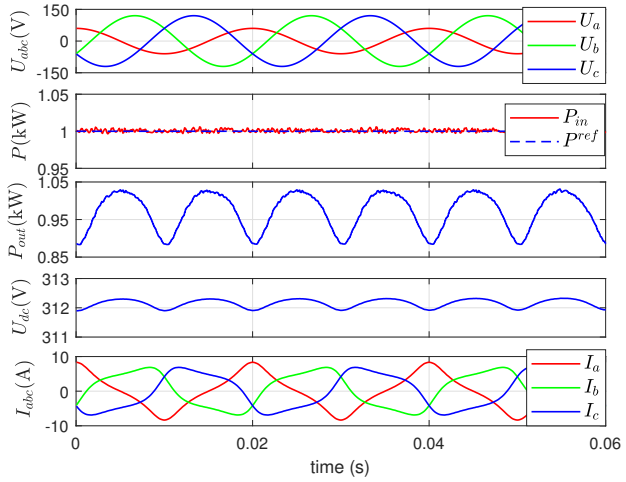


(b)

Fig. 4. Simulation results of U_{abc}, P_{in}, P^{ref}, Q_{in}, Q^{ref} and I_{abc} for (a) the MDPC-SVM and (b) CDPC-SVM.



(a)



(b)

Fig. 5. Simulation results of U_{abc}, P_{in}, P^{ref}, P_{out}, U_{dc} and I_{abc} for (a) MDPC-SVM-PC and (b) MDPC-SVM.

IV. Simulation and Experimental Results

TABLE I
System and Control Parameters

System Parameters	Symbol	Value
Line resistance	R	0.3 Ω
Line inductance	L	10 mH
Line-line voltage	U_N	150 V
Line voltage frequency	f_g	50 Hz
Load resistance	R_L	100 Ω
Sampling period	T_s	100 μs

A. Simulation Results

To verify the effectiveness of the proposed method, it is tested in the environment of Matlab/Simulink. The sampling frequency is set as 10 kHz for all the methods presented in this paper. Other control and system parameters are shown in Table I. First, the validity of the modified DPC-SVM (MDPC-SVM) in Section III-A is tested and compared with the conventional DPC-SVM (CDPC-SVM) introduced in [15]. Then, the MDPC-SVM with power compensation (MDPC-SVM-PC) is examined to confirm the effectiveness of power compensation derived in the Section III-B. To decouple the influence of DC voltage regulation on the control performance, the outer proportional-integral (PI) DC voltage controller is disabled in simulation tests and the rectifier works in power control mode. In the following tests, the original power references are set as $P^{ref} = 1$ kW and $Q^{ref} = 0$ Var.

Fig. 4 shows waveform of grid voltages U_{abc}, grid-side active power P_{in}, grid-side reactive power Q_{in} and grid currents I_{abc} when there is 50% voltage dip in phase A. It is clear that the P_{in} and Q_{in} can be regulated to follow their references accurately in the proposed MDPC-SVM. However, in the CDPC-SVM, there are obvious tracking errors with twice grid-frequency oscillations in the actual power. This test confirms that the conventional DPC-SVM cannot accurately force the actual power to track their references when grid voltages are unbalanced. While the proposed MDPC-SVM can work properly under an unbalanced network. As power compensation strategy as shown in the Section III-B is not implemented, significant distortions can be seen in grid currents for both methods.

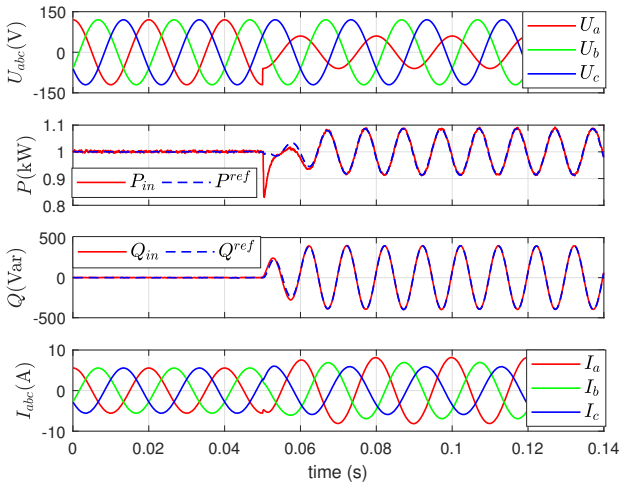


Fig. 6. Simulation results of MDPC-SVM-PC when 50% voltage dip in phase A is suddenly applied.

Fig. 5 shows simulation results of the proposed MDPC-SVM and MDPC-SVM-PC when there is 50% voltage dip in phase A. It can be seen that though grid-side power P_{in} presents oscillations, the converter-side power P_{out} and DC-link voltage U_{dc} are almost constant in MDPC-SVM-PC. On the contrary, P_{in} is constant in the MDPC-SVM. This result in oscillations in P_{out} and U_{dc}. Additionally, grid currents are highly distorted in the MDPC-SVM, while i_{abc} are sinusoidal for the MDPC-SVM-PC. As MDPC-SVM-PC is the combination of MDPC-SVM and power compensation as shown in (25) and (26), the superior performance of MDPC-SVM-PC over MDPC-SVM in this test validates the necessity of power compensation when grid voltages are unbalanced.

Fig. 6 shows simulation results when grid voltages change from balanced condition to unbalanced condition. At 0.05s, 50% voltage dip in phase A is suddenly applied to evaluate transient performance of MDPC-SVM-PC. It can be found that there is a drop in actual active power P_{in} after a sudden voltage sag. However, it can return to its reference quickly. With an ideal grid, both power references P^{ref} and Q^{ref} are kept the same as the original value. Hence, the proposed power compensation would not affect normal operation when grid voltages are balanced. However, once the grid voltages are unbalanced, twice grid-frequency oscillations are added to original power references. As verified in Fig. 5, this helps to obtain a constant DC-link voltage and sinusoidal grid currents.

From simulation tests in this section, it can be concluded that the proposed MDPC-SVM-PC can accurately control the actual power under unbalanced grid conditions where the conventional DPC-SVM fails to work properly. Additionally, twice grid-frequency oscillations in the converter-side active power P_{out} and DC-link voltage U_{dc} can be removed while maintaining sinusoidal grid currents by the proposed power compensation.

To evaluate the robustness against parameter mismatches, the proposed MDPC-SVM-PC is tested when the inductance and resistance used in the controller are 50% and 150% of their actual values. The results are shown in Fig. 7. In the

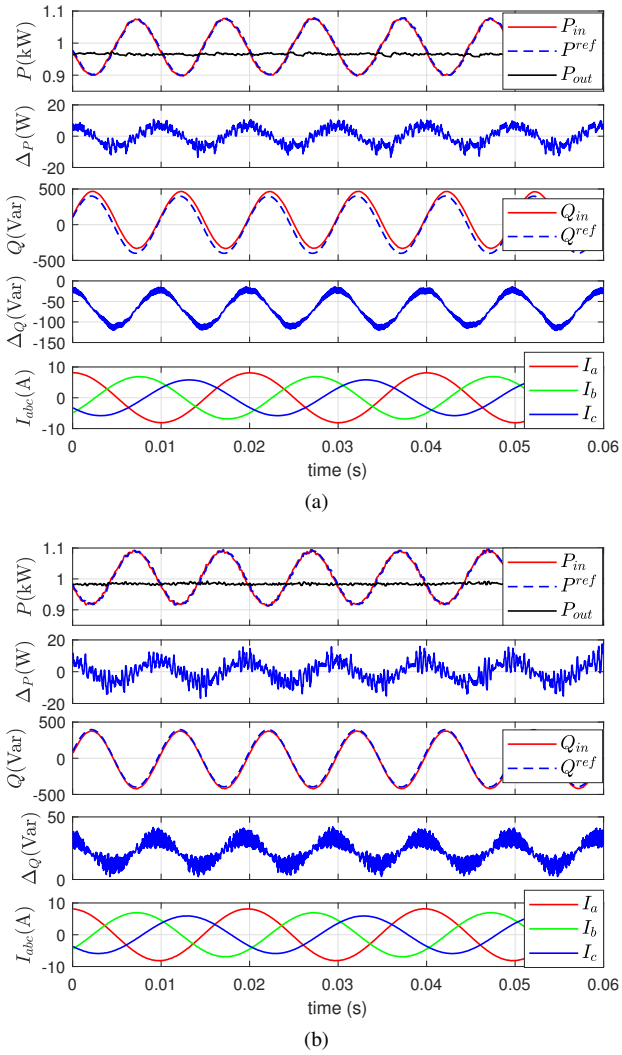


Fig. 7. Simulation results of MDPC-SVM-PC when both R and L in the controller are (a) 50% and (b) 150% of their actual value.

figure, $\Delta P = P^{ref} - P_{in}$ and $\Delta Q = Q^{ref} - Q_{in}$ are tracking errors of active power and reactive power respectively. It is seen that there are some tracking errors in both active power and reactive power under parameter mismatches. However, the controller is still stable and works well under unbalanced grid conditions. There phase grid currents are sinusoidal and there is no oscillation in converter-side power P_{out}. To eliminate the negative influence of parameter mismatches, it is suggested to use the online parameter identification technique, as shown in [11]. However, this part is out of scope of this paper and will not be further expanded.

Fig. 8 shows the simulated results of MDPC-SVM-PC when phase A is short-circuited to the ground. It can be seen that when phase-A voltage decreases to zero, the active power P_{in} can return to its reference quickly after a drop. With the proposed power compensation, the converter side active power P_{out} can be kept constant without oscillations after transient process even under severely unbalanced grid conditions. Due to the voltage sag, peak value of phase current is increased to maintain output power. In practical application, power references may be limited as studied in [3], [30] to avoid

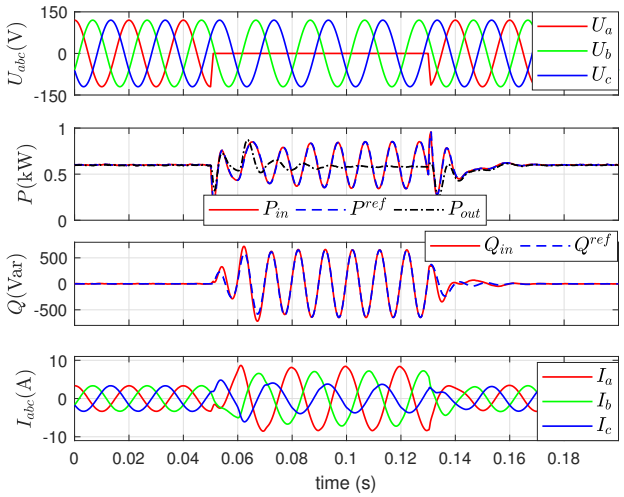
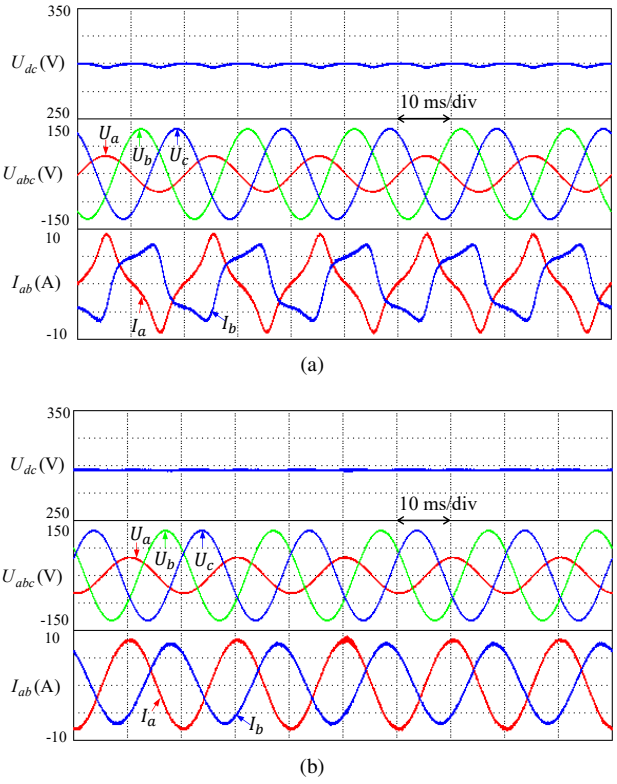


Fig. 8. Simulated results of MDPC-SVM-PC under one phase grounding fault.



(a)

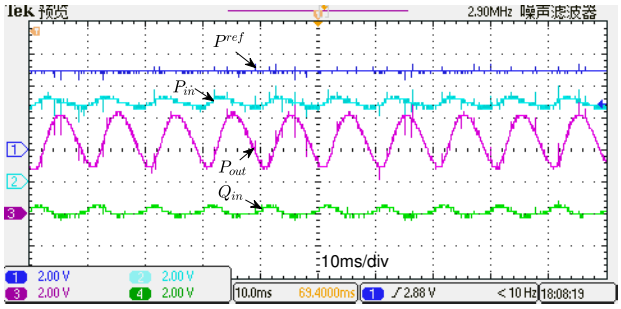
(b)

Fig. 9. Experimental results of (a) MDPC-SVM and (b) MDPC-SVM-PC under unbalanced grid conditions.

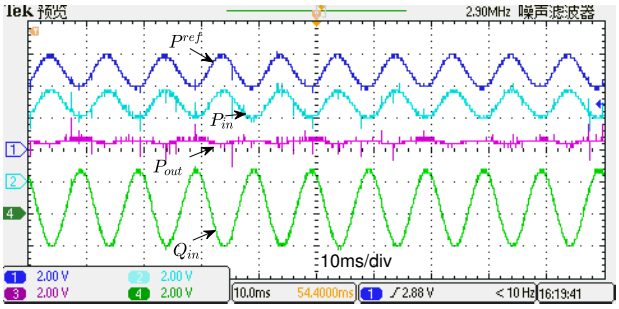
overcurrent when voltage sag occurs. After clearing of the fault, the system quickly recoveries to normal operation. This test further confirms that the proposed method can properly work under both ideal and unbalanced grid conditions.

B. Experimental Results

To further confirm the effectiveness of the MDPC-SVM-PC, experimental results obtained from a two-level PWM rectifier under both balanced and unbalanced grid voltage conditions are presented. The results of MDPC-SVM that without power



(a)



(b)

Fig. 10. Steady-state responses of P^{ref}(400W/div), P_{in}(400W/div), P_{out}(400W/div) and Q_{in}((a):120Var/div,(b):400Var/div) under unbalanced grid voltages for (a) MDPC-SVM, and (b) MDPC-SVM-PC.

compensation are also illustrated for comparison. A 32-bit floating DSP TMS320F28335 was used to implement the control algorithm. The control and system parameters are the same as that used in the simulation, as listed in Table I. The block diagram of the proposed MDPC-SVM-PC is shown in Fig. 2. During experimental tests, unbalanced grid voltages are generated using a three-phase programmable ac source (Chroma 61511), in which 60% voltage dip in phase A is applied. The internal variables such as P^{ref}, P_{in}, P_{out} and Q_{in} are displayed on a digital oscilloscope via an on-board DA converter (DAC7724U), while the the DC-link voltage U_{dc}, three phase grid voltages U_{abc} and line currents I_{ab} are displayed on a scopecorder DL850, which are obtained directly by voltage and current probes. Similar to simulation tests, to clearly show the influence of power control on U_{dc} with unbalanced grid voltages, DC voltage controller is disabled at the beginning of several tests. The obtained results are illustrated in Figs. 9-15. After that, outer PI controller is enabled to further verify the effectiveness of the proposed method in closed-loop DC voltage regulation.

Fig. 9 shows comparative results for MDPC-SVM-PC and MDPC-SVM. It is seen that grid currents are significantly distorted in MDPC-SVM. Additionally, U_{dc} exists twice-grid frequency oscillations. The peak-to-peak ripple of U_{dc} is about 1.67 V. If the proposed power compensation is implemented, the ripple in U_{dc} disappears, as can be seen in the responses of MDPC-SVM-PC. Although grid currents are unbalanced, they are sinusoidal in the shape for MDPC-SVM-PC. The experimental results are very similar to that presented in simulation. This test justifies again that the proposed power compensation can eliminate ripples in DC

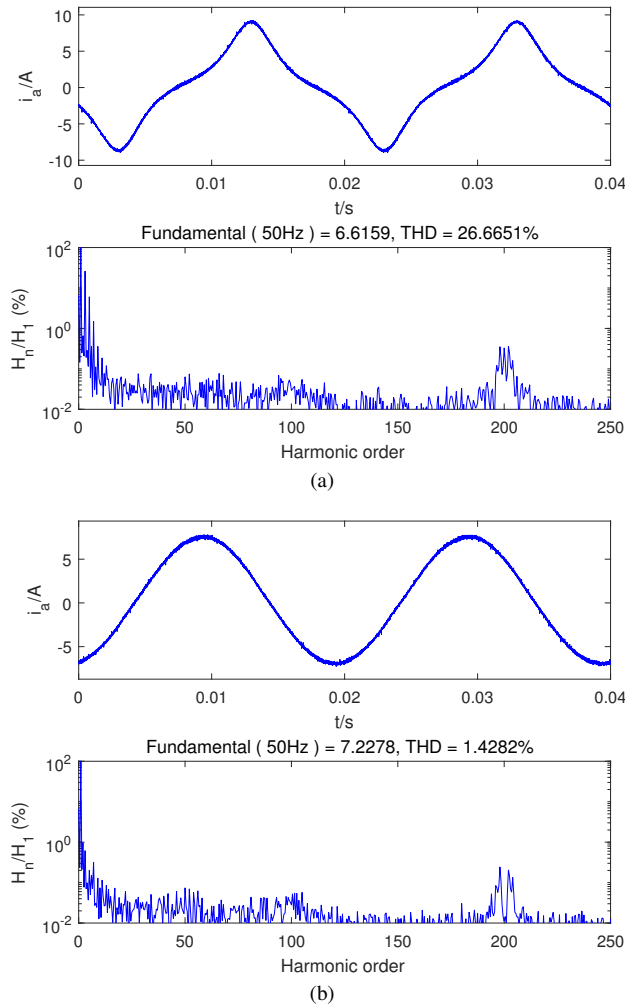


Fig. 11. Spectrum analysis of grid current for (a) MDPC-SVM and (b) MDPC-SVM-PC.

link voltage while obtaining sinusoidal grid currents when grid voltage are unbalanced. From the corresponding responses of the active power and reactive power shown in Fig. 10, one can see that P_{in} in MDPC-SVM is kept constant. However, the converter-side active power P_{out} exists significant twice-grid frequency oscillations, which accounts for ripples in the DC-link voltage. With power compensation, thought the grid-side power P_{in} is not a constant, the output power P_{out} presents much lower oscillations in MDPC-SVM-PC. This is conductive to obtaining a DC-link voltage free from twice-grid frequency harmonics.

Fig. 11 shows harmonic spectrum of one-phase grid current with power references as $P^{ref} = 1000$ W and $Q^{ref} = 0$ Var for MDPC-SVM and MDPC-SVM-PC. To calculate harmonic components, the sampled current is transferred to the PC and analyzed by Matlab function "fft". It can be clearly seen that the grid current contains significant harmonics in MDPC-SVM and the current THD is as high as 26.7%. On the contrary, by using the proposed power compensation, the current THD is only 1.43% in MDPC-SVM-PC, which is much lower than that of MDPC-SVM.

The dynamic responses of U_{dc} and i_{ab} are recorded in Fig. 12. In this test, the active power reference steps from 600

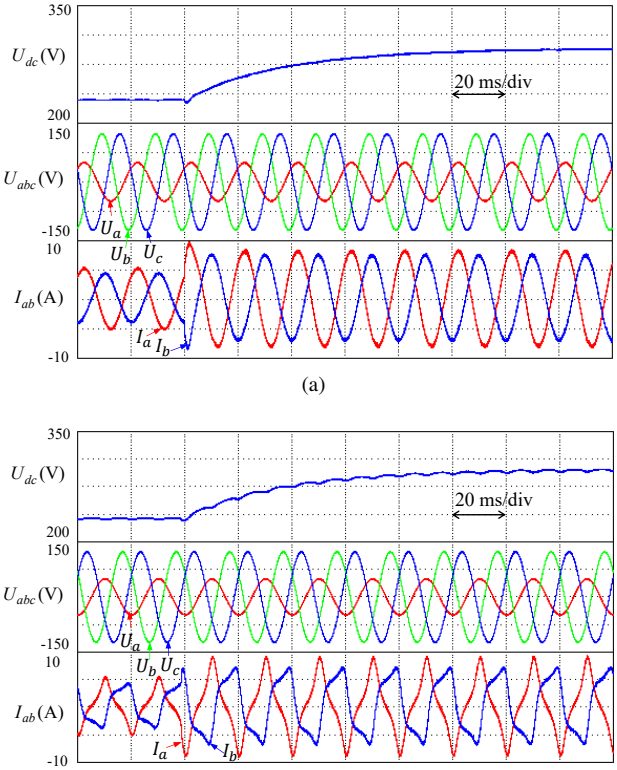


Fig. 12. Dynamic responses when P^{ref} steps from 600 W to 1 kW for (a) MDPC-SVM-PC and (b) MDPC-SVM under unbalanced grid conditions.

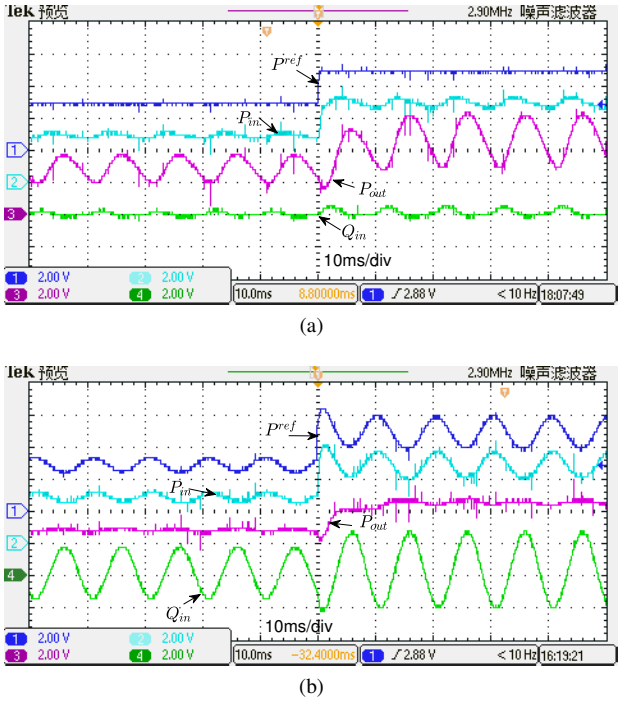


Fig. 13. Dynamic responses of P^{ref}(400W/div), P_{in}(400W/div), P_{out}(400W/div) and Q_{in}((a):120Var/div,(b):400Var/div) under unbalanced grid voltages when P^{ref} steps from 600 W to 1000 W for (a) MDPC-SVM and (b) MDPC-SVM-PC.

W to 1000 W while Q^{ref} is kept at zero. It is seen that even during the transient process, grid currents are sinusoidal

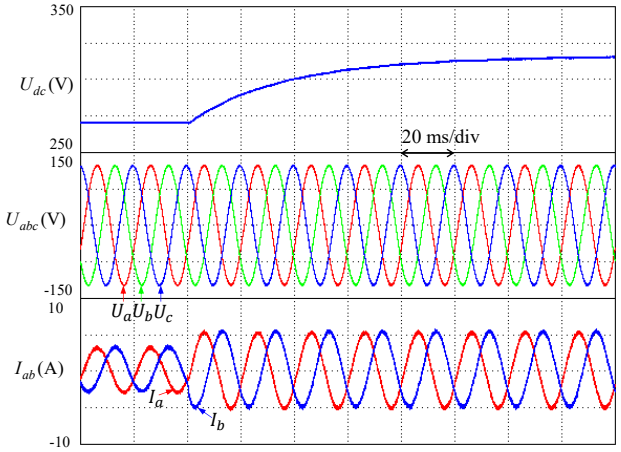


Fig. 14. Dynamic responses when P^{ref} steps from 600 W to 1 kW under ideal grid conditions for MDPC-SVM-PC.

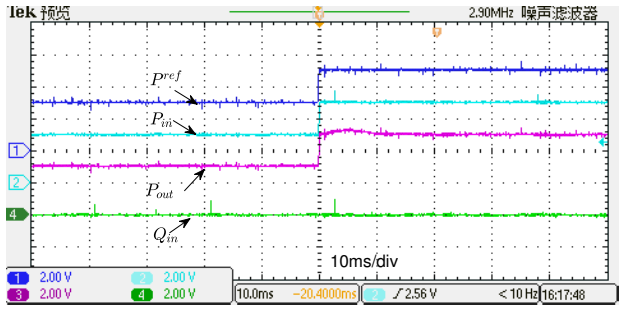


Fig. 15. Dynamic responses of MDPC-SVM-PC under ideal grid conditions when P^{ref} steps from 600 W to 1 kW. P^{ref}(400W/div), P_{in}(400W/div), P_{out}(400W/div) and Q_{in}(400Var/div).

and there is no oscillations in the U_{dc} for MDPC-SVM-PC. By contrast, MDPC-SVM presents obvious ripples in U_{dc} and significant harmonics in grid currents. The corresponding power responses are shown in Fig. 13. For both methods, P_{in} can track P^{ref} quickly during transient process. In MDPC-SVM, the original power reference is not modified, which is constant during steady state. The output power P_{out} presents large twice-grid frequency harmonics. In MDPC-SVM-PC, both P^{ref} and Q^{ref} oscillates at twice-grid frequency after employing power compensation. However, P_{out} is nearly constant during steady-state operation. Hence, the ripple in U_{dc} is greatly reduced compared with that in MDPC-SVM.

From the above tests, it can be concluded that MDPC-SVM-PC works well under unbalanced grid conditions, which can achieve constant DC-link voltage and sinusoidal grid currents when grid voltages are unbalanced. Its performance under an ideal grid condition is also tested and the result is shown in Fig. 14. It is seen that MDPC-SVM-PC works well with an ideal grid. The current are sinusoidal and there is no ripples in DC-link voltage. From the power responses as shown in Fig. 15, it can be found that power reference P^{ref} is a constant as same as the original power reference. There is no oscillations in active power P_{in}, P_{out} and reactive power Q_{in} during steady state. Hence, the proposed power compensation has no impact on operation for an ideal grid, indicating that the proposed methods are applicable for both ideal and unbalanced

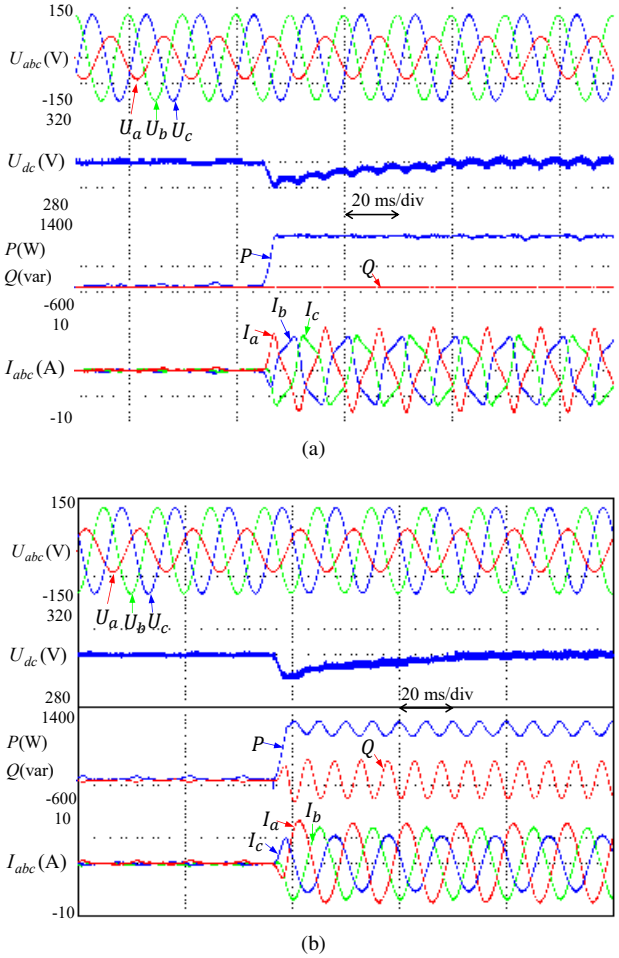


Fig. 16. Performance of closed-loop DC-link voltage control when the external load is suddenly applied under unbalanced grid conditions for (a) MDPC-SVM and (b) MDPC-SVM-PC.

grid conditions, as also confirmed in simulation results in Fig. 6.

After verifying effectiveness of the proposed method on eliminating DC voltage oscillations in power control mode, closed-loop DC voltage control is tested under unbalanced grid conditions. Fig. 16 shows responses of DC-link voltage when the external load is suddenly applied. In this test, U_{dc}^{ref} is set as 300 V and the active power reference P^{ref} is generated by a PI controller as shown in Fig. 2. It is seen that U_{dc} quickly returns to its reference after load is applied for both control schemes. However, MDPC-SVM suffers from significant DC voltage oscillations and distorted grid currents, while the proposed method presents much better performance in terms of smoother DC voltage and sinusoidal grid currents. This test further validates that the proposed method can effectively eliminate DC-voltage oscillations under an unbalanced network.

V. Conclusion

In existing literature, most studies on DPC-SVM were carried out under balanced grid voltage conditions. Under unbalanced grid voltage conditions, the steady-state performance of DPC-SVM are seriously deteriorated by exhibiting

highly distorted current and oscillations in the DC-link voltage. To cope with these problems, this paper proposes a novel DPC-SVM method, which is able to work effectively under both balanced and unbalanced grid conditions. An appropriate power compensation is derived, which only requires the grid/converter voltages and their delayed values. By adding this power compensation to the original power references without modifying the internal control structure, constant DC-link voltage and sinusoidal grid currents are achieved simultaneously without affecting the average value of grid-side active power and reactive power. The proposed DPC-SVM is compared to conventional DPC-SVM and its effectiveness is confirmed by the presented simulation and experimental results.

Due to additional calculation of power compensation, complexity of the proposed DPC-SVM is higher than conventional power control schemes. However, twice grid voltage frequency oscillations can be completely eliminated in theory by the proposed method under unbalanced grid conditions, which is beneficial to the lifetime and maintenance of capacitors. Although using a larger capacitor can also reduce DC voltage ripples, it may increase hardware cost and volume of the system. In this sense, the proposed method is more suitable for the application where a high quality DC voltage is required under unbalanced grid conditions.

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