DIRECT RF SAMPLING MIXER WITH RECURSIVE FILTERING IN CHARGE DOMAIN

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ABSTRACT

We present a novel direct RF sampling technique in which an input RF signal is converted to a current waveform, gated and integrated on a sampling capacitor. A rotating capacitor shares this charge with the main sampling capacitor and transfers it to a subsequent discrete-time switched-capacitor filter stage. This action creates a first order IIR filter which serves as an anti-alias filter for subsequent stages. The transfer function of this stage can be changed by adjusting the clock signal controlling the rotating capacitor. This approach has been validated and incorporated in a commercial Bluetooth receiver IC realized in a digital 130 nm CMOS that meets or exceeds performance of other conventional Bluetooth radio architectures.

1. INTRODUCTION

Wireless receivers are typically constructed as continuous-time architectures that perform down-conversion and sufficient filtering so that the largest interferer can fit in the available voltage headroom without creating excessive non-linearity. Despite a wealth of knowledge on architectures and circuits for low-power and low-area applications, aggressive cost targets are pushing for higher level of integration where analog circuits must share the same die as the state-of-the-art low-cost digital process without adding any cost to the baseline process. This has resulted in a constant struggle to develop new solutions that are low-cost and at the same time provide the necessary performance to meet existing RF standards in the face of shrinking voltage supply headroom [1, 2, 3, 4]. Equally important is the realization to push the complexity from analog domain to digital domain, where it is easy to apply complex signal processing approaches to make up for the problems in the analog implementations.

Discrete-time analog is typically used in IF sections where the general belief held is that such stages produce more noise and therefore are not suitable for application to the front-end electronics. The main reason is that discrete-time implementations suffer from noise folding and in the absence of sufficient antialiasing filtering, the folded noise adds up dramatically [5]. Additionally, the clock jitter places an irreducible noise floor which creates a limit on the available dynamic range [6]. The advantage of such stages is that good component matching is generally available which provides excellent control over the performance of the circuit.

We present the approach of direct RF sampling in which an input RF signal is converted to a current waveform, downconverted and integrated on a sampling capacitor. A rotating capacitor shares this charge with the main sampling capacitor and transfers it to a subsequent discrete-time switched-capacitor IF filter stage. The sampling is performed at the Nyquist rate of the RF carrier. A decimation in time is performed on the collective sampling and rotating capacitor while the incoming RF signal is accumulated on this total capacitance. This creates filtering which provides good antialiasing to the folding frequencies in narrowband RF standards such as Bluetooth. As the rotating capacitor rotates, the charge sharing between the sampling and rotating capacitor creates a first order IIR filter that serves as an anti-alias filter for subsequent stages. The transfer function of this stage can be scaled in frequency by adjusting the rate of rotation of the rotating capacitor. This filtering also helps relax the linearity requirements of subsequent analog blocks while a narrow selectivity could be achieved that is controlled by a capacitor ratio.

2. DIRECT SAMPLING MIXER

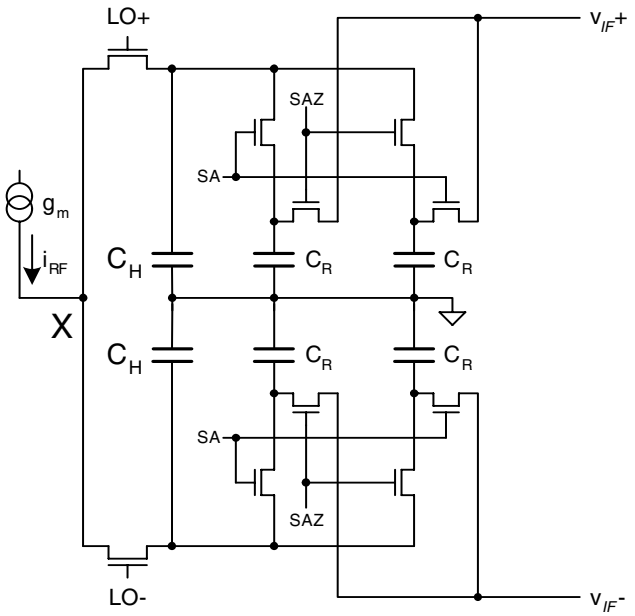

Fig. 1. Direct sampling mixer.

The basic idea of the current-mode *direct sampling mixer* (DSM) is shown in Fig. 1. A *low-noise transconductance amplifier* (LNTA) converts the received RF voltage v_{RF} into i_{RF} in current domain through the transconductance gain g_m. The current i_{RF}

gets switched by the half-cycle of the *local oscillator* (LO) and integrated into the sampling capacitor, $C_s = C_H + C_R$. The diagram shows both sides of the pseudo-differential architecture. On each side, a rotating capacitor C_R together with a history capacitor C_H combine to form the sampling capacitor C_s on which the input RF signal is accumulated. The digital clocking signal SAZ is the inverse of signal SA such that whenever one rotating capacitor is connected to C_H, the second capacitor is connected to the output. The rate of rotation can be arbitrarily chosen by adjusting the frequency of the clock applied at SA.

There are many parallels between a Gilbert cell mixer driving a switched capacitor load and the proposed structure. However, such a structure has not been investigated. In this paper, we will focus on the behavioral description and analysis of this structure in subsequent sections. The approach we use is to separate the different operations performed by this structure.

2.1. Gm-C Filtering Operation

The load seen by the g_m stage is always constant since one of the two rotating capacitors is always in parallel with C_H. The total sampling capacitance, $C_s = C_H + C_R$ is therefore constant. If the LO oscillating at f_0 frequency is synchronous and in phase with the sinusoidal RF waveform, the voltage gain of a single RF half-cycle is

$$G_{v,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot \frac{g_m}{C_s} \tag{1}$$

In the above equations, the $\frac{1}{\pi}$ factor is contributed by the half-cycle sinusoidal integration. As an example, if g_m = 30 mS, C_s = 15.925 pF and f_0 = 2.4 GHz, then $G_{v,RF}$ = 0.25.

The clock jitter spectrum of the LO appears at the output of the mixer and the dynamic range at the mixer output is ensured by keeping the clock jitter below a certain required value. In fact, the local oscillator jitter value of only $\sigma_{\Delta t} = 100\ fs$ (corresponding to -150 dBc/Hz noise floor at f_0 = 2.4 GHz) is certainly well below the amplitude noise. Using [7]

$$SNR = -20\log(2\pi f_{RF}\sigma_{\Delta t}) \tag{2}$$

that expresses the SNR limitation due to the sampling jitter, we obtain SNR = 56 dB, so the clock jitter does not limit performance of the Bluetooth system.

The clock applied to SA is an integer division by N of the LO clock. By changing N, it is possible to change the load

$$R_{eq} = \frac{1}{f_0/N \cdot C_R} \tag{3}$$

emulated by C_R that is constant for a fixed value of N.

2.2. Temporal Moving Average

The temporal integration of N half-rectified RF samples performs a *finite-impulse response* (FIR) operation with N all-one coefficients, also known as *moving-average* (MA), according to

$$w_i = \sum_{l=0}^{N-1} u_{i-l} \tag{4}$$

where, u_i is the ith RF sample of the input charge sample, w_i is the accumulated charge. Its frequency response is a sinc function and is shown in Fig. 2 for $N = 8$ (solid line) and $N = 7, 9$ (dotted lines) with sampling rate f_0 = 2.4 GHz. Since the charge accumulation is done on the same capacitor, the MA filtering does not suffer from analog mismatch effects.

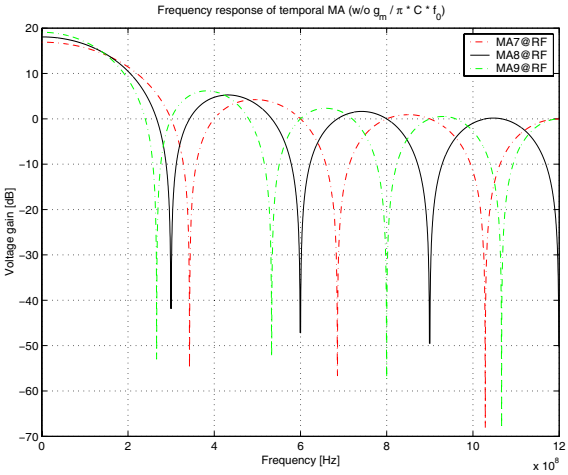

Fig. 2. Transfer function of the temporal MA operation at RF rate.

Due to the fact that the MA output is being read out at the lower rate of N RF clock cycles, there is an additional aliasing with foldover frequency at $f_0/2N$ and located halfway to the first notch. Consequently, the frequency response of MA=7 with decimation of 7 exhibits less aliasing and features wider notches than MA=8 or MA=9 with decimation of 8 or 9, respectively. These notches protect against the noise folded from the foldover frequencies. The width of the notches can be increased by decimating by a smaller N at the cost of a higher readout rate.

The charge accumulation over N samples results in a larger voltage gain. This fact was also described in [5] where the author applied this principle on an IF filter. Ideally, the gain over accumulation of N samples is equal to N for charge as well as voltage gain. However, in reality, our measurements indicate that the parasitics at node X in Fig. 1 cause a loss of gain as charge from C_s constantly leaks out. The longer is the integration period, the more loss is incurred in the charged accumulated in the earlier samples. To study this effect, we modeled the charge loss from C_s as a linear function of time to see its effects.

Fig. 3 shows the effects of the parasitics at node X using three different rates of charge leakage. It shows that the depth of the notch is limited by the rate at which the charge leaks out. Consequently, in order to get an excellent depth of notch, it is important to pay special attention of the node X parasitics. Fig. 3 reveals that the charge leakage of 1/100 is the best fit to the measured results.

2.3. IIR Filtering

The splitting of C_s into C_H and C_R on a periodic basis creates a first order IIR filter. Fig. 1 is now redrawn in Fig. 4 to better present the proposed technique. In order to understand this operation, we now focus on the event when the RF current has been integrated over N RF cycles and at this time, SA toggles its value causing C_R to rotate. Just before the rotation, the charge is being shared on both C_H and C_R capacitors proportional to their capacitance values. Let

$$a_1 = \frac{C_H}{C_H + C_R} \tag{5}$$

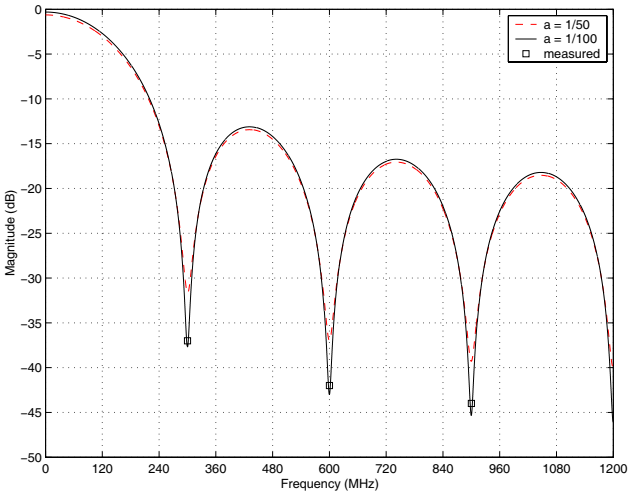

Fig. 3. Temporal MA operation at RF rate.

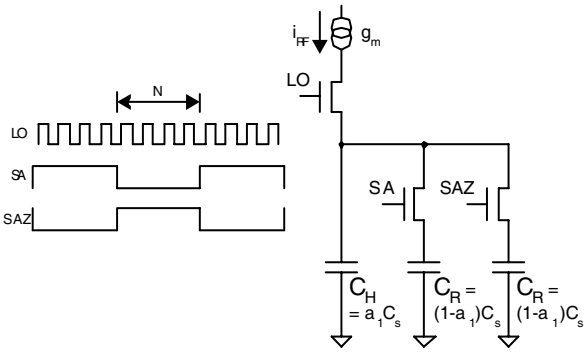

Fig. 4. IIR operation with cyclic charge readout.

Then, C_R stores $(1-a_1)$ factor of the total charge on C_s, while C_H stores the remaining a_1 factor of charge. Just as the other rotating capacitor joins the C_H capacitor in the RF sampling process and, at the same time, it obtains $\frac{1-a_1}{a_1+(1-a_1)} = 1-a_1$ of the total remaining charge in the "history" capacitor, provided it has no initial charge at the time of commutation. Thus the system retains a_1 portion of the total system charge of the previous cycle.

If the input charge accumulated over the most-recent N RF samples is w_j then the charge s_j stored in the system at sampling time j, where $i = N \cdot j$, (as stated earlier, i is the RF cycle index) could be described as a single-pole recursive IIR equation:

$$s_j = a_1 s_{j-1} + w_j \tag{6}$$

$$x_j = (1-a_1)s_{j-1} \tag{7}$$

The output charge x_j is $(1-a_1)$ of the system charge in the most-recent cycle. This discrete-time IIR filter operates at f_0/N sampling rate and introduces a single pole with the frequency attenuation of 20 dB/dec. The equivalent pole location in the continuous-time domain for $f_{c1} \ll f_0/N$ is

$$f_{c1} = \frac{1}{2\pi}\frac{f_0}{N} \cdot (1-a_1) = \frac{1}{2\pi}\frac{f_0}{N} \cdot \frac{C_R}{C_H + C_R} \tag{8}$$

Since there is no sampling time expansion for the IIR operation, the discrete signal processing charge gain is one. In other words, due to the charge conservation principle, the input charge per sample interval is on average the same as the output charge. For the voltage gain, however, there is an impedance transformation of $C_{input} = C_H$ and $C_{output} = (1-a_1)C_H$, thus resulting in a gain.

$$G_{q,iir1} = 1 \tag{9}$$

$$G_{v,iir1} = \frac{1}{1-a_1} = \frac{C_H + C_R}{C_R} \tag{10}$$

As an example, the IIR filtering with a single coefficient of a_1 = 0.9686, placing the pole at f_{c1} = 1.5 MHz, is performed at f_0/N = 2.4 GHz / 8 = 300 MHz sampling rate and it follows the FIR MA=8 filtering of the input at f_0 RF sampling rate. The voltage gain of the high-rate IIR filter is 31.85 (30.06 dB).

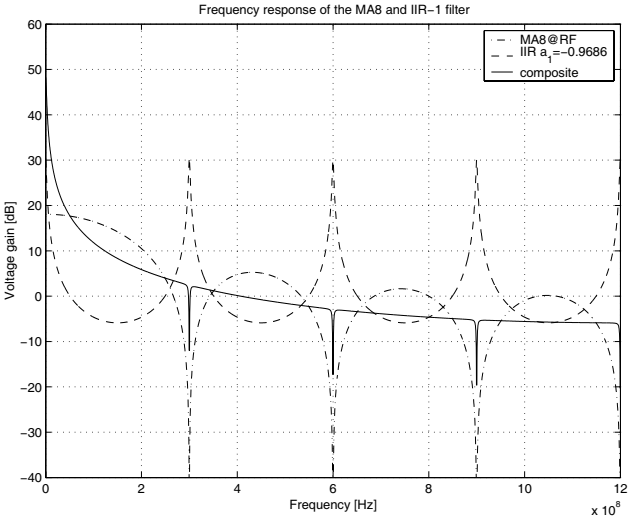

Fig. 5. Transfer function of the temporal moving average with a decimation of 8 and the IIR filter operating at RF/8 rate. The solid line is the composite transfer of both filters.

Fig. 5 shows frequency response of the temporal moving average with a decimation of 8 (G_v = 18.06 dB) and the IIR filter operating at RF/8 rate (G_v = 30.06 dB). The solid line is the composite transfer function with the DC gain of G_v = 48.12 dB. The first decimation of $N = 8$ reveals itself as aliasing. It should be noted that it is possible to avoid aliasing of a very strong interferer into the critical IF band by simply changing the decimation ratio N, as Fig. 2 suggests. This brings out advantages of integrating RF/analog with digital circuitry by opening new avenues of novel signal-processing solutions not possible before.

3. NOISE PERFORMANCE

The total noise power sampled onto C_s is equal to kT/C_s in a bandwidth determined by f_{LO} since the sampling takes place at the rate of LO. The second noise source comes into play when C_R is rotated. When the rotating capacitor is disconnected from C_H, it will sample kT/C_R noise due to the resistance of the switch that connects it to C_H. In general it is desirable to have $C_H \gg C_R$ in order to get a low-pass filter with good adjacent channel rejection. Hence, the switching of C_R dominates the noise behavior of the circuit shown in Fig. 1. The power of kT/C_R noise which falls into the signal of interest having a one-sided bandwidth B is equal

to

$$x^2_{n,rms} = \frac{kTB}{C_R f_s} \tag{11}$$

where $f_s = f_0/N$ is the sampling rate. Quite interestingly, one would recognize that a switched capacitor emulates a resistor with value $R_{eq} = 1/C_R f_s$ and that the noise in the signal bandwidth equals $kTB/C_R f_s = kTBR_{eq}$!

The above discussion shows that the noise contribution by the switched capacitor resistor is equivalent to the noise contributed by a continuous-time resistor which it emulates, provided that kT/C noise is flat. This however, is not the case and the noise contribution by the switched capacitor "resistor" is somewhat higher than the equivalent continuous-time resistor. However, switched capacitor resistor offers the advantage of excellent control of matching. It should also be noted that there is a sufficiently large signal processing gain before the C_R sampling, thus further minimizing this effect.

4. EXPERIMENTAL RESULTS

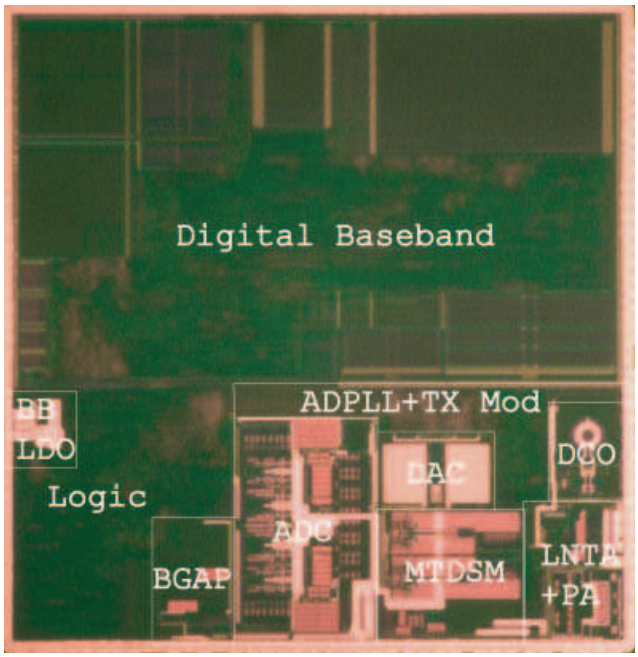

Fig. 6. Die micrograph of the single-chip Bluetooth radio.

The principles described in the previous sections were used to create a receiver structure addressing the Bluetooth specifications. The entire IC chip also included transmitter and baseband processor and was fabricated in a 130 nm digital CMOS process featuring copper interconnects, 1.5 V transistors, 0.35 μm minimum metal pitch, 2.9 nm gate oxide thickness and no extra processing steps. Fig. 6 shows a micrograph of the complete single-chip Bluetooth radio. The receiver front-end is located in the lower-right corner and consists of the LNTA, the described *multi-tap direct sampling mixer* (MTDSM), high-speed $\Sigma\Delta$ ADC and DAC. The discrete-time signal processing described in the previous sections has been verified through lab measurements. Table 1 shows the resulting performance of the radio in comparison to earlier published works using continuous-time architectures. It is interesting to notice that the proposed approach has been able to either match or surpass the performance of the other traditional solutions despite smaller voltage headroom. This indicates that discrete-time signal processing in the RF front-ends has now become feasible.

Table 1. Comparison to previous work.

Work	Technology	RX Current mA	Sensitivity dBm
This	0.13 μm, 1.575 V	37	-83
[1]	0.18 μm, 2.5$\tilde{3}$.0 V	30.5	-78
[2]	0.18 μm, 2.7 V	39	-83
[3]	0.25 μm, ? V	45	$\leq$-70
[4]	0.25 μm, 2.5 V	$<$ 50	-80

5. CONCLUSION

We have proposed and demonstrated a novel RF direct sampling technique that achieves great selectivity right at the mixer level. The dynamic range requirements of the following ADC are thus significantly relaxed. The selectivity is digitally controlled by the LO clock frequency and the capacitance ratio, both of which are extremely precise in digital deep-submicron CMOS processes. The clock jitter and the switching kT/C noise effects that are plaguing conventional subsampling mixer receivers could be overcome with low-noise oscillators and proper capacitor sizing. In order to validate the proposed technique, the direct sampling mixer has been fabricated as part of a commercial Bluetooth radio in a digital 130 nm CMOS process. This paper demonstrates feasibility and attractiveness of employing the charge-domain RF signal processing within a larger system-on-chip (SoC) designs.

6. REFERENCES

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