

Directed integration of ZnO nanobridge devices on a Si substrate

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We demonstrate the directed assembly and integration of ZnO nanobridges into working devices on silicon-on-insulator substrates. The “pick and place” method of nanowire integration is avoided and metal catalysts are not used. ZnO nanowires (NWs) were grown selectively via a vapor-solid method using a patterned ZnO thin-film seed layer that was deposited on Si trench sidewalls via atomic layer deposition. ZnO NWs grew to span the trench and self-terminate on the opposing surface, effectively forming electrically accessible horizontal ZnO nanobridge devices. Vertical bridge devices were also constructed using undercut islands. Directly grown horizontal ZnO nanobridge devices were operated as gas and UV sensors, demonstrating that this method represents a significant step towards practical large-scale integration of nanodevices into Si microelectronics. © 2005 American Institute of Physics. [DOI: 10.1063/1.2136218]

Due to its many unique properties, ZnO is an attractive material for nanowire-based electronics, UV photonics, and sensing applications.^{1–17} The sensing properties of ZnO and other metal oxides are known to be due to charge-exchange reactions with surface adsorbants.³ Because of their inherently large surface-to-volume ratio, nanostructured metal-oxide materials offer the promise of high sensitivity.^{3,18} In order to take full advantage of nanomaterials, however integration into Si-based microelectronics devices is necessary. Currently, the most widely used method of nanomaterial integration is the “pick and place” method, where the ZnO nanorods are “harvested” from a growth substrate, placed into solution, and then dispersed randomly onto the device substrate (with various modifications such as electric field and fluidic flow assisted alignment, etc.). Using this method, much excellent work has recently been performed describing the formation and testing of individual ZnO nanowire devices and their sensitivity to UV light, O₂, H₂O, ethanol, CO, NO₂, NH₃, etc.^{4–6,10–18} Unfortunately, with drawbacks such as random placement, contamination, and a general incompatibility with Si processing, the “pick and place” method is not considered to be suitable for large-scale manufacturing. We have therefore been exploring more practical methods of integrating nanomaterials into Si devices. A more elegant approach is to selectively grow nanostructures directly onto desired areas of a substrate.^{19–23} An even better technique would be to grow nanowires (NWs) from one desired location directly to another desired location, such as between two electrodes. The HP group was the first to use a semiconductor, successfully growing Si nanowires across a trench on a Si substrate.²⁴ Unfortunately the HP technique, along with almost all of the above selective growth techniques, suffers from a reliance on the use of metal catalysts such as Au or Ti to initiate and define vapor-liquid-solid (VLS) (Ref. 25) growth of nanostructures. As metal catalysts are generally difficult to subtractively pattern and can be a source of detrimental contamination, they are best avoided.

Recently, selective growth of ZnO nanorods on Si substrates has been achieved without the use of a metal catalyst.

Instead, a thin-film ZnO seed layer was used to define regions of selective vapor-solid (VS) growth.^{17,26} Using this seed layer technique, we demonstrate a repeatable method for directed assembly and integration of ZnO nanobridges (NBs) into working devices on silicon-on-insulator (SOI) substrates. Atomic layer deposition (ALD) was used to deposit a thin-film ZnO seed layer conformally onto the sidewalls of SOI trench structures and ceilings and floors of undercut SOI island structures. High-quality ZnO nanorods were then self-assembled on the patterned ZnO seed layer. Wire growth was observed to span the gaps to self-terminate on the opposing surface and effectively form vertical and horizontal ZnO NBs. Operation of the horizontal ZnO NB devices as gas and UV sensors was achieved, demonstrating the potential of this method for practical large-scale integration of nanodevices into Si microelectronics.

Construction of horizontal NBs began by forming Si islands on the SiO₂ buried oxide (BOX) layer of an SOI substrate [see Fig. 1(c)]. In order to form vertical NBs, the BOX

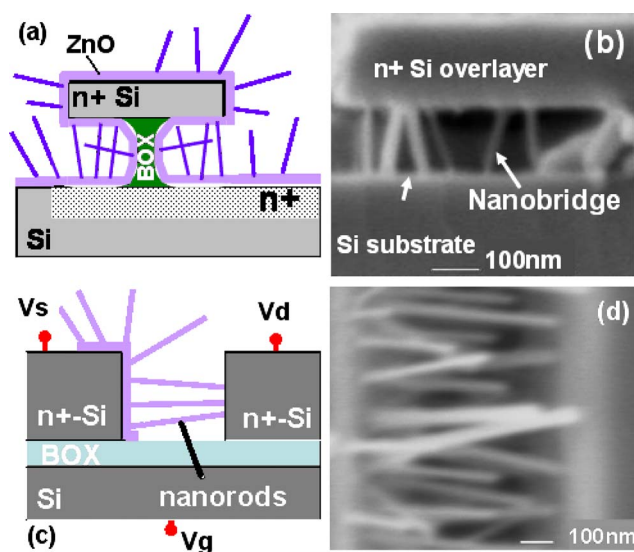


FIG. 1. (a) Schematic sketch and (b) cross-sectional SEM of vertical ZnO NBs spanning an undercut Si island. (c) Sketch and (d) top-view SEM of horizontal ZnO NBs spanning a trench structure.

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layer between the Si islands was dry etched down to the Si substrate, and then wet etched using HF to undercut the Si islands [see Fig. 1(a)]. Next, a highly conformal thin ZnO seed layer was deposited via ALD, using alternating pulses of diethylzinc (DEZ) precursor and H₂O vapor at a substrate temperature of approximately 170 °C (Ref. 27). In ALD, precursors are pulsed alternately into the deposition chamber and are separated by N₂ purges. Reactions take place on the substrate surface and are self-limiting, allowing for the excellent conformality and uniformity. As deposited ALD ZnO films were polycrystalline hexagonal wurtzite. Elevated temperature annealing increased the crystal size and the *c*-axis orientation of the films. After a photolithographic step and dry etch, ZnO was left coating only horizontal surfaces and areas under the Si islands. ZnO nanostructure growth was then performed in a 5-cm-diam quartz tube furnace by exposing substrates to Zn vapor at 800–915 °C for approximately 30 min with a flow of 30–80 sccm Ar and a trace amount of oxygen.¹⁷ Zn vapor is generated through carbothermal reduction of ZnO powder using equal parts of ZnO and graphite.² SEM images were taken using a JEOL Instruments 6400F.

ZnO nanostructures initiate selectively on ZnO thin-film seed regions and grow roughly perpendicular to the surface,¹⁷ with some rods spanning the gap to terminate on the opposing wall of an adjacent island, forming bridges. Shown in Fig. 1 are SEM images and cross-sectional sketches of self-assembled vertical (a,b) and horizontal (c,d) NB structures. For the case of the horizontal structure, ZnO was left only on one wall so NBs terminate on Si. For the undercut vertical structure, NBs terminate on ZnO. Although ZnO was not patterned for the vertical structure, it could easily have been etched to leave ZnO only in the undercut region. By virtue of the self-assembled connection between two terminals, NBs are automatically integrated into an electrically accessible device structure. Fairly high densities of NBs can be grown between the two terminals, allowing a large surface area of ZnO to be exposed to an ambient and creating the potential for high sensitivity. We have previously reported that NWs grown using this vapor-solid technique are of high quality with single-crystal structure, *c*-axis orientation, high-UV photoluminescence (PL), and undetectable defect-related visible PL¹⁷. NBs were 10–100 nm in diameter and spanned gaps of up to several microns.

As shown in Fig. 1(c), the horizontal bridge structure can be operated as a three-terminal device. I_{sd} - V_{sd} measurements before and after NB growth on a 0.8- μ m comb structure (inset) for V_g stepped from -5 to +3 V in 2-V increments are shown in Fig. 2. Prior to NB growth, leakage through the structure was below measurement sensitivity (Agilent 4156C using medium integration time) indicating that the BOX is very effective at isolating the terminals. After NB growth, a large current can be measured between the n^+ Si islands, demonstrating that the ZnO NBs make an electrical connection to both terminals. V_g is seen to have some gating effect on the ZnO channel (inset) of these non-optimized devices. The gate effect appears to be larger for longer bridge gaps and could likely be increased through optimization. As further evidence of conduction through the NBs, sweeping V_{sd} to breakdown resulted in a two orders of magnitude decrease in current rather than a short (not shown). Note that the I - V curves represent the ensemble behavior of many wires in parallel. It is obvious that contact

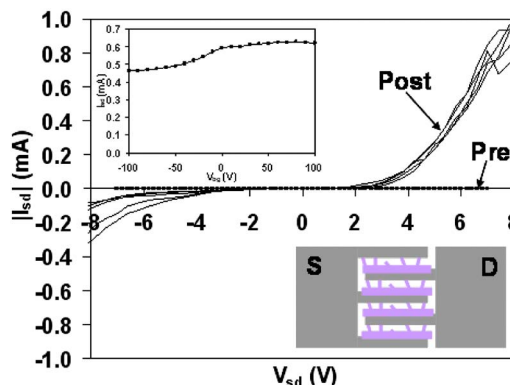


FIG. 2. Plot of I_{sd} vs V_{sd} for V_g stepped from -5 to 3 V in 2-V increments for a 0.8- μ m gap comb structure (top-view schematic shown in inset) (a) pre- and (b) post-ZnO NB growth. The inset shows plot of I_{sd} vs V_g for $V_{sd}=10$ V.

resistance, R_c , is poor. This is due primarily to the fact that measurements were made by probing directly on the Si pads without metallization. Metallization was not performed because of (a) the high temperatures used for NW growth, which made pregrowth metallization impossible and (b) the small sample size limit for NW growth in the 5-cm tube furnace, which made postgrowth conventional lithography impossible. To improve probe to pad R_c , we are currently investigating a low-temperature NW growth method that will allow full wafer processing and thus subsequent metallization. Another source of R_c lies at the termination points of the nanobridges. The difference in initiation on ZnO and termination on Si may also account for some of the asymmetry in the I - V . Due to the large probe to pad R_c , these effects are currently difficult to isolate.

ZnO is known to be sensitive to UV light, and UV illumination has been used to improve recovery time in metal-oxide sensors. Shown in Fig. 3 is a plot of I_{sd} versus time for a 0.8- μ m gap comb structure operated in air under fluorescent and/or natural lighting with $V_{sd}=10$ V and $V_g=0$ V. At $t \sim 64$ sec, the sample was exposed to the beam of a 375-nm UV pen light. The UV light resulted in an immediate greater than one order of magnitude increase in current to the mid- 10^{-3} -A range. In addition to band-to-band generation of carriers, it is thought that the large UV response is also due to rapid desorption of all surface species. As soon as the UV light was removed at $t=71$ sec, an extended recovery period (about 300 sec) begins in which the current slowly decreases back to pre-exposure value. The magnitude and period of the extended recovery was dependent on ambient and is likely

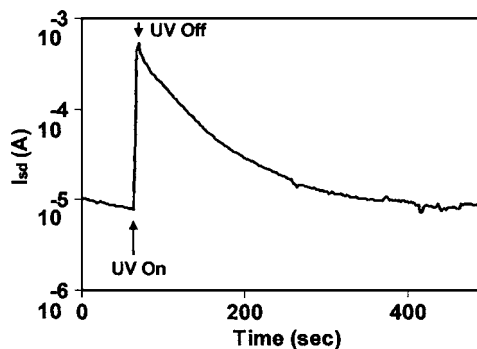


FIG. 3. Plot of current vs time for the 0.8- μ m comb device exposed to 375 nm UV light.

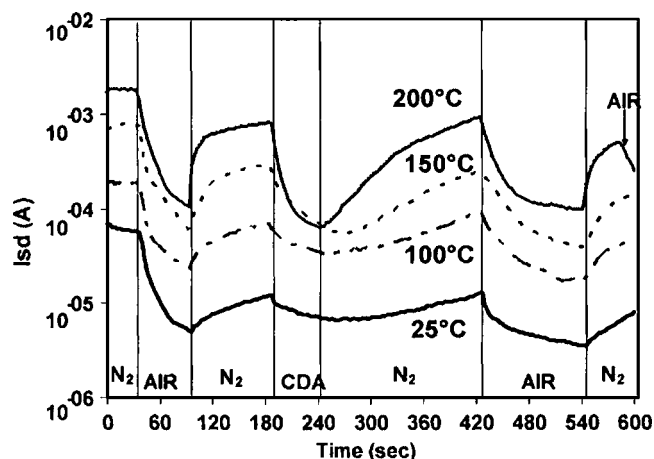


FIG. 4. I_{sd} vs time for a 0.6- μm comb structure operated with $V_{sd}=15$ V and $V_g=10$ V for exposures to N_2 , air, and CDA at 25, 100, 150, and 200 $^\circ\text{C}$.

due to the slow re-adsorption of surface species. The UV response under these nonideal experimental conditions is qualitatively consistent with reports for ZnO nanowire devices fabricated via the pick and place method.^{4,5,10,14}

Shown in Fig. 4 are plots of I_{sd} as a function of time for a 0.6- μm comb structure operated with the microscope lamp on, $V_{sd}=15$ V, and $V_g=10$ V for exposures to N_2 , air, and clean dry air (CDA) at 25, 100, 150, and 200 $^\circ\text{C}$. Ambient exposures were performed using a probe station. Focusing on the 25 $^\circ\text{C}$ trace, it is seen that ZnO NB devices are sensitive to ambient, even at room temperature. The response to either air or CDA exposure was qualitatively similar: a decrease in current. Subsequent exposure to N_2 resulted in partial to full recovery. In both cases, the mechanism for the current decrease (increase) is likely oxygen adsorption (desorption) to (from) the surface which is accompanied by a reduction (increase) in electron carrier concentration.^{4,16,10,14} Recovery from a CDA exposure appeared to be less rapid than recovery from an air exposure. One explanation for this difference is the moisture content in the air. Increasing the operating temperature resulted in a large increase in conductivity with I_{sd} increasing almost two orders of magnitude between 25 and 200 $^\circ\text{C}$. There is more than one component to this increase. Although there is likely some thermal generation of carriers, because the band gap is about 3.3 eV, this is not dominant. The main component is desorption of surface species such as O^- which results in a large increase in conductivity by freeing up electrons to contribute to conduction. Conductivity was observed to remain at elevated levels when devices were cooled down in N_2 . Increased operation temperature resulted in improved recovery times. The steepness of the conductivity recovery slope after air or CDA exposure increases as the temperature is increased from 25 to 200 $^\circ\text{C}$. This improvement was expected. Metal-oxide sensors are often operated at elevated temperatures due to the improved sensitivity and recovery brought about by enhanced redox reactions at the surface. Response times will also likely depend on partial pressures and electron concentration in the wire which can be controlled¹⁶ by the back gate. Finally, though not shown, the NB devices also showed sensitivity to moisture (breath) and isopropyl alcohol, manifested as a

rapid increase in conductivity at room temperature and consistent with previous reports.

We have achieved directed assembly and integration of working ZnO nanobridge UV and gas sensor devices onto Si wafers. Directed assembly refers to the use of top-down techniques to pattern the forces (in this case a ZnO seed layer) that guide bottom-up growth.⁷ By integration, it is meant that in addition to selective growth of NWs in desired locations, NWs are also electrically connected to other desired locations to form a working device. Although several recent studies have demonstrated the sensitivity of single ZnO NW devices to O_2 , H_2O , ethanol, CO, NO_2 , NH_3 , etc.,^{4-6,10-18} these devices were fabricated via "pick and place," a method not suitable for large-scale integration. The fact that our direct-grown nanobridge structures can be operated as gas and UV sensors demonstrates the potential of the technique and represents a significant step towards practical large-scale integration of high-quality nanostructures into Si complementary metal-oxide semiconductor (CMOS) compatible microelectronics process flows.

- ¹M. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, *Science* **292**, 1897 (2001).
- ²P. Yang, H. Yan, S. Mao, R. Russo, J. Johnson, R. Saykally, N. Morris, J. Pham, R. He, and H. J. Choi, *Adv. Funct. Mater.* **12**, 323 (2002).
- ³Y. W. Heo, L. C. Tien, DB. S. Kang, R. Ren, B. P. Gila, and S. J. Pearton, *Appl. Phys. Lett.* **85**, 2002 (2004).
- ⁴H. Kind, H. Yan, B. Messer, M. Law, and P. Yang, *Adv. Mater. (Weinheim, Ger.)* **14**, 158 (2002).
- ⁵M. S. Arnold, P. Avouris, Z. W. Pan, and Z. L. Wang, *J. Phys. Chem. B* **107**, 659 (2003).
- ⁶A. Kolmakov and M. Moskovits, *Annu. Rev. Mater. Res.* **34**, 151 (2004).
- ⁷M. Law, J. Goldberger, and P. Yang, *Annu. Rev. Mater. Res.* **34**, 83 (2004).
- ⁸Y. Xia, P. Yang, Y. Sun, Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim, and H. Yan, *Adv. Mater. (Weinheim, Ger.)* **15**, 353 (2003).
- ⁹R. Konenkamp, R. C. Word, and C. Schlegel, *Appl. Phys. Lett.* **85**, 6004 (2004).
- ¹⁰Q. H. Li, T. Gao, Y. G. Wang, and T. H. Wang, *Appl. Phys. Lett.* **86**, 123117 (2005).
- ¹¹Y. Zhang, K. Yu, D. Jiang, Z. Zhu, H. Geng, and L. Luo, *Appl. Surf. Sci.* **242**, 212 (2005).
- ¹²Q. Wan, H. Li, Y. J. Chen, T. H. Wang, X. L. He, J. P. Li, and C. L. Lin, *Appl. Phys. Lett.* **84**, 3654 (2004).
- ¹³W. I. Park, J. S. Kim, G. C. Yi, M. H. Bae, and H. J. Lee, *Appl. Phys. Lett.* **85**, 5052 (2004).
- ¹⁴Q. H. Li, Q. Wan, Y. X. Liang, and T. H. Wang, *Appl. Phys. Lett.* **84**, 4556 (2004).
- ¹⁵Z. Fan and J. G. Lu, *Appl. Phys. Lett.* **86**, 123510 (2005).
- ¹⁶Z. Fan, D. Wang, P. C. Chang, W. Y. Tseng, and J. G. Lu, *Appl. Phys. Lett.* **85**, 5923 (2004).
- ¹⁷J. F. Conley, Jr., L. Stecker, and Y. Ono, *Nanotechnology* **16**, 292 (2005).
- ¹⁸C. Yu, Q. Hao, S. Saha, L. Shi, X. Kong, and Z. L. Wang, *Appl. Phys. Lett.* **86**, 063101 (2005).
- ¹⁹H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, *Nano Lett.* **4**, 1247 (2004).
- ²⁰Y. W. Heo, L. C. Tien, DB. S. Kang, R. Ren, B. P. Gila, and S. J. Pearton, *Appl. Phys. Lett.* **85**, 2002 (2004).
- ²¹C. M. Lieber, *Mater. Res. Bull.* **28**, 486 (2003).
- ²²S. Y. Li, P. Lin, C. Y. Lee, and T. Y. Tseng, *J. Appl. Phys.* **95**, 3711 (2004).
- ²³H. Chik, J. Liang, S. G. Cloutier, N. Kouklin, and J. M. Xu, *Appl. Phys. Lett.* **84**, 3376 (2004).
- ²⁴M. S. Islam, S. Sharma, T. I. Kamins, and R. S. Williams, *Nanotechnology* **15**, L5 (2004).
- ²⁵R. S. Wagner and W. C. Ellis, *Appl. Phys. Lett.* **4**, 89 (1964).
- ²⁶J. Jie, Guanzhong W. Y. Chen, X. Han, Q. Wang, B. Xu, and J. G. Hou, *Appl. Phys. Lett.* **86**, 031909 (2005).
- ²⁷J. M. Jensen, A. B. Oelkers, R. Toivola, D. C. Johnson, J. W. Elam, and S. M. George, *Chem. Mater.* **14**, 2276 (2002).