Discrete-Time Queuing Analysis of Dual-Plane ATM Switch with Synchronous Connection Control

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CONTENTS

ABSTRACT

In this paper, we propose an ATM switch with the rate more than gigabits per second to cope with future broadband service environments. The basic idea is to separate the connection control flow from the data information flow inside the switch. The proposed switch has a dual-plane switch matrix with the synchronous control algorithm. The queuing behaviors of the proposed switch are shown by the discrete-time queuing analysis. Numerical analyses are taken both in the non-blocking crossbar switch and the banyan switch with internal blocking. Results show that a proposed dual-plane 16x16 switch would have the acceptable performance with maximum throughput of about 95 percent.

I. INTRODUCTION

To meet the forthcoming high rate communication needs, the broadband switching systems are expected to provide the switching capability more than several gigabits per second. Each port might connect to transmission equipments with synchronous digital hierarchy more than 2.488 Gb/s. In this case, *real-time* switching capability (that is, cell-by-cell switching) would be required for ATM cells with rate more than several gigabit per second. In a non-real time switching, ATM signals may be controlled by the network management [1].

Until now, ATM switch architectures have been widely investigated and proven to be acceptable for cell-by-cell switching with the rate of 155 Mb/s [2]-[7]. It indicates that the output queuing scheme is superior to the input queuing one from the viewpoint of throughput performance. However, the input queuing scheme is much flexible for connection and traffic control of ATM cells. In addition, the routing path based on virtual path identifier (VPI)/virtual channel identifier (VCI) should be given prior to the execution of switching operation regardless of whether the switch is self-routing or not. To support high-speed switching requirements, we consider the switch architectural flexibility and the control independence as the following issues:

- switching rate versus control rate;
- support of combinatorial capabilities of information flow such as copying, sorting, masking, and grouping;
- synchronous control versus asynchronous control.

As one approach to meet the high speed switching requirements, we propose a dual-plane ATM switch with synchronous control as shown in Fig. 1. The dual-plane switching architecture intends to support a flexible service requirements as well as to increase throughput performance. The switching fabric operates in fixed cycles with synchronous routing algorithm.

In the next section, we briefly discuss some design issues such as optical interface, buffering, and traffic control. In the following section, we describe the dual-plane switch architecture and present a discrete-time queuing analysis to evaluate the performance of a proposed dual-plane switch. Lastly, performance results are presented in Section V.

II. DESIGN CONSIDERATIONS OF GIGABIT ATM SWITCH

The design requirements of broadband ATM switch can be considered from three views: user, network operator, and system designer. The user may request various QoS (quality-of-service) levels with a value of bit rate, loss, delay, and priority, etc. The user may also request various connection types

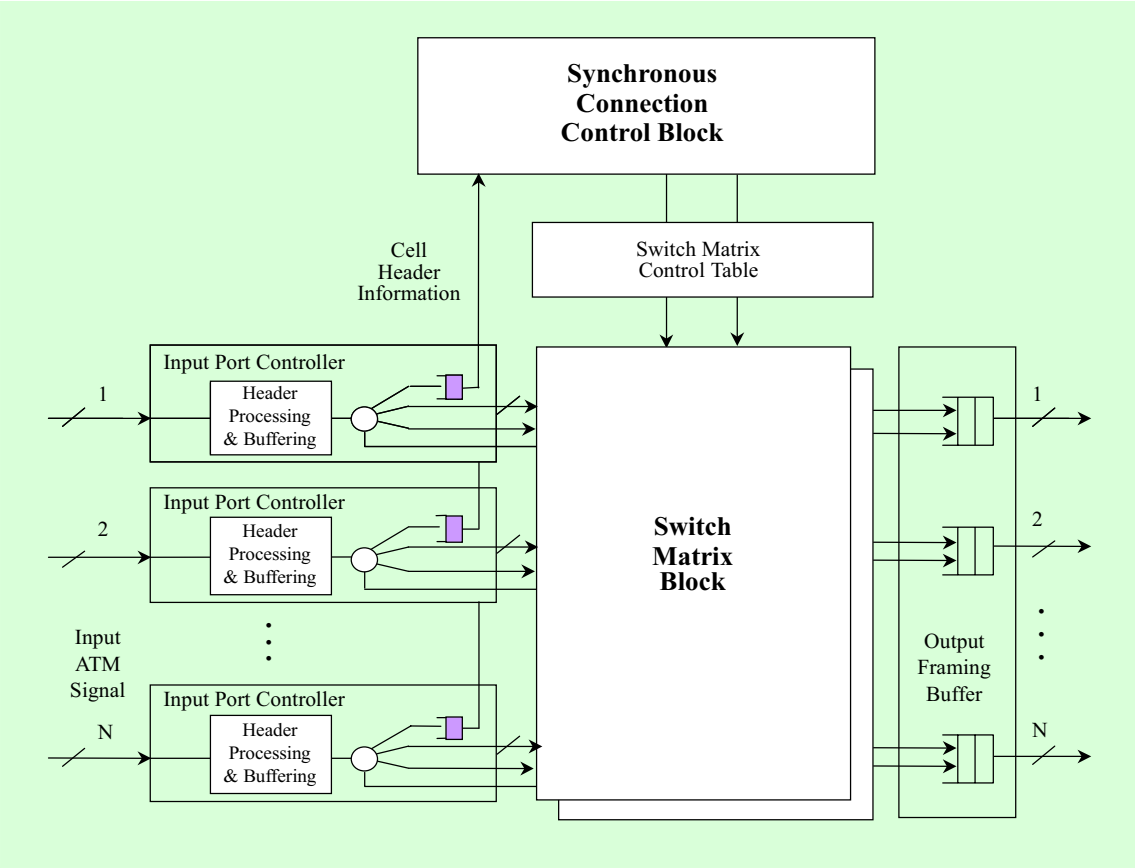

Fig. 1. Dual-plane ATM switch architecture.

including point-to-multi-point, and broadcast connections. The network operator may address various steps of network management by means of bandwidth control, traffic control, reconfiguration, and fault control, etc. From the viewpoint of system designer, the broadband ATM switch would provide the relevant switching latency for constant bit rate (CBR)/variable bit rate (VBR) traffic. It also provides the switch control capabilities such as rerouting, bypass, reconfiguration, access control and flow rate control. It means that the ATM switch shouldn't be designed only for switching performance, but also for service environments coming from the user and network operator.

Two design issues of gigabit switching may be focused in the ATM environment: optical interface, and buffering location. Most of all, the gigabit ATM switch should have good adaptation with the optical transmission equipments to reduce unnecessary processing burden. The operation, administration, and maintenance (OAM)

functions of the ATM switch should mutually help those of transmission equipments while the transmission equipment has an intelligence with virtual path concept. For example, end-to-end bandwidth of ATM virtual channel should sustain both in ATM switch and transmission equipments.Thus in the gigabit ATM service environment, switching relates closely to transmission.

There is a trade-off between input buffering and output buffering in the viewpoints of performance, service flexibility, and controllability, etc. It has been indicated that switch with output buffering has a good throughput performance and is useful for multiple bus architectures [4], [5]. On the other hand, the throughput of switch with input buffering reaches saturation at 58.6 %. However, there are considerations other than throughput performance mentioned above. For ATM header processing and traffic control, the output buffering scheme has less flexibility than input one since the ATM cell requires the appropriate control to traverse the switch before it arrives at the output buffer. The additional processing capability may be inevitable at the input side. It has been shown that the flow control procedure should be based on the source-to-destination pairs to preserve the QoS requirements. The assumption is that the gigabit ATM switch requires much simple approach for traffic and congestion control with considerations of device technology.

III. DESCRIPTION OF SWITCHING ARCHITECTURE AND OPERATIONS

1. Overall Architecture

To meet the above ATM switching requirements, we propose a dual-plane ATM switch with synchronous control. Figure 1 shows the overall switch architecture. The dual-plane switching architecture intends to provide a redundant connection path for service flexibility as well as to increase the switch throughput. The cells are stored in the input buffers. The header processing path separates from the information flow path at the input port controller. The cell header decodes at the synchronous routing block to find an appropriate switching path. When the cells cannot find a connection path on the primary switching plane, they try the secondary plane. The results of switching algorithm will set the switch matrix control table for the next switching cycle. The switching fabric operates in fixed-duration synchronous cycles equal to the cell transfer time. The cell will traverse the dual-plane switching matrix in two cell cycles: one for the routing decision and the other for switching.

By separating the synchronous routing control path from the data switching path, the proposed switch architecture can provide path-level switching capability as well as cell-level switching. During the path setup, the connection control logic does not

need to update the switch matrix control block. The corresponding connection path in the switch matrix has no change. It means that the path-level control as well as synchronous connection control is good for the high speed switching. The synchronous connection control block consists of a number of combinatorial logics depending on the type of switch matrix and connection algorithm. The cell sequences are logically aligned based on the destination according to service type, control level, and priority class. The cell header is decoded to set up the connection path between source and destination ports. The switch matrix block has a dual-plane architecture. There are two output frame buffers, that is, one buffer per plane. The output framing block is for the output transmission synchronization.

2. Switching Operations

The switch network synchronously operates by the fixed cell cycle. The cell cycle has the same duration as the cell transmission time. In Fig. 2, we show the timing diagram for cell switching. In this figure, one can show the pipe-lining effect of synchronous connection control algorithm, which has two cell cycles: one cell cycle is for routing decision and the other is for switching. The routing decision results update the switch matrix control table. These tables are updated for every cell cycle. If it uses path-level switching, this table would change only at the starting and the ending points of path request.

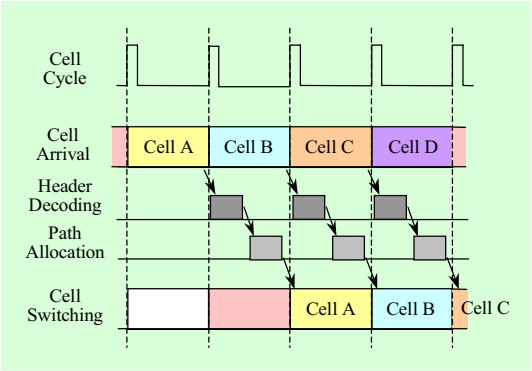

Fig. 2. Timing diagram for cell switching.

The synchronous connection control algorithm depends on the type of switch matrix with consideration of service class, control-level, and priority. The path-level control is sometimes useful since it can reduce the processing burden. To cope with the internal contention, the connection control logic takes an appropriate control before a cell collides.

IV. PERFORMANCE ANALYSIS

In order to evaluate the performance characteristics of a proposed dual-plane switch architecture, we assume the point-to-point virtual channel with the same priority. The connection paths are statistically assigned for the cell-based demand. The primary plane is first assigned to provide the connection paths and the secondary

plane is served for the cells which cannot get the connection path in the primary plane. When the cell cannot find the proper connection path in the dual-plane, it waits for the next cell cycle. In the output framing block, one cell can be sent during a cell cycle time. Here, the cell sequence is preserved at the connection control logic in which the cells are logically aligned based on the destination. The connection control logic cyclically scans the destination ports and allocates the proper connection path for the head-of-line (HOL) of the cells to the same destination, regardless of whether it is in HOL of each input buffer or not.

For a proposed dual-plane switch, we consider two types of switch matrices according to the number of cells that can be sent from one input port during a cell cycle. In the basic switch architecture, only one cell from one input port can traverse the switch during a cell cycle regardless of dual-plane operation. We name this architecture as *single-input dual-plane* (SIDP) switch. In the extended switch architecture, an input can transmit one cell on each plane during a cell cycle and thus we call it *dual-input dual-plane* (DIDP) switch. The DIDP switch could access two cells from an input port so that it maximizes the throughput of the output port. The difference between SIDP and DIDP switches is whether two cells from an input port could be accessed during a cell cycle. It should be noted that each output port can get two cells during one cell cycle regardless of switch type.

As the input traffic model, we assume the Bernoulli cell arrivals with the uniform destination distribution. As the type of switch matrix, we consider the crossbar switch as a non-blocking switch and the banyan switch as a blocking switch, respectively, with infinite input buffer.

In our analysis, we study the virtual input queuing behaviors toward a tagged output port by a discrete-time queue analysis. It should be noted that we focus the input queuing behaviors of the cells from different input ports destined to a specific output port (called the "tagged" output port.) We name the buffer for the cells destined to the tagged output as the "virtual" input buffer. Figure 3 shows the virtual input buffering algorithm for the single plane 4×4 switch. In the virtual input buffering algorithm, the synchronous connection control block logically aligns the cells of the real input buffer and assigns the connection path for the HOL cells of each virtual input buffer 1.

The connection control algorithm can avoid the same destination contention problem since it scans the virtual input queue based on the destination. However, internal blocking exists in the proposed dual-plane crossbar switch. It occurs when more than two virtual HOL cells are from the same input port within a cell cycle. We call this "same input contention." Figure 3 shows an example of internal blocking, in which the HOL cells of virtual input buffers 2 and 4 are from the same input port 4. In the

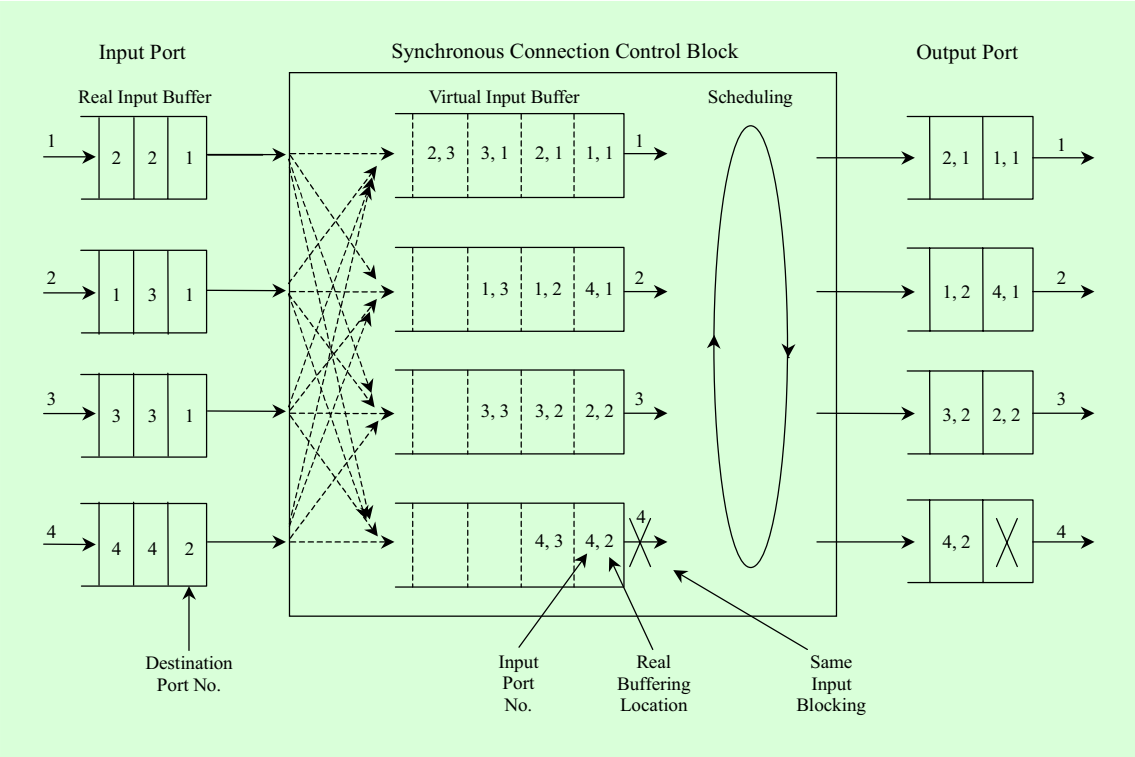

Fig. 3. Destination scheduling algorithm on connection control block.

algorithm of virtual input buffer, the cells could be randomly accessed from a real input buffer, not in the first come first service. But, it guarantees the cell sequence integrity since it functions the destination-oriented scheduling algorithm. The implementation of virtual input buffer could be easily implemented by using the content addressable memory.

Let's define the internal blocking probabilities of the primary plane and the secondary plane to be the probabilities that a cell toward the tagged destination is blocked in a given plane during a cell cycle time. We denote these by P_{b1} and P_{b2}, respectively. Now, we analyze the virtual input queuing behaviors toward the tagged output port. For the two-dimensional state variable $(i,\ j)$, i and j denote the virtual input queuing length and the tagged output queuing length at the beginning of n-th cell cycle time, respectively. The state transition relations between n-th and $(n+1)$-th states are given by :

$$(0,\ j) \rightarrow (a_n,\ 0) \quad \text{for } i = 0,\ 1$$

$$(1,\ j) \rightarrow \begin{cases} (a_n,\ 1) \text{ for } j = 0,\ 1 \text{ with Prob.}(1 - P_{b1}P_{b_2}) \\ (a_n + 1,\ 0) \text{ for } j = 0,\ 1 \text{ with Prob.}P_{b1}P_{b2} \end{cases}$$

$$(i,\ j) \rightarrow \begin{cases} (i-2+a_n,\ 2) \text{ for } i \geq 2,\ j=0,\ 1 \\ \qquad \text{with Prob.} \overline{P}_{b1}\overline{P}_{b2} \\ (i-1+a_n,\ 1) \text{ for } i \geq 2,\ j=0,\ 1 \\ \qquad \text{with Prob.} (\overline{P}_{b1}P_{b2}+P_{b1}\overline{P}_{b2}) \\ (i+a_n,\ 0) \text{ for } i \geq 2,\ j=0,\ 1 \\ \qquad \text{with Prob.} P_{b1}P_{b2} \end{cases}$$

$$(0,\ 2) \rightarrow (a_n,\ 1)$$

$$(i,\ 2) \rightarrow \begin{cases} (i-1+a_n,\ 2) \text{ for } i \geq 1 \\ \qquad \text{with Prob.} (1-P_{b1}P_{b2}) \\ (i+a_n,\ 1) \text{ for } i \geq 1 \\ \qquad \text{with Prob.} P_{b1}P_{b2}\ , \end{cases} \tag{1}$$

where the probability a_n is the random variable representing the number of cell arrivals destined to the tagged output during the n-th cell cycle, $\overline{P}_{b1} = 1 - P_{b1}$ and $\overline{P}_{b2} = 1 - P_{b2}$. In order to reduce this two-dimensional state transition diagram into a simple form, we assume that the state of the output buffer is an independent identically distributed sequence of random variables which are also independent of the input virtual queue. We now analyze the relations for the virtual input queuing behaviors and the output queuing behaviors toward the tagged output port. We define the virtual input queue length at the beginning of the n-th cell cycle time by q_n, and the tagged output queue length at the same cell cycle by d_n, where $0 \leq d_n \leq 2$ for two output framing buffers. The following relations hold:

$$q_{n+1} = (q_n - \alpha_n)^+ + a_n = q_n - \alpha_n^* + a_n \tag{2}$$

$$d_{n+1} = (d_n - \alpha_n)^+ + \alpha_n^*\ , \tag{3}$$

where the superscript + denotes the operator for non-negative value, α_n is the maximum number of cells which can be switched in the n-th cycle, and α_n^* is the randon variable for the actual number of cells which traverse the switch matrix during the same cycle time. These are given by

$$\alpha_n = \begin{cases} 2 \text{ for Prob.} P_{b1}P_{b2}P[d_n \leq 1] \\ 1 \text{ for} \begin{cases} \text{Prob.} (\overline{P}_{b1}+P_{b1}\overline{P}_{b2})P[d_n = 2] \text{ or} \\ \text{Prob.} (\overline{P}_{b1}P_{b2}+P_{b1}\overline{P}_{b2})P[d_n \leq 1] \end{cases} \\ 0 \text{ for Prob.} P_{b1}P_{b2} \end{cases} \tag{4}$$

$$\alpha_n^* = \begin{cases} 2 \text{ for Prob.} \overline{P}_{b1}\overline{P}_{b2}P[q_n \geq 2]P[d_n \leq 1] \\ 1 \text{ for} \begin{cases} \text{Prob.} (1-P_{b1}P_{b2})P[q_n = 1] \text{ or} \\ \text{Prob.} (\overline{P}_{b1}+P_{b1}\overline{P}_{b2})P[q_n \geq 2]P[d_n = 2] \text{ or} \\ \text{Prob.} (\overline{P}_{b1}P_{b2}+P_{b1}\overline{P}_{b2})P[q_n \geq 2]P[d_n \leq 1] \end{cases} \\ 0 \text{ for Prob.} P[q_n = 0] \text{or Prob.} P_{b1}P_{b2}P[q_n \geq 1] \end{cases} \tag{5}$$

The discrete time queue in (2) was considered in [8], and in the steady state, the virtual input queuing distribution for the tagged destination is found to be :

$$Q(z) = \frac{\begin{array}{l} P_0\big((1-P_{b1}P_{b2}) - ((1-P_{b1}P_{b2}) \\ \quad -(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2})z^{-1} \\ \quad -(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}z^{-2}\big) \\ +p_1(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}(1-z^{-1}) \end{array}}{\begin{array}{l} 1-\big(P_{b1}P_{b2} + ((1-P_{b1}P_{b2}) \\ \quad -(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2})z^{-1} \\ \quad +(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}z^{-2}\big)G_a(z) \end{array}} G_a(z) \tag{6}$$

where $Q(z)$ and $G_a(z)$ are the moment generating functions of the random variables q_n

and a_n, respectively. For the binomial arrival, $G_a(z) = \left(1 - \frac{\rho_i}{N} + \frac{\rho_i}{N} z\right)^N$, where ρ_i is the offered load of virtual input channel toward the tagged output and N is the number of input channels.

In (6), P_{b1} and P_{b2} are determined by the switch fabric and the traffic load; the parameters p_0, p_1, and δ_2 are interrelated as discussed below. In (6), the steady state probabilities p_0 and p_1 can be obtained by Rouche's theorem, where $p_k = \lim_{n\to\infty} P[q_n = k]$ for k =0, 1. Also, δ_2 is the probability $\lim_{n\to\infty} P[d_n = 2]$ in the steady state. From the relation of (3), it can be shown that

$$\delta_2 = \frac{\eta_2}{\eta_0 + \eta_2}$$

$$= \frac{2 + \frac{p_0 + (1-p_0)P_{b1}P_{b2}}{(1-p_0-p_1)\overline{P}_{b1}\overline{P}_{b2}} - \sqrt{\left(2 + \frac{p_0 + (1-p_0)P_{b1}P_{b2}}{1-p_0-p_1)\overline{P}_{b1}\overline{P}_{b2}}\right)^2 - 4}}{2} \quad (7)$$

where $\eta_k = \lim_{n\to\infty} P[\alpha_n^* = k]$ for k=0, 2 , are found for (3) to be given by :

$$\eta_0 = p_0 + (1-p_0)P_{b1}P_{b2} , \quad (4)$$

$$\eta_2 = (1-\delta_2)(1-p_0-p_1)\overline{P}_{b1}\overline{P}_{b2} , \quad (5)$$

The steady state queuing behavior $Q(z)$ can be calculated with the given internal blocking probabilities, P_{b1} and P_{b2}. The mean queue length, $\overline{q}$, is given by

$$\overline{q} = \left.\frac{\partial Q(z)}{\partial z}\right|_{z=1}$$

$$= \left\{ \begin{array}{l} \dfrac{\begin{array}{l} p_0\big((1-P_{b1}P_{b2} + (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2})g_1 \\ -(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}\big) + p_1(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}g_1 \end{array}}{1 - P_{b1}P_{b2} + (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2} - g_1} \\ + \left(\begin{array}{c} (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2} + (P_{b1}P_{b2} \\ -(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2})g_1 + g_2 \\ \hline (1 - P_{b1}P_{b2} + (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2} - g_1)^2 \\ \cdot\big(p_0(1 - P_{b1}P_{b2} + (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}) \\ + p_1(1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}\big) \end{array} \right) \end{array} \right. \quad (10)$$

where g_1 and g_2 are the first and second moments of $G_a(z)$ at $z = 1$, respectively. Note that when the system is saturated (i.e., $q_0 \to 0$) and $P_{b1} = P_{b2} = 0$, then $\overline{q}$ has the same form with that of M/D/1 system in the continuous-time domain as

$$\overline{q} = \rho_i + \frac{N-1}{N} \cdot \frac{\rho_i^2}{2(1-\rho_i)}. \quad (11)$$

In (10), when the system is saturated, the maximum input offered load, $\rho_{\max}$, can be found by setting the denominator to zero :

$$\rho_{\max} = 1 - P_{b1}P_{b2} + (1-\delta_2)\overline{P}_{b1}\overline{P}_{b2}$$

$$= 1 - P_{b1}P_{b2} + \frac{\sqrt{P_{b1}^2P_{b2}^2 + 4P_{b1}\overline{P}_{b1}P_{b2}\overline{P}_{b2}} - P_{b1}P_{b2}}{2}. \quad (12)$$

The queuing behaviors for the single-plane switch can be obtained by assigning P_{b2} being one in (6). In this case, the maximum input offered load is represented by $1 - P_{b1}$, which can be obtained by discrete Markov chain model, and is 0.586 for space-division switch with input queuing as in [2].

Now, we analyze the internal blocking probabilities for dual-plane crossbar and

multi-stage banyan switch. Note that the internal blocking probabilities are dependent on input traffic activities, their distributions, and switching matrix topology.

Case A) Dual-Plane Crossbar Switch Matrix

In a proposed dual-plane crossbar switch, there exists the internal blocking due to the same input contention as explained above. In order to calculate the internal blocking probabilities, P_{b1} and P_{b2}, for the SIDP and DIDP switches, we utilize the discrete Markov chain model proposed by Bhandarkar [9]. For the DIDP switch architecture, we extend the enumeration mesh of discrete Markov chain model for computing the transition probabilities (refer to Fig. 5 in [9]). We generate the enumeration meshes for the secondary plane from the final terminal states of the enumeration mesh for the primary plane. The same algorithm for evaluating the transition matrix is also applied to the enumeration mesh for the secondary plane. Here, the average number of busy input ports for the secondary-plane is dependent on the states of busy input ports of the primary plane. Internal blocking probabilities P_{b1} and P_{b2} for each plane are then calculated in the form of $1-\dfrac{\text{average number of busy input ports}}{\text{offered load}}$. For the SIDP switch, the secondary enumeration mesh is generated by the same rule except that the number of assigned input ports is less than or equal to that in the DIDP switch. In SIDP switch, the HOL cells assigned for the secondary plane can not be served when their input ports are already occupied by the primary plane at the same cell cycle. In the Appendix, we show the calculation procedure of internal blocking probabilities for the 4×4 SIDP and DIDP switches.

To obtain these internal blocking probabilities in the closed form, we try to get the approximation solution [9]. We assume that the state of the system is independent of the state during the last cycle. Then, the internal blocking probabilities in the steady state are represented by

$$P_{b1} = 1 - \frac{\rho_{i1}^*}{\rho_{i1}}, \tag{13}$$

$$P_{b2} = 1 - \frac{\rho_{i2}^*}{\rho_{i2}}, \tag{14}$$

where ρ_{i1} and ρ_{i2} are the offered loads for the primary plane and the secondary plane, respectively. ρ_{i1}^* and ρ_{i2}^* are the probabilities that the primary plane and the secondary plane are busy at a cell cycle, respectively. Here, ρ_{i1}^* and ρ_{i2}^* are given by

$$\rho_{i1}^* = 1 - \left(1 - \frac{\rho_{i1}}{N}\right)^N, \tag{15}$$

$$\rho_{i2}^* = \begin{cases} 1 - \left(1 - \dfrac{\rho_{i1}}{N}\right)^{P_{b1}N} & \text{for SIDP switch} \\ 1 - \left(1 - \dfrac{\rho_{i1}}{N}\right)^{N} & \text{for DIDP switch} \end{cases} \tag{16}$$

and ρ_{i2} is given by $(1-P_{b1})(1-P_0-P_1)$.

Case B) Dual-Plane Multistage Banyan Switch

In the dual-plane multi-stage banyan network, there exists the contention for occupying the same connection path between

stages inside the switch. This kind of contention has the same case as the same input contention problem in the crossbar switch. Thus, the internal blocking probabilities for multi-stage banyan switch can be obtained by recursively applying the algorithm for the crossbar switch as explained above. The internal blocking probabilities for each stage can be calculated by using the algorithm of case A by replacing the size of switch box. The average number of busy input ports at the first stage is used for the number of assigned input ports in the next stage.

Now, let's denote the internal blocking probabilities at the i-th stage by $P_{b1,\,i}$ and $P_{b2,\,i}$ for each plane. Then, the internal blocking probabilities are given by

$$P_{b1} = 1 - \prod_{i=1}^{n} (1 - P_{b1,\,i}), \tag{17}$$

$$P_{b2} = 1 - \prod_{i=1}^{n} (1 - P_{b2,\,i}), \tag{18}$$

where $n = \log_k N$ and k is the size of single switch box in each stage.

V. PERFORMANCE RESULTS

In Table 1(a), we show maximum throughput of the dual-plane switch for the uniform traffic for a crossbar network and a banyan network with 2×2 switching element. The discrete-time analysis results are compared to the simulation results. In SIDP crossbar and banyan switches, maximum throughput increases about 5∼10 % over those of the single-plane switch analyzed in [2]. Maximum throughput are greater than 95 % in the DIDP crossbar switch and greater than 80 % in the DIDP banyan switch. Thus the DIDP switch can provide a big increase in the achievable maximum throughput which is very close to that of the output buffering scheme. These above improvements are better than those obtained by increasing the window size in [3] and are comparable with those of the deluxe model in [7].

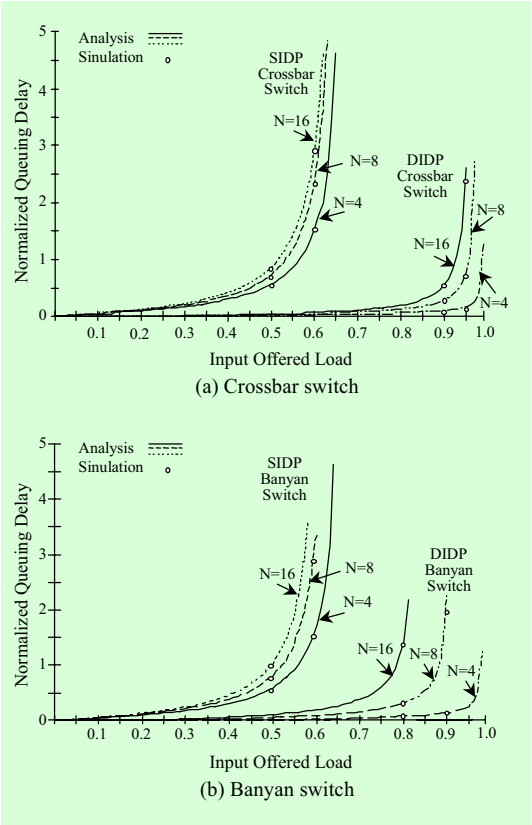

Fig. 4. Delay behavior of the dual-plane switch for uniform traffic: (a) crossbar switch, (b) banyan switch.

Table 2. Maximum throughput for the dual-plane switch.

(a) Uniform traffic.

Dimension	Output-Scheduled Banyan Network with Input Buffering		Output-Scheduled Crossbar Network with Input Buffering	
	Analysis	Simulation	Analysis	Simulation
	Single-Input Dual-Plane		Single-Input Dual-Plane	
N=4	72.80 %	71.90 %	73.90 %	72.40 %
N=8	69.30 %	68.20 %	70.80 %	69.20 %
N=16	66.60 %	65.70 %	69.40 %	67.30 %
N=64	62.50 %	61.90 %	67.80 %	65.10 %
	Dual-Input Dual-Plane		Dual-Input Dual-Plane	
N=4	97.50 %	99.20 %	99.60 %	99.50 %
N=8	93.30 %	94.70 %	97.70 %	98.10 %
N=16	87.70 %	88.90 %	95.60 %	96.50 %
N=64	78.00 %	78.70 %	94.20 %	94.70 %

(b) Non-uniform traffic with preference of the even outputs.

Size	Output-Scheduled Banyan Network with Input Buffering			Output-Scheduled Crossbar Network with Input Buffering		
P_r	60 %	90 %	100 %	60 %	90 %	100 %
	Single-Input Dual-Plane			Single-Input Dual-Plane		
N=4	69.60 %	55.40 %	48.70 %	70.40 %	55.60 %	48.70 %
N=8	67.80 %	52.80 %	46.40 %	69.00 %	53.20 %	46.50 %
N=16	65.70 %	51.30 %	44.80 %	67.20 %	52.00 %	45.10 %
N=64	61.90 %	49.20 %	42.90 %	65.10 %	50.80 %	43.70 %
	Dual-Input Dual-Plane			Dual-Input Dual-Plane		
N=4	89.60 %	60.00 %	50.00 %	89.70 %	60.00 %	50.00 %
N=8	87.30 %	59.80 %	49.90 %	89.20 %	59.90 %	49.90 %
N=16	83.90 %	59.20 %	49.80 %	88.60 %	59.80 %	49.90 %
N=64	77.10 %	56.80 %	48.70 %	87.90 %	59.60 %	49.80 %

In Figs. 4(a) and (b), we show the queuing delay behaviors of virtual input buffer for the dual-plane crossbar and banyan switches, respectively. In these figures, the queuing delay is normalized by the cell transmission cycle. The discrete-time analysis results are so close to the simulations that the 95 % confidence interval is not shown. These performance results are superior to those in the internal buffered ATM switch with cell bypass algorithm [6], [10].

In Figs. 5(a) and (b), we show the cell loss performance for the dual-plane crossbar and banyan switches as a function of the input buffer size for various offered loads. Note that these loss performance results are

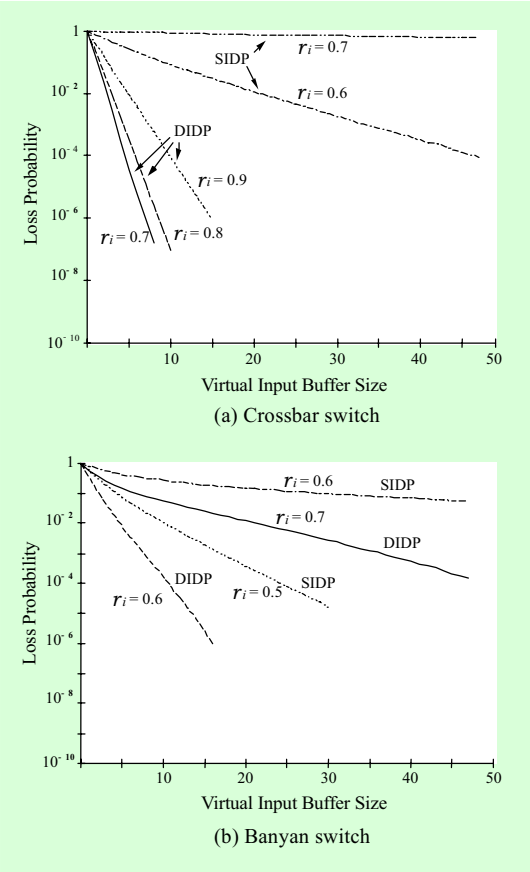

Fig. 5. Loss probability versus input buffer size: (a) crossbar switch, (b) banyan switch.

acceptable in comparison with those of the output queuing system [3]. The above performance results indicate that the DIDP crossbar switch is preferable to the SIDP switch which does not take advantage of the dual-plane architecture.

In order to show the performance of a proposed dual-plane switch in the case of the non-uniform traffic, we obtained the simulation results in Table 1(b). As the traffic model, we assume that the input traffic randomly arrives and is uniformly distributed with preference on the output ports with even number. One can show that degradation of maximum throughput occurs in the non-uniform traffic as one expects [11]. In this table, P_r is the probability that the input cell is toward the even output ports. When all the input cells are toward the even output, that is $P_r = 100$ %, maximum throughput would be less than 50 % as one can expect. In Figs. 6(a) and (b), we show the delay behaviors of the dual-plane crossbar and banyan switches for the non-uniform traffic which has the preference of probability P_r on the even outputs. In these figures, the curves are obtained by the simulation in which the discrete points are connected by the straight line with the one step interpolation. Figures 6(a) and (b) confirm the advantage of the DIDP approach over the SIDP.

For the performance of the dual-plane switches in the priority service, Figs. 7(a) and (b) show the queuing delay behaviors for two priority traffics. In these figures, we assume that the high priority traffic is equally loaded with the low priority traffic with the same traffic model. These simulation results show that the DIDP switches can provide the guaranteed delay for the high priority traffic even when the switch is highly utilized.

VI. CONCLUSIONS

In this paper, we investigate the dual-plane gigabit ATM switch, which can support the high-speed switching requirements with a rate more than 2.488 Gb/s of fu-

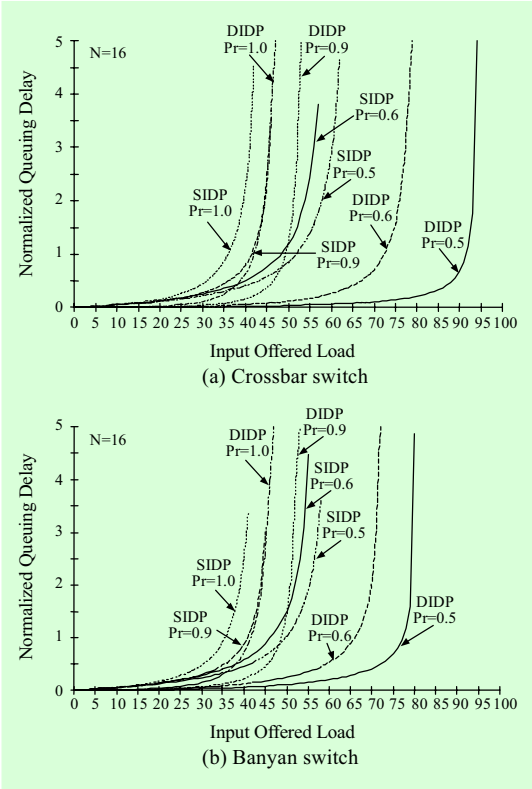

Fig. 6. Delay behavior of the dual-plane switch for non-uniform traffic: (a) crossbar switch, (b) banyan switch.

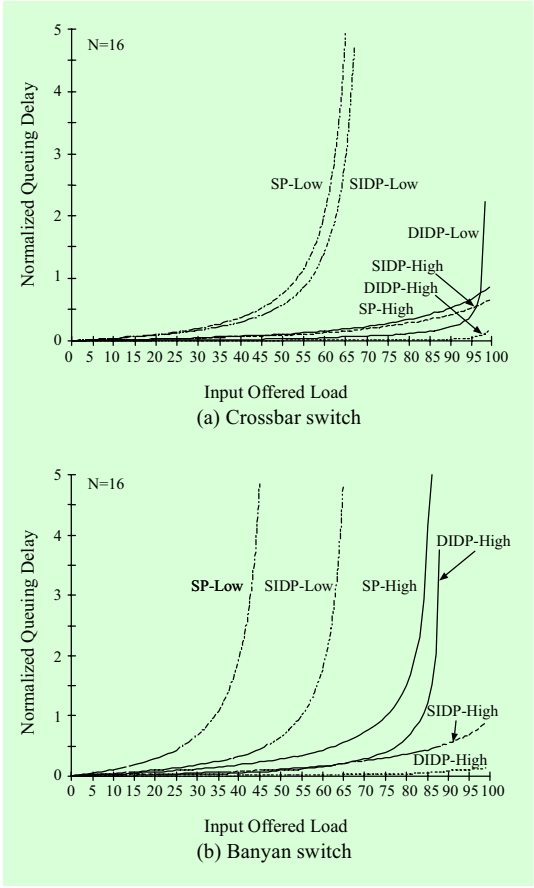

Fig. 7. Delay behavior of dual-plane switch for two priorities.

ture B-ISDN. In a proposed switch, we consider the path-level switching capability as well as the cell-level switching in accordance with virtual path concept of transmission system. The control path for cell header processing separates from the data flow path, which can support the switching flexibility including service class, control-level, and priority.

In the numerical results, a proposed 16×16 dual-input dual-plane crossbar switch has maximum throughput of about 95 %. It could also obtain maximum throughput of about 90 % in the dual-plane banyan topology. As the results, we show that a proposed 16×16 dual-plane switch would have the acceptable performance.

APPENDIX: CALCULATION OF INTERNAL BLOCKING PROBABILITIES FOR THE DUAL-PLANE SWITCH

In this Appendix, we show the discrete-

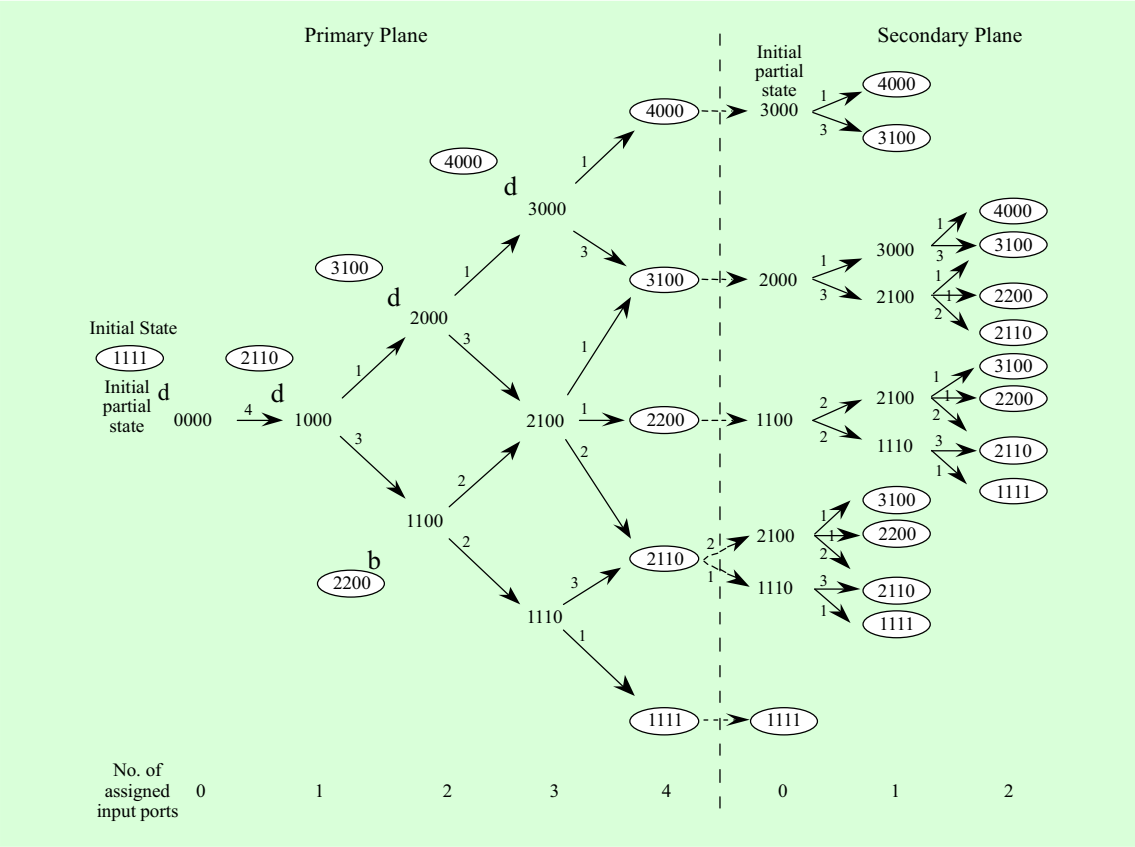

Fig. A-1. Enumeration mesh for the dual-plane switch.

time Markov chain model to calculate the internal blocking probabilities in the single-input dual-plane (SIDP) and dual-input dual-plane (DIDP) switches. For this, we extend the enumeration mesh proposed by Bhandarkar [9].

In Fig. A-1, we show the diagram of the extended enumeration mesh for the 4×4 dual-plane switch. Here, we assume that all the virtual input ports are active. In this figure, $(k_1,\ k_2,\ k_3,\ k_4)$ denotes the state of Markov chain, where k_i is the number that the head-of-line (HOL) cells in the virtual input queues are coming from an input port and $k_i \geq k_j$ for $i \leq j-1$ for the reduced state model. For example, (4, 0, 0, 0) means that all the HOL cells are coming from one input port. The circled states denote the initial states, which mean the states of the HOL virtual cells before they are served at the beginning of n-th cycle time. They also appear in the final terminal states at the end of n-th time. The initial partial state indicated from the initial state denotes the reduced state after the virtual queues are served during the n-th cycle. Then, Fig. A-1 shows the ways of reaching the final terminal states from the initial states. The number on the arrows shows the number of ways that transition can occur. The initial partial states of the secondary-plane

are generated from the final terminal states of the primary-plane by reducing the number of virtual input ports assigned for the secondary plane. In this figure, maximum number of virtual input ports that can be assigned for the secondary plane, $N^{\max}_{2,assigned}$, is given by

$$N^{\max}_{2,assigned} = \min(n_{1,non-zero}, N_{1,assigned} - n_{1,non-zero}), \quad \text{(A-1)}$$

where $N_{1,assigned}$ denotes the number of assigned virtual input ports for the primary plane and $N_{1,non-zero}$ is the number of non-zero terms of the final terminal states in the primary plane. Note that in the case of the DIDP switch, the number of assigned virtual input ports for the secondary plane is given by $N^{\max}_{2,assigned}$. But, in the case of the SIDP switch, the number of virtual input ports that can be assigned for the secondary plane would be less than or equal to $N^{\max}_{2,assigned}$ because the assigned virtual input ports for the secondary can be already occupied by the primary plane.

Now, let's the state probability vector in equilibrium be $\mathbf{P}=[P_{4000}, P_{3100}, P_{2200}, P_{1111}]^t$ and the state transition matrices for the primary and secondary planes be $\mathbf{A}$ and $\mathbf{B}$, respectively. Then, in the DIDP switch, it is satisfied as

$$\mathbf{P} = \mathbf{B}^t\mathbf{A}^t\mathbf{P}, \quad \text{(A-2)}$$

where

$$\mathbf{A} = \begin{bmatrix} \frac{1}{4} & \frac{3}{4} & 0 & 0 & 0 \\ \frac{1}{16} & \frac{3}{8} & \frac{3}{16} & \frac{3}{8} & 0 \\ 0 & \frac{1}{8} & \frac{1}{8} & \frac{5}{8} & \frac{1}{8} \\ \frac{1}{64} & \frac{3}{16} & \frac{9}{64} & \frac{9}{16} & \frac{3}{32} \\ \frac{1}{64} & \frac{3}{16} & \frac{9}{64} & \frac{9}{16} & \frac{3}{32} \end{bmatrix} \quad \text{(A-3)}$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{4} & \frac{3}{4} & 0 & 0 & 0 \\ \frac{1}{16} & \frac{3}{8} & \frac{3}{16} & \frac{3}{8} & 0 \\ 0 & \frac{1}{8} & \frac{1}{8} & \frac{5}{8} & \frac{1}{8} \\ 0 & \frac{1}{6} & \frac{1}{6} & \frac{7}{12} & \frac{1}{12} \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \quad \text{(A-4)}$$

Here, the average number of busy virtual input queues for the primary plane and the secondary plane, $\overline{N}_{1,busy}$, and $\overline{N}_{2,busy}$, are calculated respectively by

$$\overline{N}_{1,busy} = \mathbf{C}\cdot\mathbf{P}, \quad \text{(A-5)}$$

$$\overline{N}_{2,bysy} = \mathbf{C}_d\cdot\mathbf{P}, \quad \text{(A-6)}$$

where $\mathbf{C}$=[1, 2, 2, 3, 4] and $\mathbf{C}_d$=[1, 2, 2, 1, 0]. The internal blocking probabilities, P_{b1} and P_{b2}, are given by

$$P_{b1} = 1 - \frac{\overline{N}_{1,busy}}{\overline{N}_{1,offered}}, \quad \text{(A-7)}$$

$$P_{b2} = 1 - \frac{\overline{N}_{2,busy}}{\overline{N}_{2,offered}}, \quad \text{(A-8)}$$

where $\overline{N}_{1,offered} = N$ and $\overline{N}_{2,offered} = (1 - P_{b1})N$ in case of all the virtual input ports being active. For the SIDP switch, the state transition matrix $\mathbf{B}$ for the secondary plane would be changed according to the number of input ports that would be assigned for the secondary plane, which is represented by

$$\begin{aligned}\mathbf{B} &= \mathbf{B_0} + \mathbf{B_1} + \mathbf{B_2} \\ &= \begin{bmatrix} \frac{1}{4} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{4} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{4} & 0 & 0 \\ 0 & 0 & 0 & \frac{3}{4} & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \\ &\quad + \begin{bmatrix} \frac{3}{16} & \frac{9}{16} & 0 & 0 & 0 \\ \frac{5}{128} & \frac{15}{64} & \frac{15}{128} & \frac{15}{64} & 0 \\ 0 & \frac{5}{32} & \frac{5}{32} & \frac{5}{16} & 0 \\ 0 & \frac{1}{24} & \frac{1}{24} & \frac{7}{48} & \frac{1}{48} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \\ &\quad + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ \frac{1}{128} & \frac{3}{64} & \frac{3}{128} & \frac{3}{64} & 0 \\ 0 & \frac{1}{64} & \frac{1}{64} & \frac{5}{64} & \frac{1}{64} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \end{aligned} \tag{A-9}$$

where the subscript of $\mathbf{B}_i$ denotes the number of virtual input ports that are assigned at the secondary plane. Then, $\mathbf{B}_i (0 \le i \le 2)$ is the state transition probability matrix to reach the final terminal state after i virtual input ports are served in the secondary plane. Here, $\mathbf{B}_0$ shows the transition probability matrix that has no state transition since all the virtual input ports assigned for the secondary plane are already occupied in the primary plane. In the SIDP switch, the average number of busy virtual queue for the secondary plane, $\overline{N}_{2,busy}$, is given by

$$\overline{N}_{2,busy} = \mathbf{C}_s \cdot \mathbf{P} \ , \tag{A-10}$$

where

$$\mathbf{C}_s = \left[\frac{3}{4}, \left(\frac{5}{8} + \frac{1}{8} \cdot 2 \right), \left(\frac{5}{8} + \frac{1}{8} \cdot 2 \right), \frac{1}{4}, \ 0 \right].$$

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