

Distance Protection Solution for a Converter Controlled Microgrid

J. Manjula Dewadasa, Arindam Ghosh and Gerard Ledwich

ABSTRACT: Distance relay response in the presence of a converter dominated microgrid system has been analyzed in this paper. Converter structure and control mechanism are presented and a new method is proposed to limit fault currents in faulted phase/phases by reducing the converter output voltage. A method of analyzing unsymmetrical supply voltage using symmetrical component theory is proposed, where it has been assumed that voltage source converter (VSC) supplies unbalanced voltages in the event of a fault. Performance of distance relays with Mho characteristics are evaluated in a radial distribution feeder for both phase and earth unbalanced faults. The results are validated through PSCAD simulation and MATLAB calculations.

Index Terms: Microgrid, Distance Protection, Apparent Impedance, Symmetrical components, Unsymmetrical Faults.

I. INTRODUCTION

WITH THE climate change posing a grave environmental concern, distributed generation using renewable and/or less polluting sources is gaining importance. Previously it was expected that 20% of power generation will be DGs by the year 2020 [1]. However with most countries ratifying the Kyoto Protocol, the penetration level of DGs is expected to be higher by that time. Moreover the cost of transmission and distribution is rising with the rapid increase in load demand. The cost of DG technologies is expected to come down with mass production and governmental subsidies. Thus from financial standpoint, it will become attractive to increase the generation at the distribution level by connecting a DG at various points in a network.

A microgrid is an entirely DG based grid which contains both generators and loads. It is usually connected to the utility grid at a point which is called the point of common coupling (PCC). To the utility grid, the microgrid behaves as a fully controllable load. Moreover it can operate in both the grid connected and the islanded modes [2-4, 5]. There is a need to protect a micro-grid in both islanded and grid-connected modes of operation. The islanding event poses a high risk to user equipment, utility element and personnel [6]. The one of the major issues arises in islanding can be identified when it is supplied by current limited inverter sources [2, 5, 7].

Most of the existing distribution systems are radial due to the simplicity and low cost of overcurrent protection [6]. But in the presence of converter-connected DGs, overcurrent devices may not respond or may be slow to respond as a result of lower fault current levels [2-4, 8, 9]. Because the converter fault currents are usually limited to a value that is twice the rated current [2, 5, 8], a possible approach that facilitates the use the existing overcurrent protection is up-rating of the con-

verters, such that required fault current can be supplied. This however will be expensive. Once such method is reported in [4], which uses flywheel energy storage during fault system to supply the necessary fault current.

This paper discusses a distance protection scheme for detection and protection in both islanded and grid connected microgrid. Distance relays can clear faults quickly, thereby facilitating to maintain the stability of the system during contingencies. In this paper we discuss a method to analyze a faulted network with unsymmetrical voltage source converter. The distance protection scheme is implemented based on this derivation. The results are verified through MATLAB calculations and PSCAD simulations.

II. CONVERTER STRUCTURE AND CONTROL

The converter structure is shown in Fig. 1. The DG is assumed to be an ideal dc voltage source supplying V_{dc} to the VSC. The converter contains three H-bridges. The outputs of the H-bridges are connected to three single-phase transformers that are connected in wye for required isolation and voltage boosting [10]. The resistance R_f represents the switching and transformer losses, while the inductance L_f represents the leakage reactance of the transformers. The filter capacitor C_f is connected to the output of the transformers to bypass switching harmonics.

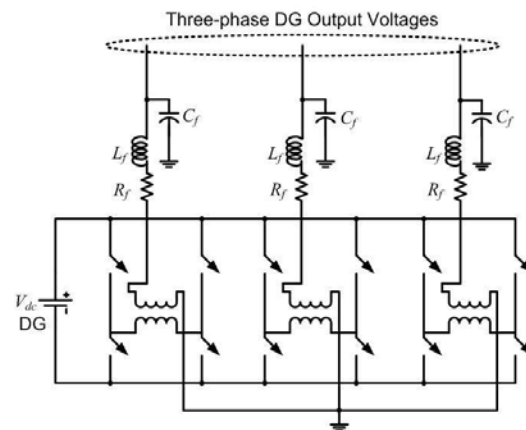


Fig. 1. Converter structure.

The advantage of the converter structure shown in Fig. 1 is that it is capable of generating unbalanced voltages in the three phases independently. To protect the inverter in case of a fault is to restrict the currents in all the three phases. One way of accomplishing this is by injecting a balanced current that can be about twice the rated current. This will however cause the voltages in the unfaulted phases to rise in case of unbal-

M. Dewadasa, A. Ghosh and G. Ledwich are with the School of Engineering Systems, Queensland University of Technology, Brisbane, Qld 4001, Australia.

anced faults [2]. This obviously is not desirable as the single-phase loads in the healthy phases will be stressed by the higher current through them. Since the converter of Fig. 1 can supply unbalanced voltages, we propose to reduce the voltage in the faulted phases when a fault is detected, while keeping the voltage of the healthy phases unaltered.

A. Converter Control

The equivalent circuit of one phase of the converter is shown in Fig. 2. In this, $u \cdot V_{dc}$ represents the converter output voltage, where $u = \pm 1$. The main aim of the converter control is to generate u . From the circuit of Fig. 2, the state space description of the system can be given as

$$\dot{x} = Ax + Bu_c \quad (1)$$

where u_c is the continuous time control input, based on which the switching function u is determined. The discrete-time equivalent of (1) is

$$x(k+1) = Fx(k) + Gu_c(k) \quad (2)$$

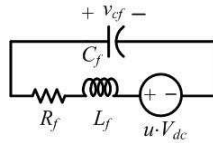


Fig. 2. Equivalent circuit of one phase of the converter.

Let the output of the system given in (2) be v_{cf} . The reference for this voltage is given by the instantaneous peak and phase angle of each phase. Let this be denoted by v^* . The input-output relationship of the system in (2) can be written as

$$\frac{v_{cf}(z)}{u_c(z)} = \frac{M(z^{-1})}{N(z^{-1})}$$

The control is computed from

$$u_c(z) = \frac{S(z^{-1})}{R(z^{-1})} \{v^*(z) - v_{cf}(z)\} \quad (3)$$

The closed-loop transfer function of the system is then

$$\frac{v_{cf}(z)}{v^*(z)} = \frac{M(z^{-1})S(z^{-1})}{N(z^{-1})R(z^{-1}) + M(z^{-1})S(z^{-1})} \quad (4)$$

The coefficients of the polynomials S and R can be chosen based on a pole placement strategy [11]. Once u_c is computed from (4), the switching function u can be generated as

$$\begin{aligned} \text{If } u_c > h \text{ then } u &= +1 \\ \text{elseif } u_c < -h \text{ then } u &= -1 \end{aligned} \quad (5)$$

where h is a small number.

B. Reference Voltage Generation

The control in (3) is computed based on the reference voltage v^* and the feedback of the capacitor voltage v_{cf} . The reference voltages are given by

$$\begin{aligned} v_a^* &= V_n \sin(\omega t) \\ v_b^* &= V_n \sin(\omega t - 120^\circ) \\ v_c^* &= V_n \sin(\omega t + 120^\circ) \end{aligned} \quad (6)$$

where V_n is the instantaneous peak voltage magnitude. Under nominal condition, $V_n = V_{n0}$. The rms values of the VSC output currents of all the three phases are monitored continuously. Once a fault occurs, the output currents shoot up. When the rms values of a particular phase crosses a threshold, the reference voltage of that phase is quenched by choosing $V_n = V_{nf}$, where $V_{nf} \ll V_{n0}$. The value of V_{nf} is chosen based on the worst case current (i.e., a fault near VSC terminals) that the converter can inject. Note that for an internal fault, the VSC is switched off to protect its switches and microgrid protection issue does not arise in this case.

III. UNSYMMETRICAL FAULT CALCULATIONS

For the calculation of fault currents, we shall make the following assumptions that the system is balanced before the fault occurs. In this case the three phases of the VSC is supplying a set of balanced voltages (i.e., with the same peak and phase displacement of 120°). Once a fault is detected in one of the phases, the voltage of the particular phase is reduced, while its phase angle is retained such that the VSC output voltages are still phase displaced by 120° . The faulted network is shown in Fig. 3 where the voltages at the faulted point are denoted by V_{tha} , V_{thb} , V_{thc} and current in the three faulted phases are I_{fa} , I_{fb} and I_{fc} . We shall now find expressions of fault currents for different types of faults.

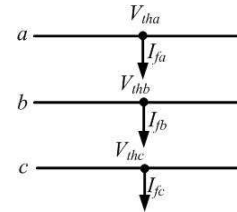


Fig. 3. Representation of a faulted segment.

A. Single-Line-to-Ground (1LG) Fault

Let a 1LG fault has occurred at node k of a network. The faulted segment is then as shown in Fig. 4 where it is assumed that phase-a has been grounded through an impedance Z_f . Assuming that the system is unloaded before the occurrence of the fault, it is well-known that the sequence components of the fault current will be given by [12, 13]

$$I_{fa0} = I_{fa1} = I_{fa2} = \frac{I_{fa}}{3} \quad (7)$$

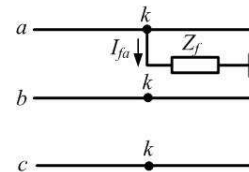


Fig. 4. Representation of 1LG fault.

For a 1LG fault in phase-a, the VSC output voltage for the phase will be reduced, while the output voltages of phases B and C will remain unaltered. Also since the phase difference between the source voltages will remain at 120° , the Thevenin voltages at the fault point can be expressed as

$$V_{tha} = V_f \angle 0^\circ, V_{thb} = V_m \angle -120^\circ, V_{thc} = V_m \angle 120^\circ \quad (8)$$

Where V_m is the magnitude of unfaulted rms voltage and V_f is the magnitude of reduced rms voltage in the faulted phase. Then the sequence components of the voltages are

$$V_{tha012} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_f \angle 0^\circ \\ V_m \angle -120^\circ \\ V_m \angle 120^\circ \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_f \\ a^2 V_m \\ a V_m \end{bmatrix}$$

From the above equation, we get

$$V_{tha012} = \frac{1}{3} \begin{bmatrix} V_f + a^2 V_m + a V_m \\ V_f + a^3 V_m + a^3 V_m \\ V_f + a V_m + a^2 V_m \end{bmatrix} = \frac{1}{3} \begin{bmatrix} V_f - V_m \\ V_f + 2V_m \\ V_f - V_m \end{bmatrix} \quad (9)$$

Let us denote the zero, positive and negative sequence Thevenin impedance at the faulted point as Z_{kk0} , Z_{kk1} and Z_{kk2} respectively. Also note since the source voltages are unbalanced, the negative and zero sequence Thevenin voltages will not be zero. We can then write

$$\begin{aligned} V_{ka0} &= V_{tha0} - Z_{kk0} I_{fa0} \\ V_{ka1} &= V_{tha1} - Z_{kk1} I_{fa1} \\ V_{ka2} &= V_{tha2} - Z_{kk2} I_{fa2} \end{aligned}$$

Adding the voltages we get

$$\begin{aligned} V_{ka} &= V_{ka0} + V_{ka1} + V_{ka2} \\ &= V_{tha0} + V_{tha1} + V_{tha2} - (Z_{kk0} + Z_{kk1} + Z_{kk2}) I_{fa0} \end{aligned} \quad (10)$$

Again from Fig. 4, we can write

$$V_{ka} = Z_f I_{fa} = Z_f (I_{fa0} + I_{fa1} + I_{fa2}) = 3Z_f I_{fa0} \quad (11)$$

Therefore combining (10) and (11), we get

$$\begin{aligned} I_{fa0} &= \frac{V_{tha0} + V_{tha1} + V_{tha2}}{Z_{kk0} + Z_{kk1} + Z_{kk2} + 3Z_f} \\ &= \frac{V_f}{Z_{kk0} + Z_{kk1} + Z_{kk2} + 3Z_f} \end{aligned} \quad (12)$$

The Thevenin equivalent sequence network is shown in Fig. 5.

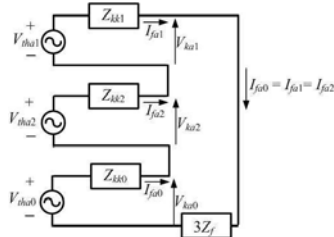


Fig. 5. Thevenin equivalent of a 1LG fault.

B. Line-to-Line (LL) fault

The faulted segment for an L-L fault is shown in Fig. 4 in which the phases b and c got shorted through the impedance Z_f . Assuming that the system is unloaded before the occurrence of the fault we have the following fault current equation [12, 13]

$$I_{fa0} = 0, I_{fa1} = -I_{fa2} \quad (13)$$

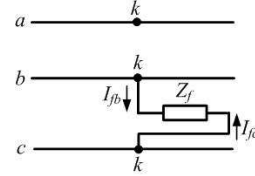


Fig. 6. Representation of L-L fault.

Now from Fig. 6, we get the following expression for the voltage at the faulted point

$$V_{kb} - V_{kc} = Z_f I_{fb} = (a^2 - a)(V_{ka1} - V_{ka2}) \quad (14)$$

Also from (13), we can write

$$I_{fb} = I_{fb0} + I_{fb1} + I_{fb2} = a^2 I_{fa1} + a I_{fa2} = (a^2 - a) I_{fa1} \quad (15)$$

Therefore combining (14)-(15) we get

$$V_{ka1} - V_{ka2} = Z_f I_{fa1} \quad (16)$$

Equations (13) and (16) indicate that the positive and negative sequence networks are in parallel. The sequence network is then as shown in Fig. 7. From this network we get

$$I_{fa1} = -I_{fa2} = \frac{V_{tha1} - V_{tha2}}{Z_{kk1} + Z_{kk2} + Z_f} \quad (17)$$

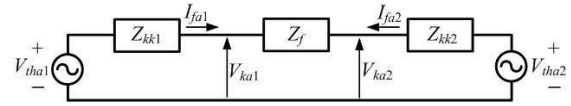


Fig. 7. Thevenin equivalent of an LL fault.

Since the fault is phases b and c, the voltages in these two phases are reduced, while that of phase a is maintained. Therefore the Thevenin voltages are

$$\begin{aligned} V_{tha} &= V_m \angle 0^\circ \\ V_{thb} &= V_f \angle -120^\circ \\ V_{thc} &= V_f \angle 120^\circ \end{aligned} \quad (18)$$

Then the sequence components of the voltages are

$$V_{tha012} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_m \angle 0^\circ \\ V_f \angle -120^\circ \\ V_f \angle 120^\circ \end{bmatrix} = \frac{1}{3} \begin{bmatrix} V_m - V_f \\ V_m + 2V_f \\ V_m - V_f \end{bmatrix} \quad (19)$$

From (17) and (19), we can write the sequence components of the fault current as

$$I_{fa1} = -I_{fa2} = \frac{1}{3} \frac{(V_m + 2V_f - V_m + V_f)}{Z_{kk1} + Z_{kk2} + Z_f} \quad (20)$$

$$= \frac{V_f}{Z_{kk1} + Z_{kk2} + Z_f}$$

C. Double-Line-to-Ground (2LG) Fault

The representation of the faulted network is shown in Fig. 8 where the phases b and c got shorted through the impedance Z_f to the ground. Since the system is unloaded before the occurrence of the fault we have [12, 13]

$$3I_{fa0} = I_{fb} + I_{fc}, \quad V_{kb} = V_{kc} = 3Z_f I_{fa0} \quad (21)$$

Furthermore using the symmetrical component transformation, we get

$$V_{ka1} = V_{ka2} \quad (22)$$

$$3V_{ka0} = V_{ka} + 2V_{kb} = V_{ka0} + V_{ka1} + V_{ka2} + 2V_{kb} \quad (23)$$

Combining (21)-(23), we get

$$V_{ka1} = V_{ka2} = V_{ka0} - 3Z_f I_{fa0} \quad (24)$$

Also since $I_{fa} = 0$ we have

$$I_{fa0} + I_{fa1} + I_{fa2} = 0 \quad (25)$$

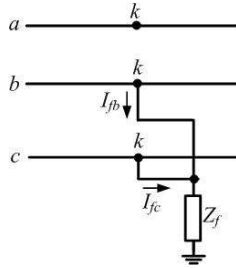


Fig. 8. Representation of 2LG fault.

The Thevenin equivalent circuit for 2LG fault is shown in Fig. 9. From this figure we get the following three equations

$$V_{tha1} - V_p = Z_{kk1} I_{fa1} \quad (26)$$

$$V_{tha2} - V_p = Z_{kk2} I_{fa2} \quad (27)$$

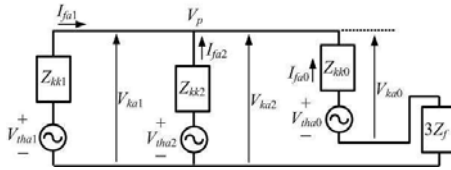


Fig. 9. Thevenin equivalent of a 2LG fault.

$$V_{tha0} - V_p = (Z_{kk0} + 3Z_f) I_{fa0} \quad (28)$$

Since the phases b and c are faulted, the Thevenin voltages will be as given in (19). Therefore combining (26)-(28) with (19), we get the following equations

$$V_f = Z_{kk1} I_{fa1} - Z_{kk2} I_{fa2} \quad (29)$$

$$V_f = Z_{kk1} I_{fa1} - (Z_{kk0} + 3Z_f) I_{fa0} \quad (30)$$

$$0 = Z_{kk2} I_{fa2} - (Z_{kk0} + 3Z_f) I_{fa0} \quad (31)$$

The equivalent circuit of Fig. 10 is obtained from (29-31). From this equivalent circuit, we get the following three equations

$$I_{fa1} = \frac{V_f}{Z_{kk1} + \frac{Z_{kk2}(Z_{kk0} + 3Z_f)}{Z_{kk2} + Z_{kk0} + 3Z_f}} \quad (32)$$

$$I_{fa0} = -I_{fa1} \left(\frac{Z_{kk2}}{Z_{kk2} + Z_{kk0} + 3Z_f} \right) \quad (33)$$

$$I_{fa2} = -I_{fa1} \left(\frac{Z_{kk0} + 3Z_f}{Z_{kk2} + Z_{kk0} + 3Z_f} \right) \quad (34)$$

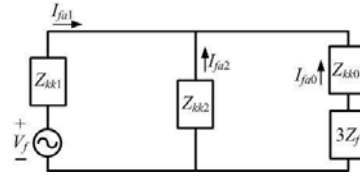


Fig. 10. Reduced equivalent circuit of a 2LG fault.

The equations derived for all the three unbalanced fault cases are similar to the standard equations used for fault calculation assuming positive sequence source voltage only [12, 13]. However the major difference is that the fault currents are dependent on the reduced voltage magnitude V_f of the faulted phase(s) and not on the nominal voltage magnitude V_m . This is a major finding that will help us to analyze voltage limited (or even current limited) faulted network.

TABLE-I: COMPARISON MATLAB AND PSCAD RESULTS FOR DIFFERENT TYPES OF FAULTS.

Fault Type	MATLAB		PSCAD	
	Current (kA)	Voltage (kV)	Current (kA)	Voltage (kV)
1LG	0	0.13∠-83.6°	2.12∠-180°	2.09∠-178°
	pos	0.13∠-83.6°	4.24∠0°	4.19∠1.8°
	neg	0.13∠-83.6°	2.12∠-180°	2.09∠-178°
2LG	0	0.12∠96.6°	2.12∠-0.03°	2.10∠1.83°
	pos	0.25∠-83.6°	2.12∠-0.03°	2.10∠1.71°
	neg	0.12∠96.2°	2.12∠-0.03°	2.10∠1.83°
LL	0	0	1.53∠0°	1.51∠1.71°
	pos	0.19∠-83.6°	2.41∠-0.02°	2.38∠1.83°
	neg	0.19∠96.3°	2.41∠0.02°	2.38∠1.83°

Example 1: Let us consider a simple system in which the VSC is connected to the fault point through an impedance of $0.5050 + j4.5867 \Omega$ and the fault impedance (Z_f) is 0.01Ω . The VSC voltages before the fault have an rms magnitude of 6.35 kV, while this is reduced to 1.77 kV rms in the faulted phase. The scheme for the switchover of the voltages during faults is given in Section II.B. Table-I summarizes the results obtained for the three faults mentioned above. This table lists the phasor values calculated using MATLAB and those ob-

tained during PSCAD simulations using fundamental phasor extraction program [14]. The fault current and voltage at the fault point listed here. It can be seen from this table that the PSCAD results match closely with the theoretical results calculated by MATLAB. We can therefore use this method for distance relay settings.

IV. IMPLEMENTATION OF DISTANCE PROTECTION SCHEME

To find out the suitability of application of distance relays for protection of microgrid under the voltage limited environment during faults, a four bus bar radial system is considered. The schematic diagram of one phase of the system is shown in Fig. 11. In this the DG is represented by the dc voltage source V_{dc} . The utility supply is denoted by V_s , while the source feeder impedance is denoted by Z_s . The microgrid feeder impedances are denoted by Z_{12} , Z_{23} and Z_{34} . A load with impedance of Z_L has been assumed to be connected at Bus-3. The system parameters are given in Table II.

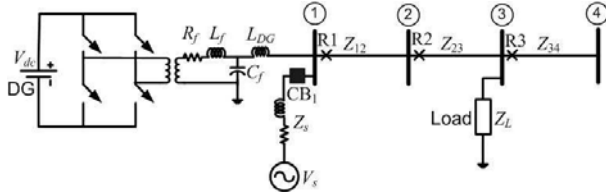


Fig. 11. The schematic diagram of the study system.

TABLE-II: SYSTEM DATA.

System data	Values
System frequency	50 Hz
Source voltage (V_s)	11 kV rms (L-L)
Source impedance	$Z_s = 0.078 + j 0.785 \Omega$
Feeder impedance	$Z_{12} = Z_{23} = Z_{34} = 3.025 + j 18.143 \Omega$
Load Impedance	$Z_L = 40.33 + j 0 \Omega$
Converter data	
DC voltage (V_{dc})	3.5 kV
Transformer rating	3.5 kV/11 kV, 1 MVA, 0.1 pu reactance
VSC losses (R_f)	3.0 Ω
Filter capacitance (C_f)	100 μ F
Input inductance	$L_{DG} = 10$ mH

Different types of faults are generated at different locations with changes in fault resistance and load conditions. For studies in this paper, we have assumed that the fault occurs at Bus-2. Distance relays having MHO characteristic with two zones of protection are used in the studies. Zone settings are chosen such that Zone-1 covers 80 per cent of the protected line, while Zone-2 covers the whole the protected line, plus 50 per cent of the adjacent line. For example, relay R_2 protects 80% of Line 2-3 in Zone-1 and 100% of Line 2-3 and 80% of Line 3-4 in Zone-2. The conventional method of calculating the apparent impedance seen by each earth and phase element of relay is given by (35) and (36) respectively.

$$Z_{LG} = \frac{V_{phase}}{I_{phase} + KI_0} \quad (35)$$

$$Z_{LL} = \frac{V_{phase1} - V_{phase2}}{I_{phase1} - I_{phase2}} \quad (36)$$

Equation (35) is used for earth fault and it includes the residual compensation factor K and zero sequence current I_0 . For

inter-phase faults, (36) is used based on the voltage and current differences between the phases. We shall now present some of the results.

A. ILG Fault

Figs. 12 and 13 give the apparent impedance plot of R1 and R2 with the variation of fault resistance in the grid connected and islanded mode operations respectively. It can be seen that operation of R1 is the same for the both modes, while R2 shows a slight difference for the islanded mode. The relay R2 sees this fault as reverse since it is located downstream from the fault. Therefore R2 operates in Zone-1 while R1 operates in Zone-2 for the small fault resistance values. Thus R2 responds before the R1 and open the circuit breaker at Bus-2. From the point of relay discrimination, this can be identified as an unacceptable operation.

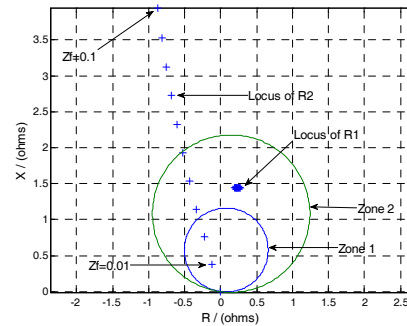


Fig. 12. Impedance plot of R1 & R2 for 1LG with fault resistance variation (0.01 Ω - 0.1 Ω) in grid connected mode with a load of 3 MW.

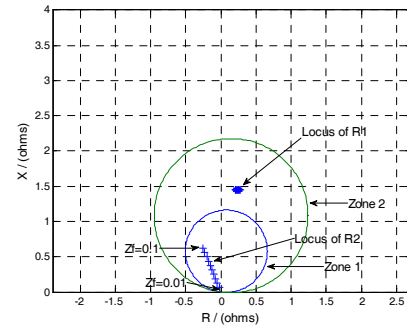


Fig. 13. Impedance plot of R1 & R2 for 1LG with fault resistance variation (0.01-0.1 Ω) in islanded mode with a load of 3 MW.

The PSCAD simulation results for the islanded case are shown in Fig. 14 in which the fault occurs at 0.1 s. It can be seen as soon as the fault is detected, the VSC voltage of phase-a reduces. Even though the current in the other two phases are unaltered, phase-a supplies a relatively large fault current. The relay R2 operates at 0.133 s thereby cutting of the load from the supply. However the phase-a current still continues to flow since the fault location is upstream from R2. The fault is isolated at 0.426 s when the relay R1 operates. The inverter voltages attain their nominal values thereafter.

B. LL Fault

For this case, both R1 and R2 behave identically for both grid-connected and islanding modes. Also the relays operate

correctly in both modes without disturbing the relay coordination. The results for this case are not shown here.

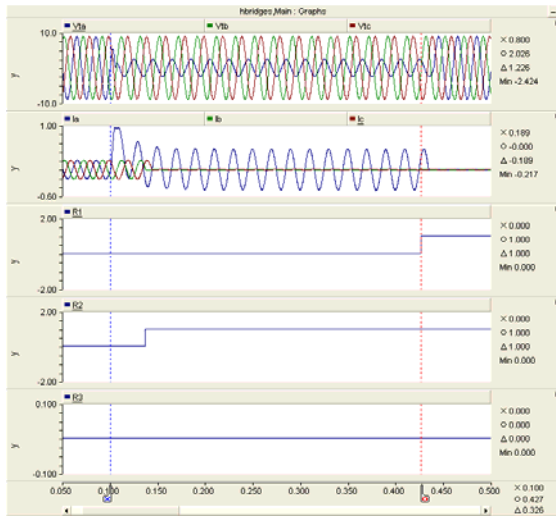


Fig. 14. System response to a 1LG fault.

C. 2LG Fault

The apparent impedance plot of R1 and R2 for a 2LG fault between phase B and phase C in grid connected and islanded mode are shown in the Figs. 15 and 16 respectively. The plots are very similar to those of the 1LG fault, since the same earth element is employed to calculate the apparent impedances for ground faults. In this case, R1 operates in Zone-2 as expected for a fault at Bus-2. However R2 operates in Zone-1 for low values of fault resistance, which is unacceptable.

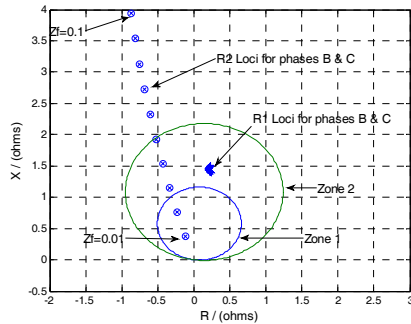


Fig. 15. Impedance plot of R1 and R2 with fault resistance (0.01 Ω -0.1Ω) in grid connected mode with a load of 3 MW.

V. CONCLUSIONS

A method for analyzing fault characteristics in a converter controlled microgrid is discussed in this paper. Based on this method, we can calculate the sequence currents and voltages at the relay locations. The effects of fault resistance and load were considered on the Mho characteristics. It has been shown that the relay downstream to the fault operates unnecessarily for the ground faults when a star connected load is connected downstream to the fault and the low fault resistance appears at the fault point. Therefore, the impedance relays with Mho characteristics may lead to an unnecessary operation by violating the coordination rules.

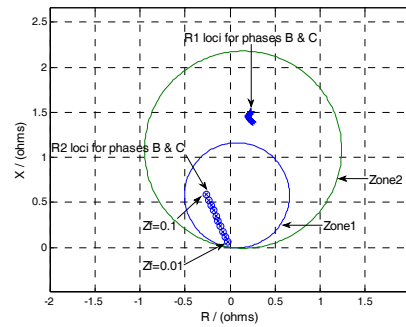


Fig. 16. Impedance plot of R1 and R2 with fault resistance (0.01 Ω -0.1Ω) in islanded mode with a load of 3 MW.

To alleviate this problem, a directional feature should be added to the distance protection scheme. A negative sequence impedance analysis is currently tried out to make sure that it can be effectively used to discriminate forward and reverse faults. This will be reported in future.

ACKNOWLEDGEMENT

The authors thank the Australian Research Council (ARC) for the financial support for this project through the ARC Discovery Grant DP 0774092.

REFERENCES

- [1] G. M. Masters, *Renewable and Efficient Electric Power Systems*, Wiley-Interscience, New Jersey, 2004.
- [2] M. Brucoli, T. C. Green, and J. D. F. McDonald, "Modelling and analysis of fault behaviour of inverter microgrids to aid future fault detection," *System of Systems Engineering, SoSE '07. IEEE International Conference on*, pp. 1-6, 2007.
- [3] R. H. Lasseter, "MicroGrids," *Power Engineering Society Winter Meeting, 2002*, vol. 1, pp. 305-308, 2002.
- [4] N. Jayawarna, N. Jenkins, M. Barnes, M. Lorentzou, S. Papthanasasiou, and N. Hatziaiyriou, "Safety analysis of a microgrid," *International Conference on Future Power Systems*, pp. 1-7, 2005.
- [5] H. Nikkhajoei and R. H. Lasseter, "Microgrid protection," *Power Engineering Society General Meeting, IEEE*, pp. 1-6, 2007.
- [6] J. C. Gómez and M. M. Morcos, "Coordination of voltage sag and overcurrent protection in DG systems," *IEEE Trans. Power Delivery*, vol. 20, pp. 214-218, 2005.
- [7] R. M. Tumilty, M. Brucoli, G. M. Burt, and T. C. Green, "Approaches to network protection for inverter dominated electrical distribution systems," in *The 3rd IET International Conference on Power Electronics, Machines and Drives*, pp. 622-626, 2006.
- [8] M. Brucoli and T. C. Green, *Fault Response of Inverter Dominated Microgrids*, Report, Department of Electrical and Electronic Engineering, Imperial College.
- [9] H. Al-Nasseri, M. A. Redfern, F. Li, , and "A voltage based protection for micro-grids containing power electronic converters " *Power Engineering Society General Meeting, IEEE*, 2006.
- [10] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," *IEEE Trans. on Power Delivery*, Vol. 15, No. 1, pp. 417-422, 2000.
- [11] A. Ghosh, "Performance study of two different compensating devices in a custom power park," *Proc. IEE – Generation, Transmission & Distribution*, Vol. 152, No. 4, pp. 521-528, 2005.
- [12] J. D. Glover and M. S. Sarma, *Power Systems Analysis and Design*, 3rd Ed., Books/Cole, Pacific Grove, CA, 2002.
- [13] J. J. Grainger and W. D. Stevenson, Jr., *Power System Analysis*, McGraw-Hill, New York, 1994.
- [14] A. Ghosh and G. Ledwich, *Power Quality Enhancement using Custom Power Devices*, Kluwer Academic Publishers, Norwell, MA, 2002.