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Distributed Control for a Modular Multilevel Converter

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***Abstract*—Conventional centralized control strategies may reduce the flexibility and expandability of a Modular Multilevel Converter (MMC) system. To tackle this issue, this paper proposes a distributed control architecture that is capable of assigning certain control tasks to distributed local controllers and improves the modularity of an MMC system. A central controller dealing with the output current regulation based on sensed arm currents is adopted. The control of MMC internal dynamics and the pulse-width modulation (PWM) generation are distributed into local controllers. Unlike the conventional MMC control that needs all sub-module capacitor voltages for capacitor voltage averaging, the proposed capacitor voltage control only relies on local sub-module voltage measurement. Consequently, communication-intensive capacitor voltage transmission in each control cycle is not required and the communication burden of the control system can be significantly reduced. The control loops and possible control conflicts among sub-modules are presented and considered for system stability analysis. The effectiveness of the proposed distributed control architecture and capacitor voltage control for an MMC are confirmed by the start-up, steady state, and transient experimental results.**

***Index Terms*—Modular Multilevel Converter, distributed control strategy, capacitor voltage control.**

I. Introduction

MODULAR Multilevel Converter (MMC) is one of the promising topologies in recent years for medium or high voltage industrial applications, such as high-voltage DC transmission (HVDC) [1], medium voltage variable speed drives [2] and static synchronous compensators [3]. The wide adoption of MMCs in the industry is mainly due to its modularity, flexible expandability, transformer-less configuration, common DC bus, high reliability from redundancy, etc. However, most of the MMCs discussed in existing literature are operated with highly centralized control strategies for multiple control objectives such as output voltage or current regulation, sub-module capacitor voltage averaging and balancing, and circulating ripple current suppression or injection [4-7]. Such centralized control strategies [8-11], whose typical structure is presented in Fig. 1, limit the modularity and expandability of the overall MMC system in terms of software development. In those control strategies, all the measurements and controls are centralized in a controller (DSP), and the gating signals are generated by FPGA modules. The computational burden is heavy and the execution time might be not sufficient in each control cycle if all tasks are centralized into a single digital controller, especially in an MMC with a large number of sub-modules. Therefore, it is beneficial and preferable to investigate distributed control architectures for MMC systems in order to distribute computation burden to different digital controllers and improve the system modularity.

Distributed control structures for MMC systems gradually attract the attention of researchers in recent years. Two different Ethernet-based protocols, distributed PWM generation and voltage balancing control are discussed in [12], where the communication delay and distributed control loop stability are investigated. A resampled uniform PWM strategy that can be applied in MMC distributed control systems is introduced in [13]. The distributed PWM carrier synchronization technique for local controllers based on EtherCAT distributed clock mechanism is exclusively addressed in [14]. A distributed control system with reduced data transmission from the central controller to local controllers is discussed in [15]. A distributed control method for an MMC based on CAN bus communication is proposed in [16]. However, the control strategy in [16] is only capable for MMCs with a low number of sub-modules. A comprehensive explanation and implementation of a control scheme based on hierarchical control units for different control tasks are reported in [17], which is complex in coordinating different control tasks if a large number of sub-modules are connected in each arm. All of the MMC distributed control architectures discussed in literature so far employ a central controller to process the tasks such as output power control, sub-module capacitor voltage averaging, differential current regulation, and system level protections. Other tasks, e.g. sub-module capacitor voltage measurement, capacitor voltage balancing, PWM generation and local protections, are distributed into local controllers. It's worth emphasizing that the capacitor voltage control and balancing are important tasks for the stable operation of MMCs, which have attracted considerable research interests in recent years. A capacitor voltage balancing method for a ±350kV/1000MW MMC is presented in [18], where a Balancing Adjusting Number is introduced into the sorting-based capacitor voltage balancing algorithm for a relatively low switching frequency. In order to

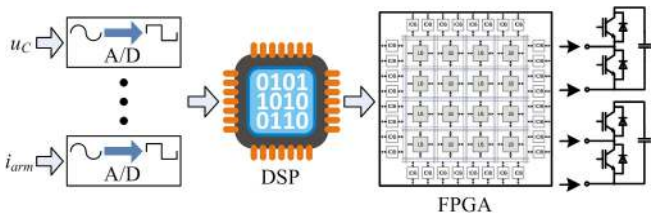

Fig. 1. Centralized control structure for MMCs.

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reduce the switching losses of the MMCs in high power applications, an alternating number controller is designed in [19] to make a trade-off between the switching losses and the effectiveness of the capacitor voltage balancing algorithm. By evaluating the charging capabilities of the driving pulses, the capacitor voltage balancing with fundamental sorting frequency is achieved in [20]. In [21], the capacitor average voltage is regulated according to the energy decomposition of the arms, and the capacitor voltage within each arm is balanced using a sorting algorithm after the modulation. More capacitor voltage balancing methods based on the various sorting algorithms have been discussed in [22-24]. The sorting algorithm based capacitor voltage balancing methods are more suitable for a centralized control system that requires high computational capability and the awareness of all capacitor voltages. The gating signals for the sub-modules have to be selected based on the sorting results in the same controller. Therefore, the sorting-based capacitor voltage balancing methods are rarely discussed in the literature of distributed control strategies. On the other hand, methods similar to the active-control-based capacitor voltage control and balancing methods with phase-shifted PWM scheme discussed in [8, 25, 26] are generally adopted in MMC distributed control strategies [12-14, 16]. It should be noted that the sub-module capacitor voltage controls are divided into different parts and separately implemented in the central and local controllers in existing distributed control strategies. In order to implement the capacitor voltage averaging, the central controller in existing distributed control has to be aware of all sub-module capacitor voltages, which requires the voltages measured by local controllers to be sent to the central controller through a communication network. In the case of an MMC system with considerable sub-modules, the communication load is quite high if all the sub-module capacitor voltages are transmitted to the central controller. Therefore, the baud rate of the communication network has to be high enough for fast closed-loop controls. Otherwise, the control bandwidth has to be decreased by increasing the period of control cycle to ensure that all the tasks can be executed within each control cycle [12].

In this paper, a novel distributed control architecture for an MMC system is proposed, in order to make the signals and data transmission required by real-time controls independent of the number of sub-modules in the MMC while all control objectives are properly achieved. This control architecture still consists of a central controller and local controllers. Only arm current measurements, output power control, and system level protection are implemented in the central controller. The local controllers take care of the internal dynamics controls, i.e. complete sub-module capacitor voltage control and differential current regulation, PWM generation, and local protection. Capacitor voltage control loops are elaborately designed so that the individual sub-module capacitor voltage can be properly governed without knowing the capacitor voltages in other sub-modules. By adopting the capacitor voltage control proposed in this paper, no capacitor voltage transmission through the communication network is required in each control cycle. Therefore, the information exchanging among central and local controllers is significantly decreased, which greatly reduces the communication burden and the baud rate requirement of the communication network. The modularity and expandability of the MMC are also improved as the software development for the proposed distributed control strategy can be more modularized and simpler for implementation, compared to existing distributed control strategies. All the control loops are analyzed and the controller parameters are designed with the consideration of system stability. The disturbances introduced by other sub-modules are taken into account while analyzing the stability of the individual average capacitor voltage control loop. The proposed distributed control strategy is applicable even the carrier frequency is around 100 Hz. The effectiveness of the proposed distributed control strategy is verified experimentally on an MMC prototype in the laboratory. The experimental results confirm that the MMC operates properly and stably under the proposed distributed control strategy in the start-up, steady state and step change operations.

II. Proposed Distributed Control Strategy and Implementation

The structure of the proposed distributed control strategy for the MMC is illustrated in Fig. 2, where the control tasks are assigned to different controllers, i.e. a central controller and local controllers located in sub-modules. The central controller mainly coordinates and manages the overall operation of the MMC, while each local controller deals with the internal dynamics and immediate protection of the corresponding sub-module. With the local controllers and the proposed distributed control, the MMC sub-modules can be more modularized in terms of software implementation. Necessary information is exchanged between the central and local controllers through a communication network. The complexity of implementing and managing a communication-based distributed control strategy is reduced, making it convenient to be extended to MMCs with a higher number of sub-modules.

A. Allocation of control tasks

System level control tasks are assigned to the central controller to coordinate the operation of the MMC at a higher level. The output power and current controls are implemented in the central controller with measured arm currents, DC bus and load/grid voltages within each control cycle. The capacitor voltage level and the power balance between the DC and AC

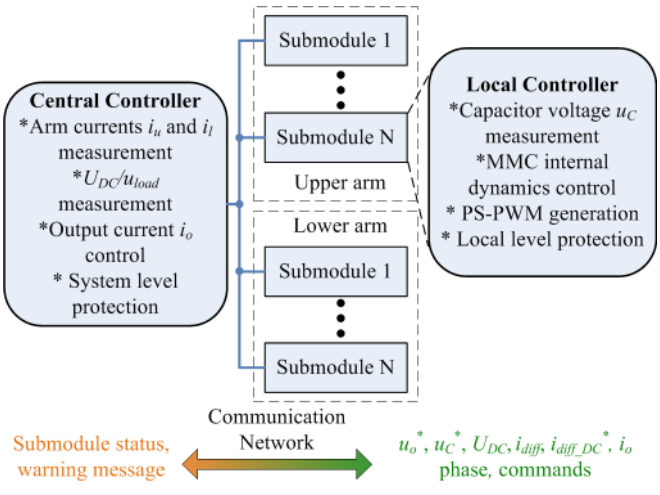


Fig. 2. Proposed distributed control structure for MMCs.

sides of the MMC are also considered in the central controller. System level protections, such as monitoring the sub-module status, are implemented in the central controller as well.

The most significant improvement of the proposed control strategy is that the internal dynamics control loops, including average capacitor voltage control, differential current regulation, and capacitor voltage balancing, are completely distributed into local controllers, without knowing the capacitor voltages in other sub-modules that are necessary for conventional control strategies. Such a distributed control with only local information will greatly reduce the communication loads within each control cycle and the time required for communication. Each local controller measures the capacitor voltage of the corresponding sub-module at each sampling instance for the distributed voltage control tasks. Sub-module protections, e.g. over-voltage, under-voltage and fault protections [17], are implemented in local controllers to protect the sub-modules immediately once abnormal conditions of the sub-modules are detected. The gating signals for switching devices in each sub-module are generated by the corresponding local controller based on individual modulation signal.

The comparison of the control tasks allocation and the signals required for real-time controls in the existing and proposed distributed control strategies are visually presented in Fig. 3, where the sub-modules in the upper and lower arms in the same phase leg are simply labeled as SM_1 to SM_{2N} for convenience. The dashed arrowed lines in Fig. 3 represent the signals transmitted through the communication network for real-time control. The number of signals for each arrowed line is directly marked in Fig. 3. As shown in Fig. 3 (b), the internal dynamics controls, including capacitor voltage controls and differential current regulation, are completely assigned to local controllers in the proposed strategy. Only two signals (u_C^* and u_{Ck}) are required by the capacitor average voltage control in the local controller in Fig. 3 (b), while $2N$+1 signals (u_C^* and u_{C1} ~ u_{C2N}) are needed in existing distributed control strategies. Therefore, the number of signals required by the capacitor average voltage control in the proposed strategy is significantly reduced and no longer depends on the number of sub-modules. The capacitor voltage transmission is not necessary for real-time control in the proposed control strategy, which is beneficial to the control system implementation and the communication network design.

B. *PS-PWM and synchronization*

The phase-shifted PWM (PS-PWM) scheme [27-29] is adopted for the proposed distributed control. A phase-shifted triangular carrier is generated in each local controller. The phase displacements of triangular carriers are calculated based on the number of sub-modules in each arm and assigned to the local controllers when the MMC is initialized after powering up. However, such phase displacements will possibly shift due to the difference of internal oscillators of the local controllers from the manufacturing tolerances, which leads to the distorted output voltage waveform. Therefore, all the local controllers have to be synchronized to the time base of the central controller to generate the desired PS-PWM signals. Since the PWM carrier synchronization is not the main focus of this paper, a similar method as introduced in [30, 31] can be adopted. A synchronization pulse or command is sent by the central controller every a certain period of time to re-synchronize PWM carriers of local controllers.

C. *Tasks execution sequence and communication*

The task execution time sequences of the proposed and existing distributed control strategies are presented in Fig. 4, where it can be seen that the most significant difference between these two strategies is the capacitor voltage transmission through the communication network. In existing distributed control, the communication bus and the execution time of the central controller would be mostly occupied by the

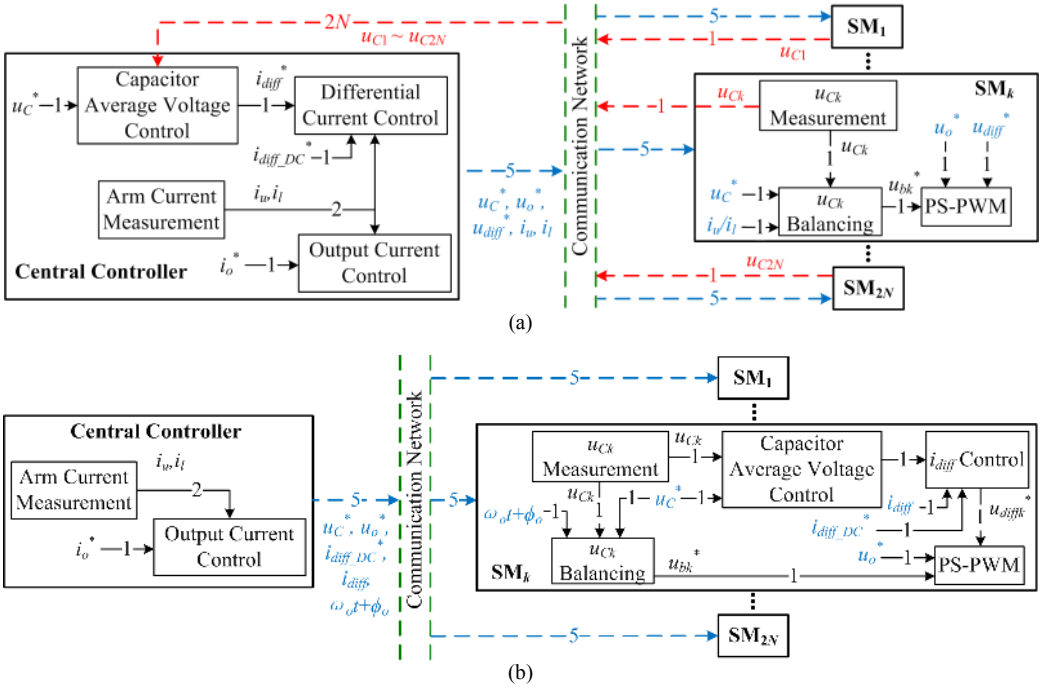


Fig. 3. Signals required by the MMC real-time controls: (a) Existing distributed control strategy; (b) Proposed distributed control strategy.

capacitor voltage updating, especially when a large number of sub-modules are employed in the MMC system. In other words, the communication burden is approximately proportional to the number of sub-modules. Consequently, a trade-off between the control bandwidth (switching and sampling frequency) and the communication network baud rate is required due to the large communication load and delays caused by the communication.

On the other hand, no capacitor voltages transmission is required in each control cycle for the proposed control, and the execution burden is independent of the number of sub-modules. The communication network as well as the controllers are in the idle state in most of the time in each control cycle and can be used for other tasks such as system status monitoring and protection. At the beginning of each control cycle, a start message (St) is sent by the central controller (CC) to synchronize and trigger the analog-to-digital conversion (ADC) of local controllers (LCs). After the measurements, the central controller calculates the references and sends the information required to local controllers. With received data, the local controllers perform the MMC internal dynamics controls and generate the gating signals for switching devices based on calculated modulation index and PS-PWM scheme.

The communication messages are designed accordingly to execute the tasks shown in Fig. 4 (b) with minimum information exchanging for real-time control with relatively high bandwidth. The output voltage reference u_o^*, the capacitor voltage reference u_C^*, $i_{diff\_DC}^*$, output current phase angle and differential current are required in each control cycle and shared by all local controllers in the same phase leg. One message containing those data, which conveys adequate information for the real-time control in local controllers, can be broadcasted by the central controller through the communication network in each control cycle. Some other messages are designed for the overall operation of the MMC as well. The synchronization message is broadcasted by the central controller every NT_s seconds, where T_s is the sampling interval. After receiving the synchronization message, local controllers reset their carrier phase angles to the initial values. Each sub-module updates its status and capacitor voltage by request for system monitoring and status display purposes. If there is any abnormal sub-module status detected by the corresponding local controller, the necessary protection actions, e.g. bypassing the faulty sub-module, can be executed locally and a warning message with the fault code is immediately sent out to inform the central controller for further decision making.

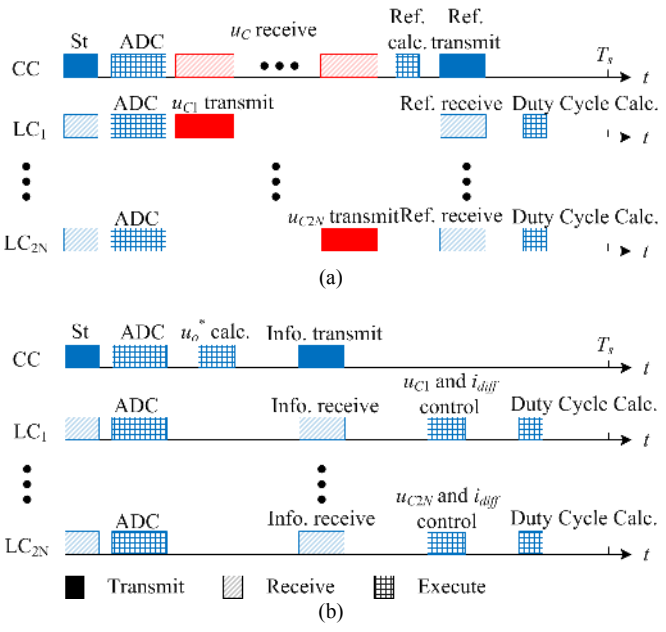


Fig. 4. Time sequence of tasks in each control cycle of: (a) Existing distributed control; (b) Proposed distributed control.

III. Distributed Control Loops Design and Analysis

A. Mathematical model of the MMC

The basic structure and operation principles of an MMC have been extensively explained in the literature [6, 8, 32] and will not be discussed in this paper. A single-phase MMC based inverter system shown in Fig. 5 is adopted in this paper to demonstrate the proposed distributed control strategy. This distributed control is applicable in three-phase grid-connected cases with modified output current controls in the central controller and the same internal dynamics controls in local controllers. There are N sub-modules connected in series in the upper and lower arms respectively. Each arm is equipped with an arm inductor L_{arm}. An equivalent resistor R_{arm} is employed in each arm to represent the losses on the semiconductors, equivalent series resistance (ESR) in C_{SM} and L_{arm}, etc. The output terminals of the MMC, which are located at the middle points of the two arms and DC bus capacitors, are connected to the load represented by a voltage source u_{load} via an inductor L_o.

If the output voltage and current of the MMC are well regulated, they can be expressed as

$$\begin{cases} u_o = U_o \sin(\omega_o t) \\ i_o = I_o \sin(\omega_o t + \phi_o) \end{cases} \tag{1}$$

where U_o and I_o are the amplitudes of u_o and i_o respectively, ω_o refers to the fundamental angular frequency in radian per second, and ϕ_o stands for the phase displacement between the output voltage and current. The differential current in the phase leg is defined as

$$i_{diff} = I_{DC} + i_{cir} \tag{2}$$

where I_{DC} is a DC current that maintains the power balance between the DC and AC sides of the MMC [2], and i_{cir} is the circulating current ripple which is dominated by the 2nd order harmonic [5, 6, 33]. Assuming the harmonics in the differential current have been completely suppressed as in [28, 33, 34], the

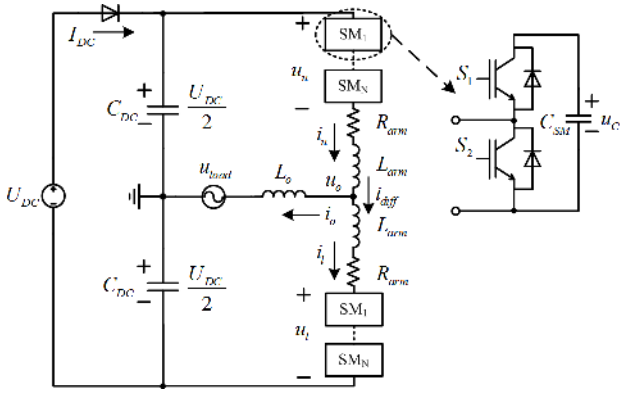


Fig. 5. Structure of a single phase MMC based inverter.

arm currents can be written as

$$\begin{cases} i_u = I_{DC} + \dfrac{i_o}{2} \\ i_l = I_{DC} - \dfrac{i_o}{2} \end{cases} \tag{3}$$

Without considering the capacitor voltage unbalance and any additional capacitor voltage control, the normalized modulation index of the k^{th} sub-module in the upper and lower arms can be obtained as

$$\begin{cases} n_{uk} = \dfrac{1}{2} - \dfrac{u_o^*}{2} - u_{diff}^* \\ n_{lk} = \dfrac{1}{2} + \dfrac{u_o^*}{2} - u_{diff}^* \end{cases} \tag{4}$$

And

$$\begin{cases} u_o^* = \dfrac{2u_o}{U_{DC}} \\ u_{diff}^* = \dfrac{U_{diff\_DC} + U_{diff\_2}\sin(2\omega_o t + \phi_{diff\_2})}{U_{DC}} \end{cases} \tag{5}$$

where U_{diff_DC} is a DC voltage to induce I_{DC}, and $U_{diff\_2}\sin(2\omega_o t + \phi_{diff\_2})$ is the voltage utilized to suppress the second-order harmonics in the differential current [35]. According to the analysis in [2], the capacitor voltage of the k^{th} sub-module in the upper and lower arms can be written as

$$\begin{cases} u_{Cuk} = U_C + U_{C\_1}\sin(\omega_o t + \phi_{C\_1}) + U_{C\_2}\sin(2\omega_o t + \phi_o) \\ u_{Clk} = U_C - U_{C\_1}\sin(\omega_o t + \phi_{C\_1}) + U_{C\_2}\sin(2\omega_o t + \phi_o) \end{cases} \tag{6}$$

where U_C denotes the average voltage across the sub-module capacitor, $U_{C\_1}\sin(\omega_o t + \phi_{C\_1})$ and $U_{C\_2}\sin(2\omega_o t + \phi_o)$ represent the voltage ripples with fundamental and second-order frequencies respectively.

B. Control loops in the central controller

Output power control of the MMC is implemented in the central controller. The reference of the output current i_o^* can be calculated according to the output power commands. The measured load voltage and i_o are used to calculate $i_{diff\_DC}^*$ for the power balance between the DC and AC sides of the MMC. The reference of the sub-module capacitor voltage u_C^* can be obtained according to the DC bus voltage and the operational requirements of the MMC, e.g. in normal operation $u_C^* = U_{DC}/N$, during the start-up process or the average capacitor voltage is intentionally varied in the application discussed in [2]. Since a single-phase MMC system is considered in this paper, a proportional-resonant (PR) controller is adopted to regulate the output current according to the power demands. The z-domain

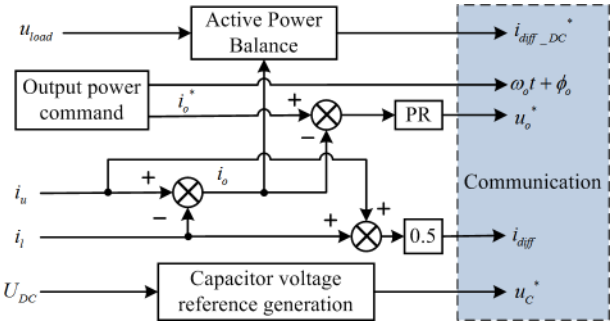


Fig. 6. Block diagram of the central controller.

transfer function of the PR controller is expressed as

$$G_{PR\_i_o}(z) = K_{P\_i_o} + \frac{2K_{R\_i_o}\omega_c T_s (z-1)}{z^2 + z\left(\omega_o^2 T_s^2 + 2\omega_o T_s - 2\right) - 2\omega_c T_s + 1} \tag{7}$$

where K_{P_io} and K_{R_io} are the proportional and resonant gains respectively, and ω_c is the resonant cut-off frequency [36]. The outputs of the central controller are passed to local controllers through the communication network.

C. Control loops distributed in local controllers

The internal dynamics of the MMC, i.e. the differential current and capacitor voltage are controlled locally in individual sub-module to implement the distributed control strategy in a more modularized manner. The block diagram of the control loops in the k^{th} local controller is shown in Fig. 7.

1) Differential current control loop:

As shown in Fig. 7, the reference of the inner differential current i_{diff}^* is mainly obtained from the capacitor voltage control and the active power balancing. The DC side current reference for power balancing is set to be $i_{diff\_DC}^* = U_o I_o \cos(\varphi_o)/(2U_{DC})$. The output of the voltage control loop, which is, ideally, a DC component as well, is regarded as the other part of the differential current reference. In this paper, a PR controller coping with the signal at the second-order frequency is employed to suppress the circulating ripple current i_{cir}. In some specific applications such as capacitor voltage ripple shaping [37, 38] and motor drives in low-frequency operations [35, 39, 40], another AC term, e.g. second-order harmonics, can be added into i_{diff}^* to inject the circulating ripple current by purpose. In these cases, the PR controller is also capable of regulating the circulating current according to its reference.

$$G_{PR\_i_{diff}} = K_{P\_i_{diff}} + \frac{2K_{R\_i_{diff}}\omega_c T_s (z-1)}{z^2 + z(4\omega_o^2 T_s^2 + 2\omega_c T_s - 2) - 2\omega_c T_s + 1} \tag{8}$$

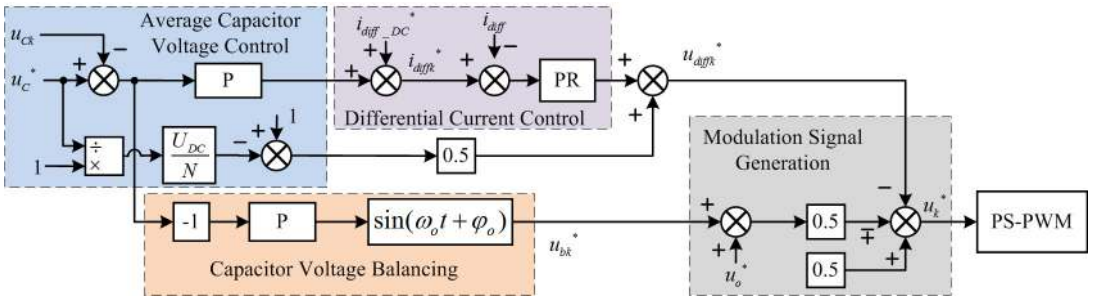


Fig. 7. Block diagram of the local controller.

2) Sub-module capacitor voltage control:

The control of sub-module capacitor voltage of the MMC is an important and unavoidable task that attracts a lot of research interests [8, 21-24]. As introduced in Section II.A, the task of capacitor voltage governing is completely distributed to local controllers with very limited information, while all the control objectives in conventional control strategies have to be still achieved. Different voltage control loops have to be particularly designed for sub-module capacitor voltage averaging and balancing. Taking the k^{th} sub-module in the upper arm as an example, the power flows through the capacitor can be calculated according to (1) – (6), as

$$P_{Cuk} = u_{Cuk} n_{uk} i_u = \overline{P}_{Cuk} + \text{AC terms} \tag{9}$$

Note that only the average power (DC components) in P_{Cuk} contributes to the capacitor voltage shifting, such average power can be used to adjust the average voltage across sub-module capacitors. The average power of the sub-module capacitor can be obtained as in (10).

a) Average capacitor voltage control:

This loop aims to control the average voltage in each sub-module according to the reference u_C^* given by the central controller. In conventional capacitor voltage averaging strategies [7-9], the average voltage in one phase leg is controlled with the help of a DC component in the differential current induced by U_{diff_DC}, with the awareness of the capacitor voltages in all sub-modules. In the proposed structure, the capacitor voltage might be easily unstable by simply distributing the PI controller used in conventional voltage controls into local controllers, due to the control conflict among different sub-modules in one phase leg. Therefore, a new voltage control strategy is designed to maintain the mean value of the capacitor voltage in each sub-module.

As analyzed in [41], the average capacitor voltage is usually selected as $u_C = U_{DC}/N$ in most applications, by simultaneously inserting N sub-modules into one phase leg, for the sake of the capability to generate the maximum output voltage. In fact, such average capacitor voltage in one phase leg can be, ideally, regulated as U_{DC}/N_{eq} by changing the equivalent number of sub-modules inserted into the phase leg N_{eq}. The average voltage control loop is illustrated in Fig. 7, where the equilibrium average capacitor voltage is U_{DC}/N and a feedforward path is designed to implement the average voltage control by adjusting N_{eq}. The proposed feedforward path can be expressed as

$$G_{feedfwd} = \frac{1}{2}\left(1 - \frac{U_{DC}}{N u_C^*}\right) \tag{11}$$

where the coefficient 1/2 is adopted because the equivalent numbers of sub-modules inserted in the upper and lower arms are equally adjusted. In addition, a proportional (P) controller is employed to fine-tune the average capacitor voltage in individual sub-module and compensate the voltage deviation caused by losses, etc. This P controller is disabled whenever i_o^* is zero, and the sub-module capacitor average voltage is then only regulated by the feedforward path in this case.

b) Capacitor voltage balancing:

The voltage control strategy introduced in the previous subsection cannot guarantee the capacitor voltage balance during the operation of the MMC, which might lead to the instability of the overall system. Since the DC side current I_{DC} will affect all sub-module capacitor voltages in the phase leg, the AC side active power is utilized to control the individual sub-module capacitor voltage. An AC component with fundamental frequency is intentionally added to the modulation signal of individual sub-module to generate a controllable active power. The modulation signals are modified as

$$\begin{cases} n_{uk} = \dfrac{1}{2} - \dfrac{u_o^* + u_{buk}^*}{2} - u_{diffuk}^* \\ n_{lk} = \dfrac{1}{2} + \dfrac{u_o^* + u_{blk}^*}{2} - u_{difflk}^* \end{cases} \tag{12}$$

where u_{buk}^* and u_{blk}^* are the capacitor voltage balancing signals for the k^{th} sub-module in the upper and lower arms respectively. $u_{diffuk}^* = u_{difflk}^*$ is assumed in the analysis. Taking the upper arm as an example, u_{buk}^* can be expressed as

$$u_{buk}^* = U_{buk}^* \sin(\omega_o t + \phi_b) \tag{13}$$

The average power of the k^{th} sub-module capacitor in the upper arm is derived according to (1), (3), (5), (6) and (12) as in (14), where the last three terms on the right-hand side are introduced by the capacitor balancing strategy. Among them, $U_C I_o U_{buk}^* \cos(\phi_b - \phi_o)/8$ is obviously the most dominant term since the average voltage across the sub-module capacitor is normally much larger compared to the amplitudes of voltage ripples. Therefore, the capacitor balancing loop is most effective if $\phi_b = \phi_o$ is selected. As illustrated in Fig. 7, the amplitude of u_{buk}^* is generated by a P controller according to the capacitor voltage tracking error. The output of the P controller is multiplied by $\sin(\omega_o t + \phi_o)$ to generate u_{buk}^* having the same phase angle as the output current. $u_{buk}^* = 0$ if the output current is set to be zero, which is reasonable as the sub-module capacitor voltages are generally stable if there is no power drawn from the MMC by the loads.

3) Modulation signals generation:

The outputs of the controllers for the MMC output current and internal dynamics regulation are combined based on (12) to generate the modulation signals for each sub-module, as shown in Fig. 7. The PS-PWM scheme is adopted to generate the

$$\begin{aligned} \overline{P}_{Cuk} = & \left[\frac{U_C}{2} - \frac{U_o U_{C\_1}\cos(\phi_{C\_1})}{2U_{DC}} - \frac{U_{C\_2}U_{diff\_2}\cos(\phi_o - \phi_{diff\_2})}{2U_{DC}} - \frac{U_{diff\_DC}U_C}{U_{DC}}\right] I_{DC} \\ & - \left[\frac{U_C U_o \cos(\phi_o)}{U_{DC}} - \left(\frac{1}{2} - \frac{U_{diff\_DC}}{U_{DC}}\right) U_{C\_1}\cos(\phi_o - \phi_{C\_1}) - \frac{U_{C\_1}U_{diff\_2}\sin(\phi_{diff\_2} - \phi_{C\_1} - \phi_o)}{2U_{DC}}\right]\frac{I_o}{4} \end{aligned} \tag{10}$$

$$\overline{P}_{Cuk} = \text{Equation (10)} - \left[\frac{U_C I_o \cos(\phi_b - \phi_o)}{8} + \frac{U_{C\_1} I_{DC}\cos(\phi_{C\_1} - \phi_b)}{4} + \frac{U_{C\_2} I_o \sin(\phi_b)}{16}\right] U_{buk}^* \tag{14}$$

TABLE I. PARAMETERS OF THE MMC SYSTEM

Parameters	Values
DC bus voltage: U_{DC}	240 V
DC bus capacitance: C_{DC}	4.4 mF
Output inductance: L_o	0.7 mH
Load Resistance: R_l	10 Ω
Rated output frequency: f_o	50 Hz
No. of SM in each arm: N	3
Arm inductance: L_{arm}	5 mH
Arm resistance: R_{arm}	0.025 Ω
SM capacitance: C_{SM}	940 uF
Carrier frequency: f_c	2 kHz

gating signals for switching devices, as introduced in Section II.B.

IV. Case Study and Controller Parameters Design

The key parameters of the single phase MMC system shown in Fig. 5 are listed in TABLE I. Three sub-modules are connected in series in each arm. As the equivalent switching frequency of the MMC is $6f_c$ = 12 kHz [8, 27, 28], the sampling frequency is designed to be f_s = 12 kHz and the control system is synchronized with it, having a period of $T_s = 1/f_s$. The resistor R_l and inductance L_o are regarded as an inductive-resistive load for the MMC in this paper.

A. Phase-shifted PWM implementation and digital control system delay analysis

The phase-shifted PWM scheme for the MMC is implemented in local controllers, whose principle is illustrated in Fig. 8. Three triangular carriers $c1$, $c2$ and $c3$ are respectively generated in the three local controllers in the same arm. The phase angles of the carriers are shifted by $2\pi/3$ radian from each other. The carriers in the upper and lower arms have the same phase angles to generate $2N+1$ output voltage levels when N is an odd number [27, 28]. All the sampling instances are synchronized based on the message sent from the central controller in every control cycle. The duty cycle of each sub-module is updated at the instances that the corresponding carrier reaches the period and zero. Note that the output and differential currents can be adjusted by switching action of any sub-module in the same phase leg so that the equivalent switching frequency of the current control loops is correspondingly $f_s = 2Nf_c$. Equivalently, the current measurements are executed at each sampling instance and the duty cycles calculated based on these measurements for current regulation are updated at the next sampling instance, which introduces T_s seconds computational delay. In addition, the PWM can be regarded as a Zero-Order-Holder (ZOH) for the reference and will introduce $0.5T_s$ PWM delay into the current control loops [36, 42]. Therefore, 1.5 T_s digital control delay exists in current control loops.

In contrast, the digital control delay in the capacitor voltage control loops is different from that of the current control loops, since the capacitor voltage is adjusted by the local controller and switching actions in individual sub-module. Taking sub-module 1 as an example, the time sequence for the voltage control is illustrated in Fig. 9. The capacitor voltage is sampled at the $(3k-1)^{th}$ sampling instance and the corresponding reference is calculated in this sampling interval. At the next sampling instance (the k^{th} duty cycle updating instance of sub-module 1 as well), the reference calculated in the last sampling interval is used to update the duty cycle of sub-module 1. The updated duty cycle will be held for the next three sampling intervals ($3T_s$) and an average $1.5T_s$ PWM delay is consequently introduced due to the equivalent ZOH with a sampling period of $3T_s$. Thus, a total $2.5T_s$ digital control delay has to be taken into account while designing the capacitor voltage control loop.

B. Current control loops analysis and parameters design

According to the discussion in Section III, the output and differential current control loops can be depicted in Fig. 10, where the sampling frequencies of all samplers are set to be f_s = 12 kHz. The open-loop transfer functions of these two current control loops can be derived according to the block diagrams in Fig. 10, as

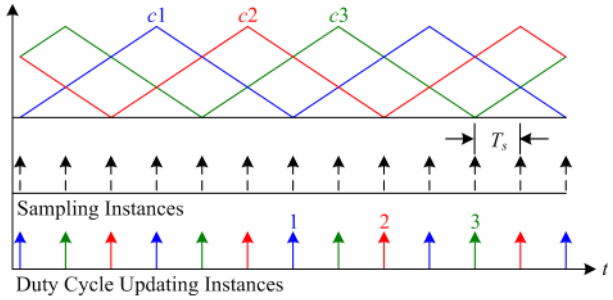


Fig. 8. Phase-shifted PWM scheme.

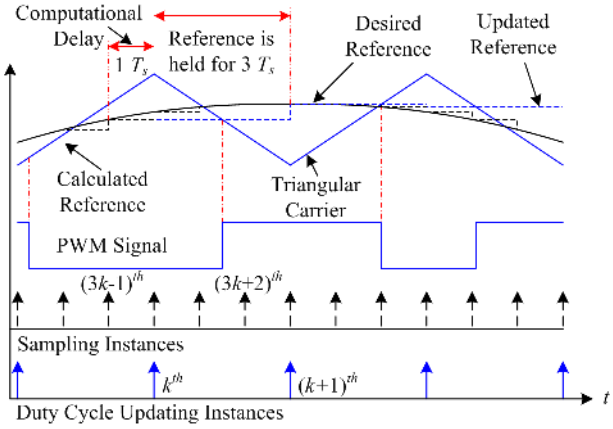


Fig. 9. Illustration of the digital control delay in voltage control loops.

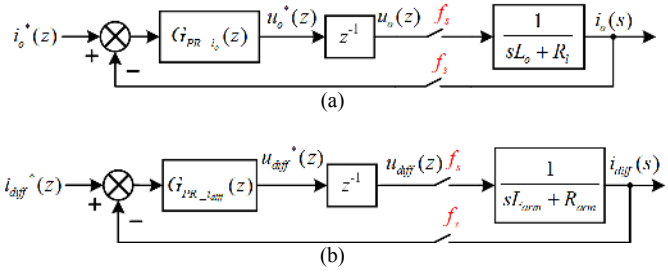
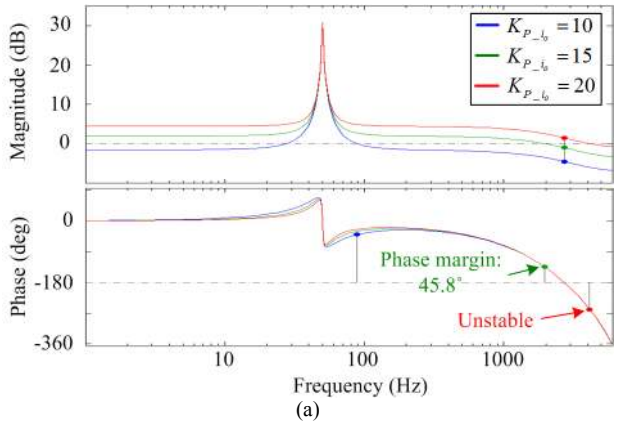
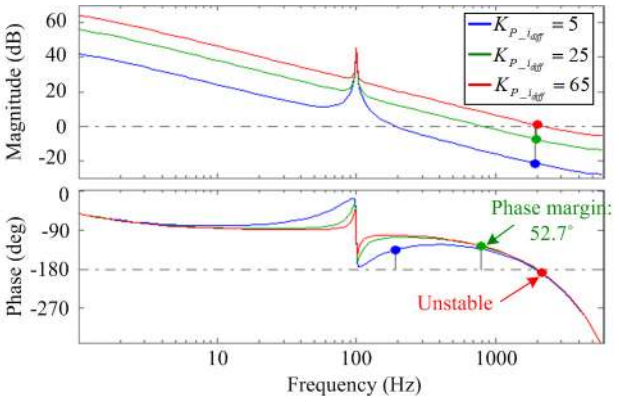


Fig. 10. Block diagrams of: (a) Output current control loop; (b) Differential current control loop.



(a)



(b)

Fig. 11. Bode diagrams of: (a) Output current control loop with different K_{P_io}; (b) Differential current control loop with different K_{P_idiff}.

$$\begin{cases} G_{i_o\_op}(z) = G_{PR\_i_o}(z) z^{-1} Z_{ZOH}\left(\dfrac{1}{sL_o + R_l}\right) \\ G_{i_{diff}\_op}(z) = G_{PR\_i_{diff}}(z) z^{-1} Z_{ZOH}\left(\dfrac{1}{sL_{arm} + R_{arm}}\right) \end{cases} \tag{15}$$

In practice, a minimum phase margin of 45° is required to ensure the stability of a feedback control system [43]. The Bode diagrams of G_{io_op}(z) shown in Fig. 11 (a) indicate that K_{P_io}=15 provides relatively high open-loop controller gain with a phase margin of 45.8°, which guarantees the fast response and the stability of the output current control loop. The resonant gain K_{R_io} is set to be 400 to obtain a high magnitude peak at the fundamental frequency 50 Hz, providing satisfactory output current regulation. Similarly, proportional gain of G_{io_op}(z) can be selected as K_{P_idiff} = 25 with the consideration of excellent current regulation and system stability (phase margin 52.8°). The resonant gain is set to be 500 to compensate the second-order harmonics at 100 Hz.

C. Average capacitor voltage control loop analysis and parameters design

The average capacitor voltage control block diagram for the k^{th} sub-module, which can be derived according to Fig. 7, is shown in Fig. 12 (a). The sampling frequency for voltage and current quantities measurements is f_s while the sampling frequency of the sampler representing the PWM action is f_c. Note that the references i_{diffk}^* and u_{diffk}^* of the k^{th} sub-module are different from the ones in other sub-modules because of the individual average capacitor voltage control. There might be control conflicts among sub-modules, e.g. one sub-module requires higher differential current to increase its capacitor voltage while another sub-module is trying to reduce the current to decrease its own capacitor voltage. Such control conflicts from other sub-modules are modeled as voltage disturbances $D(s)$ to the capacitor voltage of sub-module k, as shown in Fig. 12 (a). The MAF(z) term stands for a moving average filter with a 0.02-second time window, whose z-domain transfer function can be denoted as

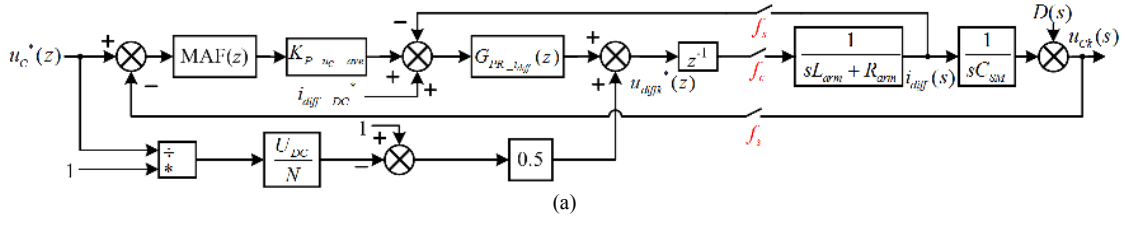
$$\mathrm{MAF}(z) = \frac{1 + z^{-1} + \cdots + z^{1-0.02/T_s}}{0.02/T_s} \tag{16}$$

Since u_C^* and $i_{diff\_DC}^*$ are generally set to be constant in the steady state operation, the feedforward path for the average voltage control, as well as the $i_{diff\_DC}^*$ term, are ignored while designing the proportional controller gain $K_{P\_uC\_ave}$, as shown in Fig. 12 (b). $G_{idiff\_cl}(z)$ refers to the closed-loop transfer function for differential current regulation, which can be written as

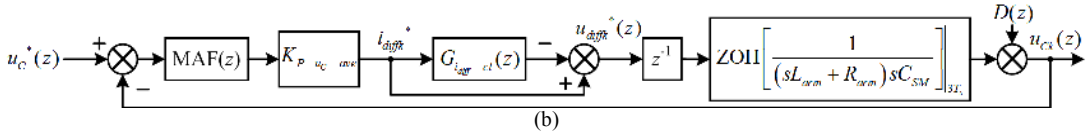
$$G_{i_{diff}\_cl}(z) = \frac{G_{i_{diff}\_op}(z)}{1 + G_{i_{diff}\_op}(z)} \tag{17}$$

The plant of the average capacitor voltage control loop is discretized by a ZOH with a sampling interval of $3T_s$. As aforementioned, such ZOH will introduce a $1.5T_s$ seconds delay into the voltage control loop. The open-loop transfer function derived from Fig. 12 (b) is expressed as

$$G_{u_C\_ave\_op}(z) = \mathrm{MAF}(z) K_{P\_u_C\_ave} (1 - G_{i_{diff}\_cl}(z)) z^{-1} \times \mathrm{ZOH}\left[\frac{1}{(sL_{arm} + R_{arm})\, sC_{SM}}\right]_{3T_s} \tag{18}$$



(a)



(b)

Fig. 12. Block diagrams for the average voltage control: (a) Actual block diagram; (b) Simplified block diagram in z-domain.

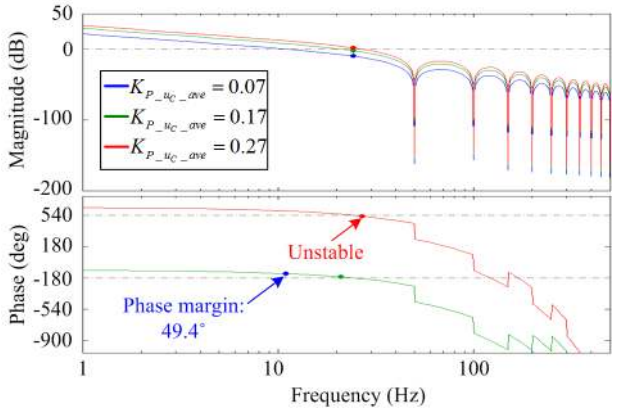


Fig. 13. Bode diagram of $G_{uC\_ave\_op}(z)$.

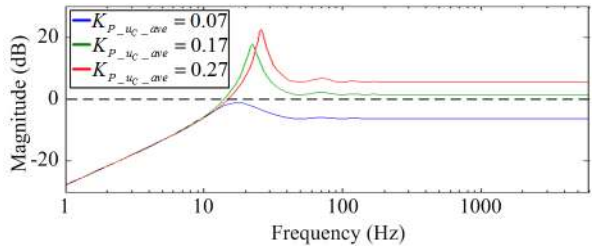


Fig. 14. Magnitude-frequency characteristics of the right-hand side of inequality (21).

The proportional gain of the average voltage control loop is selected as $K_{P\_uC\_ave}$ = 0.07 for a phase margin of 49.4°. It should be noted that the control conflict among different sub-modules in the same phase leg has to be taken into account to ensure the overall system stability. The disturbances introduced by control loops in other sub-modules to the capacitor voltage of the k^{th} sub-module can be derived as

$$D_k(z) = \frac{\sum_{i\neq k}^{N}(u_C^{\ *} - u_{Ci})K_{P\_u_C\_ave}K_{P\_i_{diff}}}{2N^2} \leq \frac{(N-1)K_{P\_u_C\_ave}K_{P\_i_{diff}}\max(|e_{u_{Ci}}|)}{2N^2} \tag{19}$$

where e_{uCi} is the error of the capacitor voltage in the i^{th} sub-module that is one of the N sub-modules inserted in the MMC. The closed-loop transfer function from $D_k(z)$ to u_{Ck} can be derived as

$$\frac{u_{Ck}}{D_k(z)} = \frac{1}{1+G_{u_C\_ave\_op}(z)} \tag{20}$$

Substituting (19) into (20)

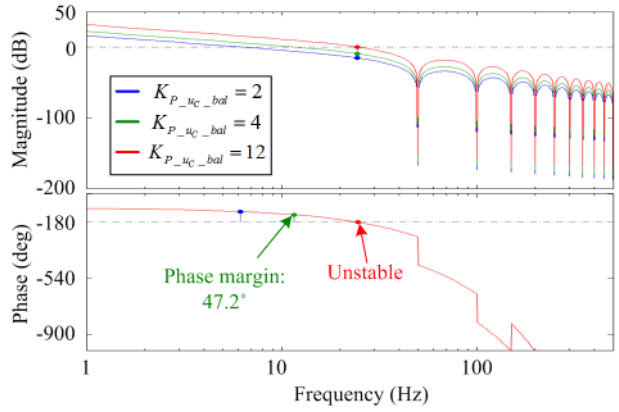


Fig. 17. Bode diagram of the open-loop transfer function of the capacitor voltage balancing loop.

$$\frac{u_{Ck}}{\max(|e_{u_{Ci}}|)} \leq \frac{(N-1)K_{P\_u_C\_ave}K_{P\_i_{diff}}}{2N^2\left[1+G_{u_C\_ave\_op}(z)\right]} \tag{21}$$

The bode diagram of (21) depicted in Fig. 14 shows that the disturbances can be well damped if $K_{P\_uC\_ave}$ = 0.07 is selected, since the magnitude characteristics of the right-hand side of equation (21) are always below 0 dB at all frequencies.

D. Capacitor voltage balancing control loop analysis and parameters design

Ignoring the voltage ripples across the sub-module capacitor, the block diagram of the capacitor voltage balancing loop for the k^{th} sub-module discussed in Section III.C can be found in Fig. 15, where the signs of terms containing $\sin(\omega_o t + \phi_o)$ are '–' for sub-modules in the upper arm and '+' for sub-modules in the lower arm. According to the previous analysis, only the DC components in the capacitor current i_C contribute to the shifting of the capacitor voltage, while the AC terms in i_C introduce voltage ripples across the capacitor. Consequently, the block diagram of the capacitor voltage balancing loop can be simplified as in Fig. 16, where U_{bk}^{*} refers to the amplitude of u_{bk}^{*}, I_{Ck} and U_{Ck} stand for the DC components of the capacitor current and voltage respectively.

It should be noted that the gain of the capacitor voltage balancing loop is proportional to the amplitude of the output current I_o, and higher I_o leads to less phase margin for the system stability with the same $K_{P\_uC\_bal}$. Therefore, the controller gain is designed under the condition that the MMC is operated with its designed maximum output current, i.e. I_o = 12 A. Based on the Bode diagram shown in Fig. 17, $K_{P\_uC\_bal}$ = 4 is accordingly selected for sufficient phase margin in the entire operation range of the MMC.

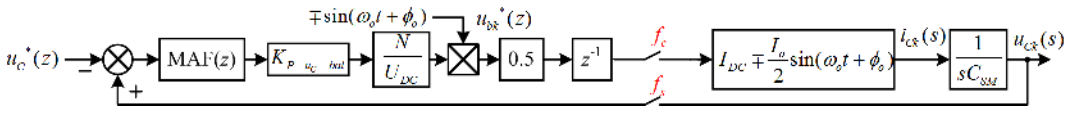


Fig. 15. Block diagram of capacitor voltage balancing loop.

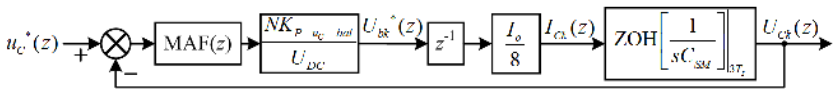


Fig. 16. Simplified block diagram of capacitor voltage balancing loop.

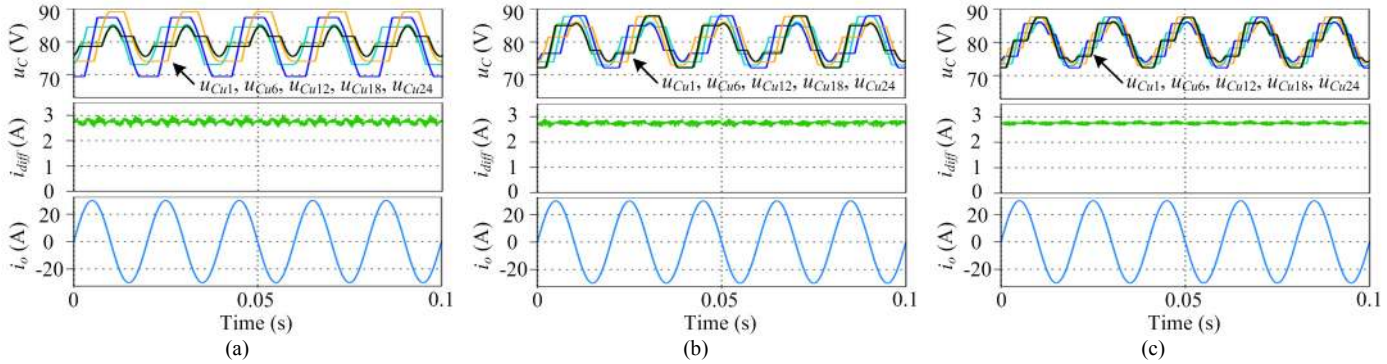


Fig. 18. Simulated waveforms of the MMC with different carrier frequencies: (a) f_c = 100 Hz; (b) f_c = 125 Hz; (c) f_c = 175 Hz.

E. Effectiveness of the proposed distributed control strategy with low carrier frequency

The carrier frequency f_c = 2 kHz is adopted in the case study to achieve a higher equivalent switching frequency with three sub-modules in each arm. In fact, the switching frequency of the semiconductors can be as low as around 100 Hz [25, 44] in MMCs with a large number of sub-modules in high power applications. Therefore, the effectiveness of the proposed control loops with low carrier frequencies around 100 Hz is investigated in the Piecewise Linear Electrical Circuit Simulation (PLECS) software. 24 sub-modules are adopted in the simulation so that the equivalent switching frequency of the MMC is relatively high even with low carrier frequencies. The simulation results are presented in Fig. 18, where the waveforms of i_o and i_{diff} are scarcely affected by the low semiconductor switching frequencies. On the other hand, the capacitor voltage waveforms are significantly influenced if the carrier frequency is 100 Hz. Although the capacitor voltage is not perfectly balanced in Fig. 18 (a), all the capacitor voltages converge around the set point 80 V with limited ripples, which guarantees the stable operation of the MMC. The capacitor voltage waveforms are much improved and better balanced if the carrier frequency is increased to 125 Hz, and the capacitor voltages can be well balanced if the carrier frequency is 175 Hz, as illustrated in Fig. 18 (b) and (c). The simulation results confirm the effectiveness of the proposed distributed control when the sub-module carrier frequency is around 100 Hz.

V. Experimental Results

The performance of the MMC under the proposed distributed control strategy in steady state and transients are validated experimentally on the single-phase MMC inverter shown in Fig. 5, whose detailed parameters are listed in TABLE I.

A. MMC start-up process and voltage regulation with zero output current

The start-up process of the MMC is illustrated in following experiments to verify the effectiveness of the capacitor voltage regulation. The sub-module capacitor voltage should be automatically charged to, ideally, $U_{DC}/2N$ through the body diode of switching devices if the MMC is connected to the DC bus without any switching action. The sub-module capacitor voltages in the start-up process are depicted in Fig. 19. After activating the switching devices, the capacitor voltage is initially set to be 50 V and then ramp up to 80 V (U_{DC}/N) with a rate of 40 V/s until t1, which represents the end of the start-up process. It can be seen in the voltage curves in Fig. 19 that the capacitor voltage is unavoidably unbalanced due to the parameters difference among sub-module capacitors if no voltage balancing control is applied. After the start-up process, the capacitor voltage reference is intentionally set to be 88 V ($1.1U_{DC}/N$) and 72 V ($0.9U_{DC}/N$) respectively to demonstrate that the capacitor average voltage can be regulated according to the references.

B. Steady-state performance

The steady-state performance of the MMC under the proposed distributed control is presented in this set of

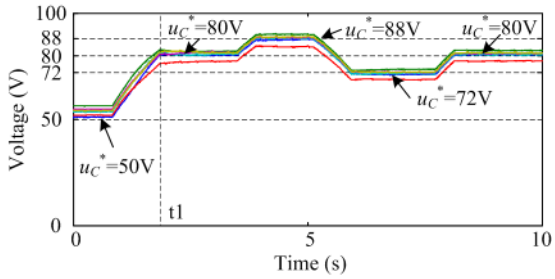


Fig. 19. Sub-module capacitor voltages during the MMC start-up process with zero output current.

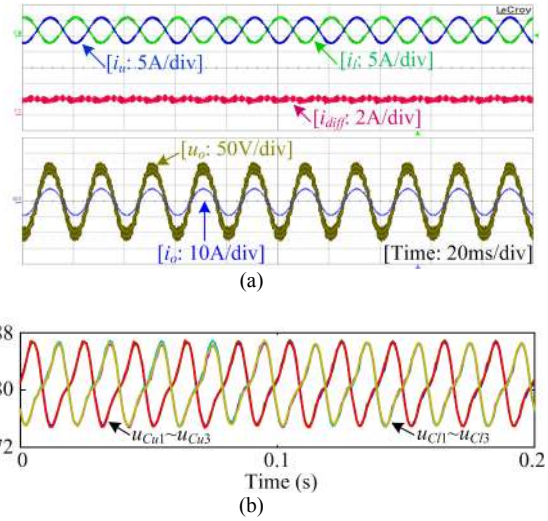


Fig. 20. Voltage and current waveforms of the MMC during the steady-state operation: (a) Arm currents, differential current, output voltage and current; (b) Capacitor voltages.

experiments. Fig. 20 shows the voltage and current waveforms of the MMC in steady-state operation, where the amplitude of the output current is set to be 9 A. A seven-level output voltage is generated and the output current tracks its reference accurately. The second-order harmonics in i_{diff} is effectively suppressed with the help of the resonant controller, leaving a DC component in the differential current with negligible ripples. Moreover, the sub-module capacitor voltages are well balanced by the proposed voltage control strategy. The system works stably under the distributed control in steady-state.

C. Dynamic response

The dynamic responses of the MMC during large current reference and capacitor average voltage reference step changes are studied in the following experiments. In the first set of experiments, the performance of the MMC under the proposed distributed control during output current step changes is evaluated. In Fig. 21, the output current of the MMC is initially set to be 3 A and then steps to 9 A at 0 s, while the waveforms when the output current changes from 9 A to 3 A are depicted in Fig. 22. The experimental results show that the MMC system is stable during large output current step changes. The output current tracks its reference rapidly with smooth transients and the DC component in the differential current is accordingly increased or decreased for the power balancing between the input and output sides of the MMC. The capacitor voltages shown in Fig. 21 (b) and Fig. 22 (b) converge to the set point 80 V during the output current step changes.

In the other set of experiments, the proposed control strategy is evaluated when there is a capacitor voltage reference step change. The voltage and current waveforms of the MMC are depicted in Fig. 23, where the capacitor voltage reference is changed from 70 V to 90 V at 0 s. After the capacitor voltage reference step change, the DC component of the differential current is increased to charge the capacitors according to the capacitor average voltage and differential current control loops. The capacitor voltages are well-balanced and the average voltage of all capacitors in the phase leg follows the reference within three fundamental periods without severe transients. The experimental results confirm the effectiveness of the proposed distributed control during capacitor voltage step changes.

D. Effectiveness of the capacitor voltage balancing

The effectiveness of the voltage balancing control loop is illustrated in this set of experiments, whose results are presented in Fig. 24. After the capacitor voltage balancing controller being disabled at 3 s, the capacitor voltages start to diverge from the set point 80 V. It can be seen that the capacitor voltages of sub-modules in the upper and lower arms are unequally distributed as well. The overall system tends to be unstable because of capacitor voltage divergence without the voltage balancing control loop. The capacitor voltages converge within about 0.1 s after the voltage balancing is enabled again at 5 s. During the entire process, no severe disturbance introduced by the unbalanced sub-module capacitor voltage is observed in the voltage and current waveforms of the MMC.

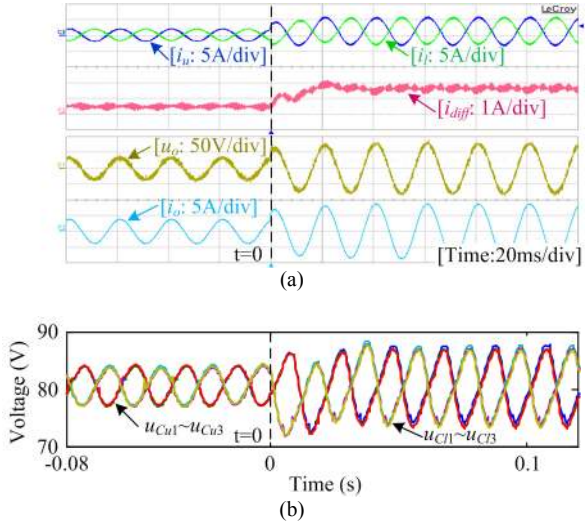


Fig. 21. Voltage and current waveforms of the MMC when i_o^* changes from 3 A to 9 A: (a) Arm currents, differential current, output voltage and current; (b) Capacitor voltages.

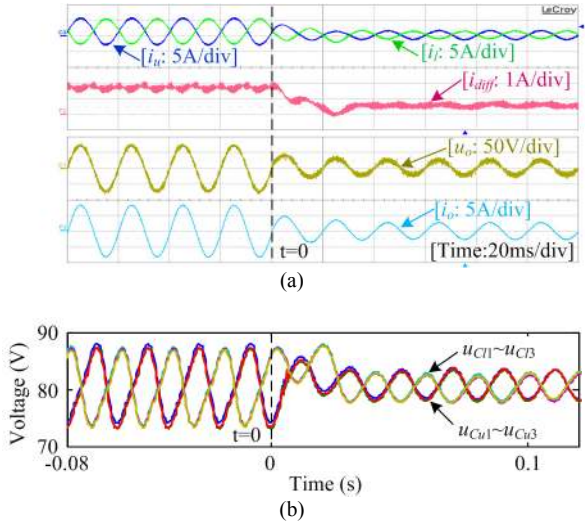


Fig. 22. Voltage and current waveforms of the MMC when i_o^* changes from 9 A to 3 A: (a) Arm currents, differential current, output voltage and current; (b) Capacitor voltages.

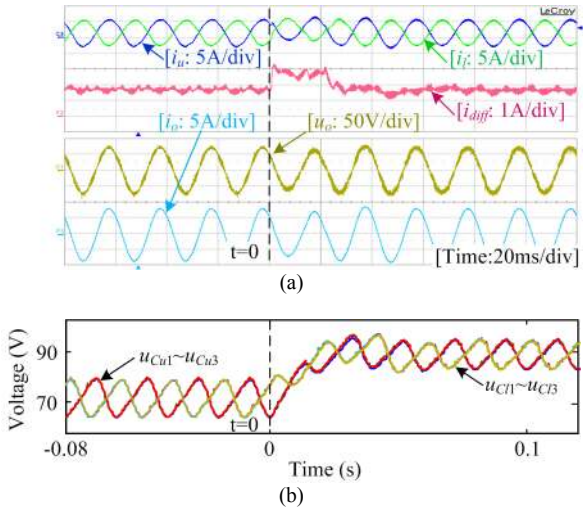


Fig. 23. Voltage and current waveforms of the MMC during capacitor voltage step change: (a) Arm currents, differential current, output voltage and current; (b) Capacitor voltages.

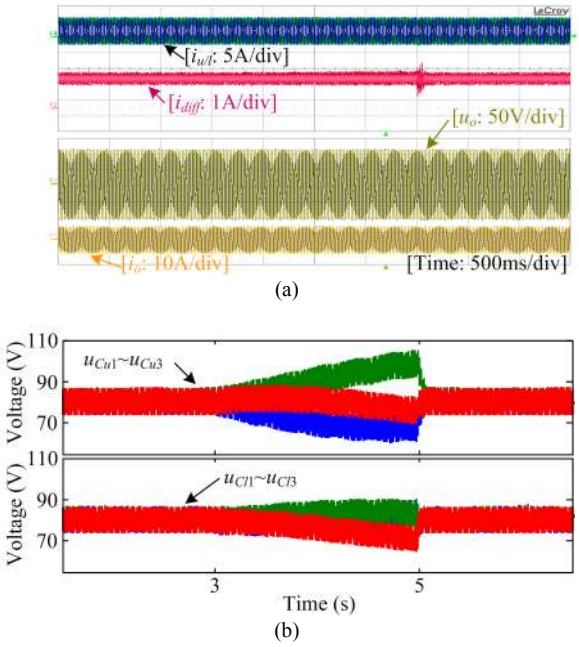


Fig. 24. Illustration of the effectiveness of the capacitor voltage balancing: (a) Arm currents, differential current, output voltage and current; (b) Capacitor voltages.

VI. Conclusion

In this paper, a novel distributed control architecture is proposed to improve the modularity of an MMC system, with additional advantages such as less information exchanging and reduced communication burden. One central controller is used to perform the output current regulation and system-level operations, while the MMC internal dynamics control, PWM signal generation, and local-level protections are distributed into local controllers. The voltage control loops in each local controller are designed to govern the capacitor voltage with only local information. This avoids the capacitor voltage transmission in each control cycle, which contributes to significantly reduced information exchanging through the communication network and less execution time required. The more modularized control architecture design makes it more flexible and convenient while applying the control strategy in MMCs with different numbers of sub-modules. The controller parameters are selected based on the control loops analysis and system stability considering the disturbances from other sub-modules. The effectiveness of the proposed distributed control strategy is experimentally verified on a prototype in the laboratory. The results confirm that the MMC system under the proposed distributed control operates properly and stably in steady-state and during large step changes, with well-regulated and balanced capacitor voltages.

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