Distributed Matched Bypasssing for Board-Level Power Distribution Networks

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ABSTRACT

Power-distribution networks need to provide impedance response with specified shape/value over a wide frequency band. Bypass capacitors with different values, and capacitors and planes may create resonance peaks, unless the capacitor parameters are selected properly. Distributed Matched Bypassing (DMB) is suggested to create a smooth impedance profile. DMB requires components with Q<<1, which in turn requires user-defined ESR. Different options are shown to set (increase) the ESR of bypass capacitors. The concepts of Bypass Quality Factor (BQF) and Bypass Resistor (BR) are introduced.

I. Introduction

There has been considerable interest in recent years to improve the power-distribution network (PDN) of high-end computer and networking equipment. At the module level, on printed-circuit boards, full-area conductive layers over regular-thickness or thin dielectric laminates provide low impedance for high-frequency decoupling [1] and a low-inductance conduit among PDN components. This is complemented by sometimes several thousands of capacitors for mid and lower frequency bypassing and decoupling [2] [3]. Conductive plane pairs in printed-circuit boards (PCB) may exhibit multiple resonances [4] [5] [6], which can be suppressed by proper damping of the structure [7], [8].

Bypass capacitors with different values connected to the conductive planes also may exhibit resonances either between different capacitor banks [9] or between capacitors and planes. The application and benefits of higher-ESR bypass capacitors are mentioned in several papers, see e.g., [8], [9], and [11] through [15]. One universal approach to reduce the resonance peaks is to minimize the inductance connecting the parts. With discrete surface-mount capacitors the loop inductance is several hundred pH, and usually the dimensions of PCB and capacitor do not allow us to lower it much below 100 pH, which value is still too high in some applications to suppress resonance peaks.

The ESR of bypass capacitors could also be selected to provide a flat impedance response, however, the ESR parameter for today's capacitors is not user defineable.

ESR of tantalum and electrolytic capacitors is usually in the ohm range, whereas ESR of multi-layer ceramic capacitors is usually in the milliohm range. Tantalum and electrolytic capacitors are usually considered as low-frequency bulk capacitors, and as such their construction and geometry is not optimized for low-inductance connection to the PCB.

This paper introduces the Bypass Quality Factor (BQF) parameter of bypass capacitors, followed by the description of the board-level Distributed Matched Bypassing (DMB) design methodology for PDNs, with possible ways to set (increase) the ESR of bypass capacitors.

II. Distributed Matched Bypassing of Power Distribution Network

The cumulative impedance of all board-level bypass capacitors should be a basin-shape impedance profile. For a lumped-equivalent model, shown in Fig. 1, the cumulative capacitance and inductance values are C_{tot} and L_{tot}. At low frequencies it is complemented by the (inductive) impedance of the power source, usually a Voltage Regulator Module, VRM (L_{VRM}). At high frequencies it is met by the capacitance of power planes or by the package/die capacitance (C_p). The goal is to create a cost-effective design, which meets the system's impedance requirement.

For power-distribution networks, the requirement is to guarantee that the peak-to-peak transient noise stays within specified limits, for all possible combinations of noise-source activities. With some exceptions, this is usually translated to a wide-band, resistive impedance requirement of PDN. Whenever the flat, resistive impedance profile cannot be maintained, or –due to other constraints– is not the optimum solution, the requirement toward the PDN's impedance profile can be expressed as having either

- overshoot-free transient response, or
- overshoot-free impedance-magnitude response

The board-level bypass capacitors are typically surface-mount ceramic parts for capacitance values at or below 10uF, and tantalum, electrolytic or organic through-hole or surface-mount parts for large capacitance values. In its simple form, the equivalent circuit of a bypass capacitor is a series C-R-L network.

A. The Bypass Quality Factor (BQF) of capacitors

Let us assume lumped models for multiple bypass capacitors, and frequency-independent equivalent-circuit elements for each capacitor. If we start with one single capacitor value (either a single capacitor piece or multiple capacitors with the same value, what will be referred to as a capacitor bank) with C-R-L values for the nominal capacitance, ESR and ESL parameters, respectively, we get the impedance profiles shown in Figure 2. Figure 2.a shows the impedance of a capacitor with C=1uF , L=1nH L and two different values of R; R=0.1 and R=0.01 ohms. The series resonance frequency is independent of R and is:

$$f_0 = \frac{1}{2p\sqrt{LC}} = 1.59MHz$$

The quality factor (Q) of the capacitor for the two different R values are:

$$Q = \frac{2\pi f_0 L}{R} = \frac{\sqrt{\frac{L}{C}}}{R} = 1,\ 0.1$$

If we need to achieve an impedance profile in a given frequency range at or below a specified value of Z, as long as Z>R, there are two frequencies (f_1 and f_2) where the impedance curve of the capacitor intercepts Z: f_1 is where the C-R-L impedance is still capacitive, and f_2 where the impedance of capacitor is already inductive. For Q<1, these frequencies can be approximated by:

$$f_1 = \frac{1}{2\pi CZ},\ \ f_2 = \frac{Z}{2\pi L}$$

In traditional radio-frequency applications, the above definition of Q is a good indication of the losses in the capacitor. In power-distribution applications, however, a bypass capacitor is more effective if it covers a bigger f_2/f_1 ratio of frequencies, within which frequency range its impedance is below a required value of Z. We call the f_2/f_1 ratio the Bypass Quality Factor (BQF). For Q<1, as illustrated in Figure 2.a and 2.b, BQF depends only on the ratio of capacitance and inductance of the individual capacitors, and can be also expressed as the inverse square of the product of Q and R. For a bank of N (N>=1) identical capacitors, it is:

$$BQF = \frac{\frac{f_2}{f_1}}{(ZN)^2} = \frac{C}{L} = (QR)^{-2}$$

Figure 2.a illustrates the concept of BQF for one piece of capacitor with C=1uF, L=1nH, and with two ESR and two Z values. For these parameters

$$BQF = \frac{\frac{f_{j2}}{f_{j1}}}{Z_j^2} = \frac{\frac{f_{i2}}{f_{i1}}}{Z_i^2} = \frac{C}{L} = 10^4$$

Figure 2.b illustrates the concept of BQF for two capacitor banks, both having capacitors with C=1uF, L=1nH, one bank having one piece of capacitor (N=1), the other bank having ten pieces of the same capacitor (N=10).

$$BQF = \frac{\frac{f_{j2\#1}}{f_{j1\#1}}}{(1Z_j)^2} = \frac{\frac{f_{j2\#10}}{f_{j1\#01}}}{(10Z_j)^2} = \frac{\frac{f_{i2\#1}}{f_{i1\#1}}}{(1Z_i)^2} = \frac{\frac{f_{i2\#10}}{f_{i1\#01}}}{(10Z_i)^2} = \frac{C}{L} = 10^4$$

Note that the above definition of BQF yields a parameter, which is independent of Z, N, and R (ESR). The BQF parameter in bypass applications is in line with the design methodologies where only the highest capacitance value of any given case style is used, thus maximizing BQF of the parts.

To create the specified power-distribution network response, the Distributed Matched Bypassing uses concepts similar to those described in the Adaptive Voltage Positioning [10], Extended Adaptive Voltage Positioning [11], and Dissipative Edge Termination [12] concepts. Recently bypass capacitors with increased ESR values have also been proposed to suppress capacitor-capacitor and capacitor-board resonances ([13], [14], [15]).

It should be noted that while the capacitance is a sole attribute of the capacitor piece, the inductance presented by the capacitor to the PDN depends not only on the shape and size of the capacitor body

(which sets its partial self inductance), but also on its connection to the PDN. It has also been shown (see [16], [17]) that the inductance and resistance may be a noticeable function of frequency.

B. Adaptive Voltage Positioning:

The Adaptive Voltage Positioning is a 'low-frequency' concept, referring to the proper selection of output resistance of VRMs. It suggests that with a given mid-frequency impedance requirement (Z_{mf}), the optimum (lowest) value of bulk capacitance for a given peak-to-peak transient noise can be achieved with an output resistance of VRM matching the mid-frequency impedance value

$$R_{out\_VRM} = Z_{mf}$$

This is contrary to the practice when a high DC gain in the control loop sets the output resistance of VRMs to very low values.

C. Extended Adaptive Voltage Positioning:

The Extended Adaptive voltage Positioning suggests that not only the VRM-to-bulk-capacitor interface, but also the bulk-capacitor-to-bypass-capacitor interface should follow the above procedure by setting the ESR of the lower and higher frequency capacitor banks the same and to match the square root of inductance-to-capacitance ratio of the adjacent capacitor banks.

D. Dissipative Edge Termination:

The Dissipative Edge Termination provides resistive termination to the power-distribution planes, by matching the real part of termination elements to the characteristic impedance of planes.

The Distributed Matched Bypassing combines and extends the above concepts, as described below. The DMB methodology provides matching between and among the impedances of the low-frequency VRM, mid-frequency bypass capacitors, and high-frequency planes and/or silicon elements, and thus creates a controlled impedance response over the entire frequency range of interest. The methodology gives simple rules and conditions for the parameters of PDN components, both for the same required impedance value throughout the entire frequency range and for situations when the required impedance varies with frequency.

E. The unit cell of Distributed Matched Bypassing

The Distributed Matched Bypassing concept uses elements with $Q<1$ ($Q<<1$ is preferred). The $Q<1$ condition creates a shallow flat bottom on the impedance curve of each capacitor bank. As a result, capacitor banks which are adjacent on the frequency axes, can be described by a lower-frequency R-L, and a higher-frequency R-C elements in parallel. This R-L-R-C network approximation is valid only in the vicinity of the crossover frequency of the adjacent component banks, as this first-order analysis neglects the interaction of the capacitance of the lower-frequency bank and the inductance of the higher-frequency bank. The equivalent circuit and frequency response of the unit cell is shown in Fig. 3. As long as the serial losses interconnecting the DMB elements are not significant, the power-distribution network can be represented by a number of such unit cells lumped in parallel, each covering different portions of the required frequency range, still not having interaction among the elements other than the interaction within each unit cell. This means that each bank in the power-distribution network is represented by two adjacent unit cells: one represents the lower-frequency R-C signature, whereas the other represents the higher-frequency R-L signature of the same bank of elements.

The frequency-dependent impedance of the unit cell (Z_{DMB_u}) is a second-order complex function:

$$Z_{DMB\_u} = \frac{\left(R_C + \frac{1}{jwC}\right)(R_L + jwL)}{\left(R_C + \frac{1}{jwC}\right) + (R_L + jwL)}$$

With s=jω, and rearranging, this becomes:

$$Z_{DMB\_u} = R_C + \frac{s(L - CR_C^2) + (R_L - R_C)}{s^2 LC + sC(R_C + R_L) + 1}$$

The characteristic equation in standard form is:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0;\ \omega_n = \frac{1}{\sqrt{LC}};\ \zeta = \frac{(R_C + R_L)}{2}\sqrt{\frac{C}{L}}$$

When R_L=R_C=R, the impedance expression can be simplified:

$$Z_{DMB\_u} = R + \frac{s(L - CR^2)}{s^2 LC + s2CR + 1}$$

If, moreover, we set

$$R_0 = \sqrt{\frac{L}{C}} = R$$

the unit-cell impedance reduces to a frequency-independent resistive impedance of R:

$$Z_{DMB\_u} = R = R_0$$

When capacitor banks with different capacitance values are attached together along the frequency axes, keeping the above condition yields the optimum solution, as the resistive impedance provides overshoot-free transient response, and no peaking in the frequency response. This is the default solution for DMB: the adjacent DMB unit cells both having the same resistive flat impedance response.

Under some circumstances, the entirely flat impedance response is either not desirable, or not feasible to maintain. In the general case

$$R_C \neq R_L$$

and the second-order impedance function yields a complex impedance. The impedance has to transition from R_L at low frequencies (or DC in this simplified DMB unit-cell model) to the R_C value at higher frequencies (or infinite frequency in this simplified DMB unit-cell model). Of the various possibilities, three special conditions will be considered here:

- case 1: overshoot-free transient response
- case 2: overshoot-free impedance-magnitude response, and
- case 3: impedance-magnitude response with a fixed amount of small overshoot (peak)

Case 1:

Overshoot-free transient response for a step-like current excitation is achieved when the characteristic equation has at least critical damping and yields two real roots. This means that the ζ damping factor must be equal to or bigger then one. At the boundary, the damping factor should be unity, which sets the following condition among the DMB unit-cell parameters:

$$\zeta^2 = 1;\ (R_C + R_L) = 2R_0 = 2\sqrt{\frac{L}{C}},\ \frac{(R_C + R_L)^2}{4} = \frac{L}{C}$$

Case 2:

Sometimes it is useful to set the requirement for the impedance magnitude as not having a peak, or $|Z_{DMB\_u}| = \max(R_L, R_C)$. This means that for a sinusoidal current excitation, the response magnitude will stay within the bounds of the responses at DC and infinite frequency. As shown in the Appendix, to achieve overshoot-free impedance response, the following condition should hold among the DMB unit-cell parameters

$$R_L R_C = R_0^2 = \frac{L}{C}$$

Case 3:

As will be shown later, the condition for case 2 becomes very restrictive and pessimistic for

$$\max\left(\frac{R_L}{R_C};\frac{R_C}{R_L}\right) >> 1$$

If we allow for a small, approximately 1% overshoot in the impedance-magnitude response, the conditions become more realistic and favorable. Evaluating the DMB unit-cell impedance numerically, the condition for the unit-cell parameters become:

$$(b_2 r^2 + b_1 r + b_0) R_{LC}^2 = \frac{L}{C}$$

where $R_{LC}=\max(R_L, R_C)$, $r=R_L/R_C$ if $R_L<R_C$, and $r=R_C/R_L$ if $R_C<R_L$, $b_0=0.4831$, $b_1=0.4907$, $b_2=-0.0139$.

A few typical applications of these cases and conditions are listed and described below.

1. VRM-to-bulk-capacitor interface

We assume that the active control loop of the VRM and the inductance connecting the VRM to the bypass capacitors have a simple one-pole R-L equivalent network representation, with a DC output resistance of $R_L=R_{VRM}$ and inductance of $L=L_{VRM}$. We also assume that the ESR of bulk capacitor(s) meets the mid-frequency impedance requirement: $R_C=ESR_{bulk}=Z_{mid}$.

The DC output resistance of the VRM and the required mid-frequency impedance of power-distribution network are determined by the system partitioning and are not necessarily the same. For instance, if the VRM supplies several independent boards, its output resistance should be lower than the mid-frequency impedance required by each of the boards. Depending on how many loads the VRM has to service, and what value of series DC loss in the power-distribution network has to be assumed, the DC output resistance of the VRM is equal to or lower than the mid-frequency impedance requirement: $R_{VRM}<=Z_{mf}$, $R_L = r\ R_C = r\ Z_{mf}$.

From the above conditions, we can solve either for C or for L. It is usual that we estimate the affordable inductance (L) of the VRM output and its connections, and solve for the required total low-frequency (bulk) capacitance.

The required inter relation among the four DMB unit-cell parameters:

Case1: $\frac{L}{CR_C^2} = \frac{(1+r)^2}{4},\ C = \frac{L}{Z_{mf}^2}\frac{4}{(1+r)^2}$

Case2: $\frac{L}{CR_C^2} = r,\ C = \frac{L}{Z_{mf}^2}\frac{1}{r}$

Case3: $\frac{L}{CR_C^2} = b_2 r^2 + b_1 r + b_0,\ C = \frac{L}{Z_{mf}^2}\frac{1}{b_2 r^2 + b_1 r + b_0}$

For all of the above cases, the lowest value of bulk capacitance is required if r=1. For r<1 values, the normalized capacitance requirement is shown in Figure 4. Note that as r decreases, the capacitance value necessary to maintain the specified condition monotonically increases; the highest value is required for overshoot-free frequency response (case2), and the lowest value is needed if we allow for a small amount of peaking (case3).

2. Bulk-to-mid-frequency capacitor interface

In case of capacitor-capacitor interfaces, selecting the resistance values in adjacent DMB unit cells to be equal, will guarantee a smooth continuation of impedance from one DMB cell to the next, and creates a flat and resistive impedance profile. As it was shown above, for R_C=R_L, the optimum solution is defined for all three cases by $R_L R_C = L/C = R_o^2$. If for any reason R_L does not equal R_C, we get either the situation of VRM-to-bulk-capacitance described above, or the situation of mid-frequency-to-package/die situation described below.

3. Mid-frequency-to-plane interface

If packages and silicons are assumed to have no noticeable influence on the PDN impedance, the mid-frequency bypass capacitor banks interface with the power-distribution planes. A pair of power/ground planes with dimensions of x*y and separation of h, with ε_r relative dielectric constant of the insulating laminate, can be chosen to substitute for all of the power plane pairs the stackup may have on the particular supply rail. The approximate characteristic impedance of the equivalent plane pair then becomes:

$$Z_p = \frac{266\left(\frac{h}{x}\right)}{\sqrt{e_r}\left(1+\frac{y}{x}\right)} = \frac{532}{\sqrt{e_r}}\frac{h}{P}$$

where P is the perimeter of the rectangular plane shape, P=2*(x+y). A bedspring equivalent circuit is used to simulate the impedance profile of the planes with their assumed bypass capacitors [25]. Figure 5 shows the simulated self-impedance profiles at the center of a pair of 25.4x25.4cm (10”x10”) plane pair with 50um (2-mil) separation, and N pieces of DMB components are placed uniformly around the edge of the planes, each having an ESR of R_L and ESL of L. Fig. 5a shows the impedance profile for the case when the R_L/N cumulative ESR of the mid-frequency DMB cells matches the Z_p plane impedance. The parameter is the L/N cumulative inductance of all of the DMB

parts. For a total inductance of 10pH, the impedance profile is smooth, for 100pH and 1nH inductance values there is an increasing ripple in the impedance profile due to the resonance peak of the static plane capacitance and DMB inductance. Fig.5b shows the same scenario, just the ESR of parts is ten times lower. Note that even at the 10pH inductance value, there is a noticeable ripple in the impedance profile. Detailed simulations show that sufficiently smooth impedance profile can be achieved under the following conditions:

$$\frac{R_L}{N} = Z_p,\ \frac{L}{N} = \frac{m_0 h}{5}$$

Note that the above matching conditions do not assume thin power/ground laminates, and are valid for a wide range of laminate thicknesses. Also, matching the planes' characteristic impedance may not be necessary if there is a sufficient number of large silicon devices spread over the planes so that those dampen plane resonances. However, there are situations when additional damping is necessary: on planes with large open areas, or planes with no silicon attached (such as DDRAM termination planes), or when socket/package inductances isolate the silicon from the planes at the resonance frequencies.

4. Mid-frequency-to-package/die interface

In power-distribution networks, feeding a large piece of silicon, the connection may be point-to-point, where the path goes through a package, with optional package capacitors, and ends on the silicon. The low equivalent resistance of silicon usually creates a package resonance [19]. The DMB unit cell on the boundary of package and silicon has the mid-frequency target impedance (Z_{mf}) and package inductance (L_{pkg}) in the R-L leg, and the die capacitance (C_{die}) and die equivalent resistance (R_{die}) in the R-C leg.

In this situation, usually $R_C<R_L$, $r=R_C/R_L$, and the task may be to find the maximum permissible value of L (L_{pkg}). Expressing L in cases 1 through 3 yields:

Case1: $\frac{L}{CR_C^2} = \frac{(1+r)^2}{4},\ L = \frac{C}{Z_{mf}^2}\frac{(1+r)^2}{4}$

Case2: $\frac{L}{CR_C^2} = r,\ L = \frac{C}{Z_{mf}^2} r$

Case3: $\frac{L}{CR_C^2} = b_2 r^2 + b_1 r + b_0,\ L = \frac{C}{Z_{mf}^2} b_2 r^2 + b_1 r + b_0$

For all of the above cases, the highest value of inductance is allowed if r=1. For r<1 values, the normalized inductance requirement is shown in Figure 6. Note that similar to the VRM-to-bulk-capacitance interface, as r decreases, the inductance value necessary to maintain the specified condition monotonically decreases; the lowest value is required for overshoot-free frequency response (case2), and the highest value is allowed if we allow for a small amount of peaking (case3).

As a summary, the Distributed Matched Bypassing methodology uses a few simple steps:

a) determine the number of high-frequency capacitors from the required total inductance,
b) select the highest available capacitance in the given size,
c) calculate the required ESR of each capacitor. If the total capacitance of high-frequency bypass capacitors and the achievable connecting inductance of VRM would still create a

resonance peak, additional (lower-frequency) capacitor banks are selected, similar to the process described in [14].

d) Optionally, if suppression of plane resonances is also required, the inherent plane dimensions should be selected to match the mid-frequency impedance requirement.

By following the above procedure, the possibility of inter-capacitor and plane-to-capacitor resonances can be minimized.

Note that requesting the highest available capacitance in a given package style also conveniently minimizes the inductance of the capacitor body. As shown in Figure 7, higher capacitance in the same package size often comes with a thinner cover layer, thus lowering the inductance.

F. Sensitivity to component tolerances

The Q<<1 condition of the DMB components yields a lower sensitivity to component tolerances. As opposed to the case when the bypass components have Q>=1, when the impedance magnitude of peaks and valleys at each frequency transition between adjacent components depend on at least three parameters (C, L, and R), the Q<<1 condition decouples the L and C values within each unit cell, thus leaving effectively only the tolerance of R itself.

III. Implementation of DMB

A. ARIES implementation

The ARIES solution (***A***nnular ***R***esistive ***I***nterstitial ***E***lement, ***S***creened-in) is based on the ABR™ (***A***nnular ***B***uried ***R***esistor, Fig. 8) process [20] [21], where the ESR of a ceramic capacitor is increased by adding a series resistor element, created in an annular void between a conductive pad and its surrounding antipad. In bypassing applications, one terminal of the resistor should be on one of the power rails, usually located on large metal areas or full planes, conveniently eliminating the need for an antipad ring connection, thus maximizing the available density.

In a series R-C connection, assuming linear components, the sequence of the two parts does not affect the resulting impedance. The external resistance can be either on the ground side, or on the power side, or split in any ratio between the ground side and power side. To reduce the number of required components, in the ARIES solution resistors are inserted only between the capacitor terminals and the power plane.

To minimize the required footprint and the loop inductance, as shown in Figure 9, the ARIES solution uses a multi-terminal capacitor (eight-terminal capacitor is shown in the Figure) with blind vias connecting to the PCB planes. The capacitor sits on the outermost (L1) metal layer, and four of the capacitor's terminals are connected to the second (L2) ground plane. Four other blind vias connect the remaining terminals of the capacitor to the third (power) layer (L3). Having the ground layer outside with direct connection to the capacitor has several advantages:

- The ground layer provides EMI shielding
- The capacitor body is tied to ground, it does not 'float' on the noise voltage across the series resistance
- Larger-diameter ABR™ components can be used which can extend underneath the ground blind vias

The direct physical connection of the embedded resistors to one of the planes also increases their power rating.

In one ARIES element there is either one eight-terminal capacitor (IDC: Inter Digitated Capacitor) or one array of four capacitors with eight independent terminals (IPC: Integrated Passive Component), plus four embedded resistors. The close proximity of the embedded resistors in one block provides good current sharing among the four legs, thus reducing the current difference due to resistance tolerances.

Note that the same geometrical concept can be extended to capacitor packages with more terminals [22], or fewer terminals, including the regular two-terminal straight or reversed geometry capacitors.

The tolerance of embedded printed resistors depends on the resistive ink composition, printing consistency, and long-term behavior of the part. Without trimming, +-25% tolerances can be achieved, which can be further improved, if necessary, by trimming processes. In bypassing applications, though, a tolerance tighter than +-20% is rarely required.

B. DMB implementation with controlled-ESR capacitors

Designs of high CV, low inductance capacitors typically include a large number of internal layers, multiple parallel external termination contacts and minimized inactive margins, all of which combine to also reduce the ESR, relative to standard MLC's. This trend of lowering ESR is contrary to the system need of controlled, increased ESR. Thus, in leading edge decoupling applications, capacitor Equivalent Circuit Parameters must be fully specified and controlled, including series capacitance, inductance, and now, resistance. The challenge for capacitor designers is to develop ways to control and increase ESR without compromising hard-won gains in lower ESL and higher CV ([22], [23], [24]). AVX Corporation is actively developing capacitors with controlled, selectable ESR while preserving the low inductance structure of the capacitor device. Efforts to date yield capacitors with deliberate ESR variations over three orders of magnitude in 0306, 0508 and 0612 LICC and, 0508 and 0612 IDC (Fig. 10). Figure 11 shows the impedance profiles of a conventional (low-ESR) and a controlled-ESR 0612 1uF ceramic capacitor. The parts were soldered on two pads, connecting with one pair of blind vias from the pads to a plane pair one and two layers below. The figure also shows the impedance of the small bare fixture board. Note that

- the impedance profile of controlled-ESR part is flat over more than two decades of frequencies
- the first antiresonance peak is at about 750MHz for both parts, indicating that ESL is not increased by controlling ESR

C. Test board implementation

Twenty-layer 25.4x12.7 cm (10"x5") test boards with 50um (2-mil) FR4 dielectric layers between power and ground planes were designed and built. The stackup is shown in Fig. 12. The boards had two 2.54cm (one-inch) grids with 1.27cm (0.5") offset with respect to each other. On one of the grids, nominally starting at the lower left corner of the board, test through-holes were placed to allow the measurement of the impedance profile. Because the length and width of the board are integer multiples of an inch, there would be thirty test points exactly falling on the periphery of the board. These thirty test points were pulled back 0.63cm (0.25") from the board edge. The grid points of the

second square grid start at a 1.27x1.27cm (0.5"x0.5") offset from the lower left corner, and they accommodate surface pads for 1206 eight-terminal capacitors with the appropriate blind vias and embedded resistors. For the locations of test vias and capacitor pads see also Figures 13 and 14.

A second set of boards with the same stackup and dimensions, except with solid copper connection in place of the embedded resistors serve the purpose of reference structure to measure and simulate the printed-circuit board itself. The same reference boards with no embedded resistors were also used to measure controlled-ESR capacitors.

The test structure was characterized by measurements and simulations in several steps.

1. Bare board parameters:
The bare board was characterized by detailed SPICE-grid simulations and measurements. Uniform and homogenious cross section and materials were assumed. Considering the 1.27mm (50 mils) pullback of planes from the board edge, the plane dimensions were a=25.15cm (9.9") and b=12.44cm (4.9"). There are two parameters, however, the dielectric constant and the plane separation, which on a finished board cannot be measured directly without destructive probing.

To obtain the dielectric constant and the plane separation, we can use the expressions of static plane capacitance and first modal resonance frequency:

$$C = \varepsilon_0 \varepsilon_r \frac{ab}{s} \qquad f_{res} = \frac{1}{2a\sqrt{\varepsilon_0 \varepsilon_r \mu_0}}$$

where C is the static capacitance of the plane pairs, a and b are the length and width of planes, s is the separation of planes, f_{res} is the first modal resonance frequency of the planes, and ε_0, ε_r, μ_0 are the dielectric constant of free space, relative dielectric constant of laminate material between conductive planes, and permittivity of free space, respectively.
By rearranging, we get:

$$s = \varepsilon_0 \varepsilon_r \frac{ab}{C} \qquad \varepsilon_r = \left(\frac{1}{4a^2 f_{res}^{\ 2} \varepsilon_0 \mu_0} \right)$$

From the above expressions, with the measured values of C=44.5nF, and f_{res}=291MHz, the dielectric constant and plane separation were calculated:

s= 52.3um (2.06 mils) per pair, and ε_r= 4.217.

The good correlation of simulated and measured self impedance of the bare test board, defined in Figures 12 through 14, at the test point of x=10.16cm (4") and y=7.62cm (3") from the lower left corner, is illustrated in Fig. 15. The SPICE grid used for the simulation had 0.635cm (0.25-inch) uniform grid of lossy transmission-line segments, the topology and simulation parameters were as described in [25].

2. Capacitor pad and blind-via connection parameters:

The electrical parameters of the eight-terminal capacitor connection were derived by shorting all eight pads of one capacitor location on the surface with a copper sheet. The self impedances and transfer impedances at several locations were measured and simulated. Three different capacitor locations were shorted, one at a time. Using the parameters of the bare board, the elements of a series R-L circuit were selected during the simulations to fit the measured impedance profile of the shorted board. The attached impedance of the via/pad combination was matched with the following elements:

$$L_a=48.5pH,\ R_{dc\_a}=5E\text{-}4\ ohms,\ R_{sk\_a}=1.6E\text{-}7\ ohms*sqrt(f)$$

Note that this R-L equivalent circuit represents the pads and vias only, these values are independent from and do not contain the impedance contribution from the planes and capacitors.

The correlation of the simulated and measured self impedance of the shorted test board is illustrated in Fig. 16, having a short at the capacitor location x=11.43cm (4.5") and y=6.35cm (2.5"), the impedance being measured at test point x=7.62cm (3") and y=10.16cm (4"). The peak at 90MHz corresponds to the resonance of the static plane capacitance with the shorting inductance.

3. Capacitor parameters:

Similar to the extraction of via-pad parameters, the capacitor parameters were also extracted by soldering one piece of eight-terminal capacitor on the board, and correlate the measured self and transfer impedances on the board . Data in this paper is shown for the AVX 2.2UF X7R IDC part (W3L16C225MAT). The equivalent circuit is a series C-R-L network, however, as it was shown in [16] and [17], the inductance and resistance associated with the capacitor body are both frequency dependent. The correlation and curve fitting was performed at two characteristic frequencies: the series and first parallel resonance frequencies. In this particular case, the series resonance was around 8MHz, the first parallel resonance was at 62MHz.

The extracted R and L parameters at these two frequencies were 6mohm and 160pH at 8MHz, and 10.5mohm and 120pH at 62MHz. Note that as was shown above, the via-pad combination at these frequencies represent 1mohm and 48.5pH at 8MHz, and 1.8mohm and 48.5pH at 62MHz, therefore the extra resistance and inductance due to the capacitor piece itself is 5mohm and 111.5pH at 8MHz, and 8.7mohm and 71.5pH at 62MHz.

The correlation of measured and simulated impedances with the above parameters is illustrated in Fig. 17.

4. Fully populated DMB test board:

The test boards with and without embedded resistors were also measured with a full population of low-ESR capacitors. Though other allocations are also feasible, the population described in this paper was a full ring of capacitors along the periphery of board, a total of twenty-six pieces. Figure 18 compares the self-impedance magnitude of the populated board with and without embedded resistors and the self-impedance of the bare board. The three traces: a) thin continuous line: impedance of the bare board (for reference), b) dashed line: impedance of the board populated with low-ESR parts without embedded resistors, and c) solid heavy line: impedance with embedded resistors. The graph above shows that by adding the embedded resistors, the impedance at 324 MHz is reduced from 0.119 ohms to 0.052 ohms, and at 480MHz from 0.133 ohms to 0.038 ohms.

D. Module card implementation

Figure 19.a is a photo of the embedded resistor on an un-laminated inner layer, figure 19.b shows the cross section at the printed-resistor element. Figure 20 illustrates the savings in component count and board area on a module card. Figure 21 shows the distribution of measured resistance values on two separate DMB layers on the finished board.

IV. The concept of Bypass Resistor (BR)

The Distributed Matched Bypassing relies on the controlled ESR of capacitor parts to create a wide-band resistive impedance profile. It also assumes capacitors with Q<<1, so that there is a pronounced flat resistive-like impedance bottom of their impedance curve. This reduces the interaction of capacitance and inductance tolerances, creating a less sensitive network. To achieve a design goal with the lowest number of parts, we also need the highest available capacitance in a given package style.

Realyzing that for bypass applications the resistance (ESR) is of primary importance, we can define a new part, called Bypass Resistor (BR). It is a virtual R-C-L component, where the R and C are specified, and L depends both on the geometry of package(s) and the geometry of usage. It can be either one piece: controlled-ESR capacitor; or separate pieces: a low ESR capacitor in series to resistor(s) forming a low-inductance geometry.

The suggested specification items for the bypass resistor:

- Capacitor part: all specification items that are used for bypass capacitors, except the capacitance, which is always the maximum available for the particular case style and material
- Resistor part: all specification items that usually go with a resistor

The available resistance values should match the resistance tolerance and stability. For a +-30% resistance tolerance, the E3 series is adequate: 1, 2.2, 4.7, 10. For +-20% resistance tolerance, the E6 series is suitable: 1, 1.5, 2.2, 3.3, 4.7, 6.8, 10. Assuming +-20% tolerance (E6), the 10 mohm to 10 ohm range can be covered with just 19 different ESR values for each case size. As a comparison, the +-10% E12 series covers the four decades of 100pF to 1uF range with a total of 49 entries.

Conclusions

It is shown that the Adaptive Voltage Positioning, Extended Adaptive Voltage Positioning, and Dissipative Edge Termination concepts can be merged to provide a user-defined optimum PDN impedance profile over a wide band of frequencies. Distributed Matched Bypassing requires low Q (Q<1) bypass capacitor elements. Two different solutions and their implementations are described how to set the ESR of bypass capacitors. It is also shown that for DMB applications, the Bypass Quality Factor (BQF) is a useful representation of the expected capacitor performance. The Bypass Resistor (BR) concept is introduced. Simulated and measured results on test boards and module-cards illustrate the feasibility of DMB.

Acknowledgement

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Appendix: Condition for overshoot-free impedance profile of DMB unit-cell

With the notations of Figure 3, the complex impedance of the DMB unit cell is:

$$Z_{DMB\_u} = \frac{\left(R_C + \frac{1}{j\omega C}\right)(R_L + j\omega L)}{\left(R_C + \frac{1}{j\omega C}\right) + (R_L + j\omega L)}$$

The condition for having overshoot-free impedance magnitude is defined as:

$$|Z_{DMB\_u}| = \max(R_L, R_C)$$

The expression of impedance magnitude involves the square-root function. This can be removed by squaring both sides:

$$Z^2_{DMB\_u} = \max(R_L^2, R_C^2)$$

$$Z^2_{DMB\_u} = \frac{u}{v} = \frac{(R_L - \omega^2 LCR_C)^2 + (\omega(L + CR_C R_L))^2}{(1 = \omega^2 LC)^2 + ((R_L + R_C)\omega C)^2}$$

The extrema of the squared impedance can be found by setting the first derivative to zero:

$$\frac{d}{d\omega}\left|Z_{DMB\_u}(\omega)\right|^2 = \frac{d}{d\omega}\left(\frac{u}{v}\right) = \frac{v\frac{du}{d\omega} - u\frac{dv}{d\omega}}{v^2} = 0$$

where

$$\frac{du}{d\omega} = 4\omega^3 (LCR_C)^2 + 2\omega(L^2 + (CR_C R_L)^2)$$

$$v = (1 = \omega^2 LC)^2 + ((R_L + R_C)\omega C)^2 = \omega^4 (LC)^2 + \omega^2 (C^2 (R_L + R_C)^2 - 2LC) + 1$$

$$\frac{dv}{d\omega} = 4\omega^3 (LC)^2 + 2\omega(C^2 (R_L + R_C)^2 - 2LC)$$

$$v\frac{du}{d\omega} = 4\omega^3 (LCR_C)^2 \left[\omega^4 (LC)^2 + \omega^2 (C^2 (R_L + R_C)^2 - 2LC) + 1\right] +$$

$$+ 2\omega(L^2 + (CR_C R_L)^2)\left[\omega^4 (LC)^2 + \omega^2 (C^2 (R_L + R_C)^2 - 2LC) + 1\right]$$

$$v\frac{du}{d\omega} = 4\omega^7 (LC)^4 R_C^2 + 2\omega^5 (LC)^2 \left[2C^2 R_C^2 (R_L + R_C)^2 - 4LCR_C^2 + L^2 + (CR_C R_L)^2\right] +$$
$$+ 2\omega^3 C\left[2C(LR_C)^2 + (L^2 + (CR_C R_L)^2 (C(R_L + R_C)^2 - 2L)\right] + \omega\left[2(L^2 + (CR_C R_L)^2)\right]$$

$$u\frac{dv}{d\omega} = \left[\omega^4 (LCR_C)^2 + \omega^2 (L^2 + (CR_C R_L)^2) + R_L^2\right]\left[4\omega^3 (LC)^2 + 2\omega(C^2 (R_L + R_C)^2 - 2LC))\right]$$
$$u\frac{dv}{d\omega} = \omega^7 \left[4(LC)^4 R_C^2\right] + \omega^5 \left[(LCR_C)^2 2(C^2 (R_L + R_C)^2 - 2LC) + (L^2 + (CR_C R_L)^2)4(LC)^2\right] +$$
$$+ \omega^3 \left[(L^2 + (CR_C R_L)^2)2(C^2 (R_L + R_C)^2 - 2LC) + (LC)^2 4R_L^2\right] + \omega\left[R_L^2 2(C^2 (R_L + R_C)^2 - 2LC)\right]$$

$$\frac{d}{d\omega}\left(\frac{u}{v}\right) = \frac{v\frac{du}{d\omega} - u\frac{dv}{d\omega}}{v^2} = 0 \text{ where}$$

$v\frac{du}{d\omega} - u\frac{dv}{d\omega} = 0$, which yields a seventh-order equation for ω:

$$v\frac{du}{d\omega} - u\frac{dv}{d\omega} = \omega^7 \left[4(LC)^4 R_C^2 - 4(LC)^4 R_c^2\right] +$$
$$+ \omega^5 \{(LCR_C)^2 2(C^2 (R_L + R_C)^2 - 2LC) + (L^2 + (CR_C R_L)^2)4(LC)^2\}$$
$$- \omega^5 \{2(LC)^2 [2C^2 R_C^2 (R_L + R_C)^2 - 4LCR_C^2 + L^2 + (CR_C R_L)^2]\} +$$
$$+ \omega^3 \{(L^2 + (CR_C R_L)^2)2(C^2 (R_L + R_C)^2 - 2LC) + (LC)^2 4R_L^2\} -$$
$$- \omega^3 \{2C[2C(LR_C)^2 + (L^2 + (CR_C R_L)^2)(C(R_L + R_C)^2 - 2L)]\} +$$
$$+ \omega\{R_L^2 2(C^2 (R_L + R_C)^2 - 2LC)\} - \omega\{2(L^2 + (CR_C R_L)^2)\}$$

The highest-order term is identical to zero. Also, we can divide both sides of the equation by ω, this yields a quadratic equation in ω^2.

$$v\frac{du}{d\omega} - u\frac{dv}{d\omega} = 0 = a_4\omega^4 + a_2\omega^2 + a_0$$

The possible frequencies, where impedance maximum bigger than max{R_C, R_L} can occur, are given by:

$\omega^2 = \frac{-a_2 \pm \sqrt{a_2^2 - 4a_0 a_4}}{2a_0}$, where

$$a_4 = \{(LCR_C)^2 2(C^2 (R_L + R_C)^2 - 2LC) + (L^2 + (CR_C R_L)^2)4(LC)^2\} -$$
$$- \{2(LC)^2 [2C^2 R_C^2 (R_L + R_C)^2 - 4LCR_C^2 + L^2 + (CR_C R_L)^2]\}$$
$$a_2 = \{(L^2 + (CR_C R_L)^2)2(C^2 (R_L + R_C)^2 - 2LC) + 4(LCR_L)^2\} -$$
$$- \{2C[2C(LR_C)^2 + (L^2 + (CR_C R_L)^2)(C(R_L + R_C)^2 - 2L)]\}$$
$$a_0 = \{R_L^2 2(C^2 (R_L + R_C)^2 - 2LC)\} - \{2(L^2 + (CR_C R_L)^2)\}$$

The maximum of the impedance magnitude occurs at those non-trivial frequencies, where $\omega^2 > 0$. No maximum occurs if the discriminant of the quadratic equation is zero or negative. This yields the following condition:

$$D^2 = a_2^2 - 4a_0a_4 = 0$$

This condition can be evaluated by using the following notations:

$$R_0 = \sqrt{\frac{L}{C}};\ R_L = aR_0;\ R_C = bR_0$$

which yields the following equation:

$$(a^2 - b^2)^2 = (1 + 2a^2 - 2a^3b - a^4)(-1 - 2b^2 + 2ab^3 + b^4)$$

This equation can be rearranged as follows:

$$(1-a^4)(1-b^4) + (1-a^4)2b^2(1-ab) + (1-b^4)2a^2(1-ab) + 4a^2b^2(1-ab)^2 + (a^2-b^2)^2 = 0$$

Substituting

$x = (1 - a^2b^2);\ and\ \ y = (1-ab)$, we get $\quad x^2 + 2(a^2 + b^2)xy + 4a^2b^2y^2 = 0$

By inspection, one solution is x=0 and y=0, which occurs if a=1/b. For real, non-zero R_L and R_C parameter values, the squared terms in the equation must be non-negative, and also x and y will always have the same sign, therefore the xy term is always nonzero.

From the above, we can conclude that the boundary condition for having no impedance-magnitude peak bigger than R_L or R_C (whichever is bigger) is:

$$R_LR_C = R_0^2 = \frac{L}{C}$$

Figures and tables

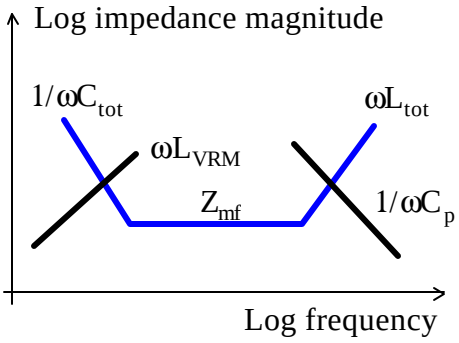


Figure 1.: Typical impedance curve of a board-level Power Distribution Network. The cumulative ESR values of parts in one or more bypass capacitor banks create the flat bottom with value of Z_{mf}.

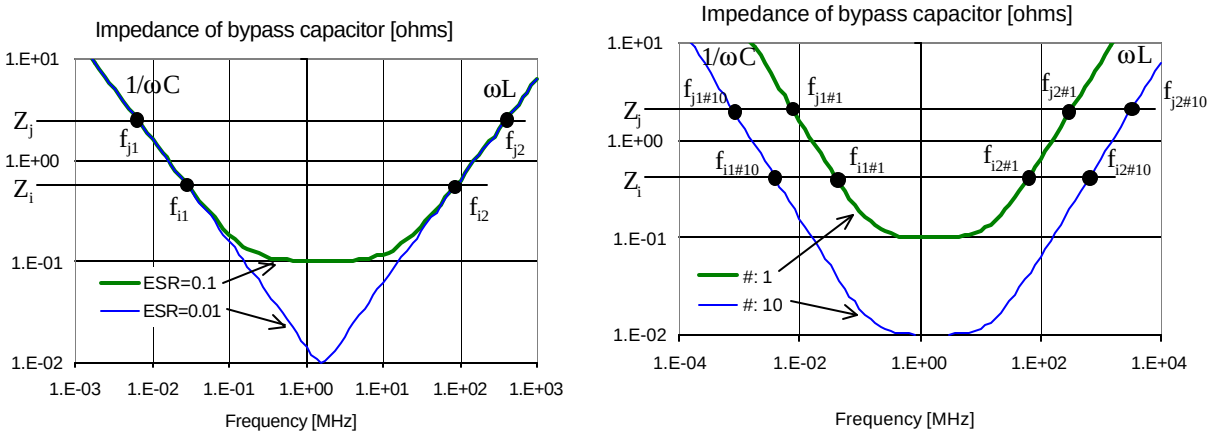


Figure 2.: Illustration of Bypass Quality Figure for a capacitor bank with C=1uF, L=1nH. Figure 2.a shows the effect of ESR, Fig.2.b illustrates the effect of number of capacitors in the bank. Note that as long as Q<1 and Z>ESR, BQF= f_{2i}/f_{1i} is the same for all Z and ESR values. Also note the expanded frequency scale in Figures 2.b.

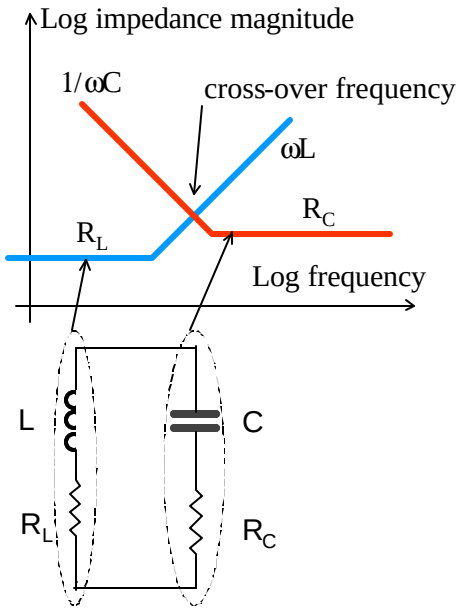


Figure 3.: Equivalent circuit and Bode diagram of unit cell of Distributed Matched Bypassing. The equivalent circuit is valid near the cross-over frequency, where the lower and higher frequency capacitor banks are represented by an R_L-L and R_C-C circuit, respectively.

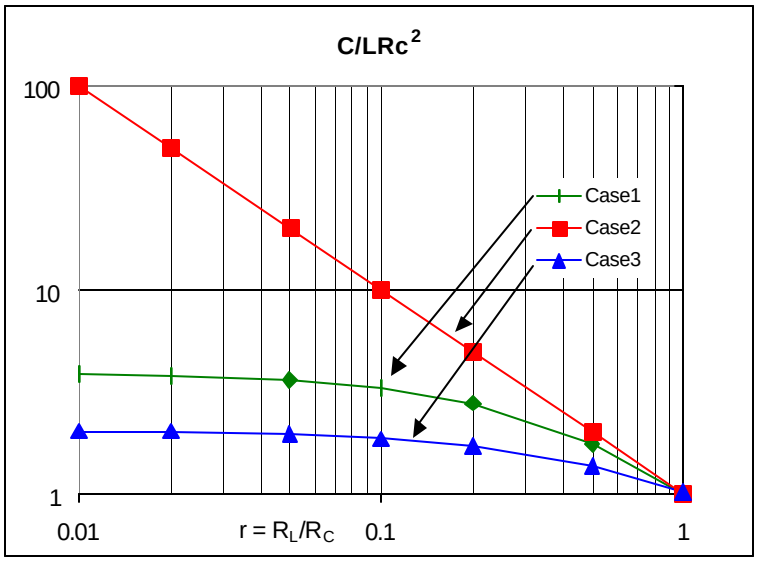
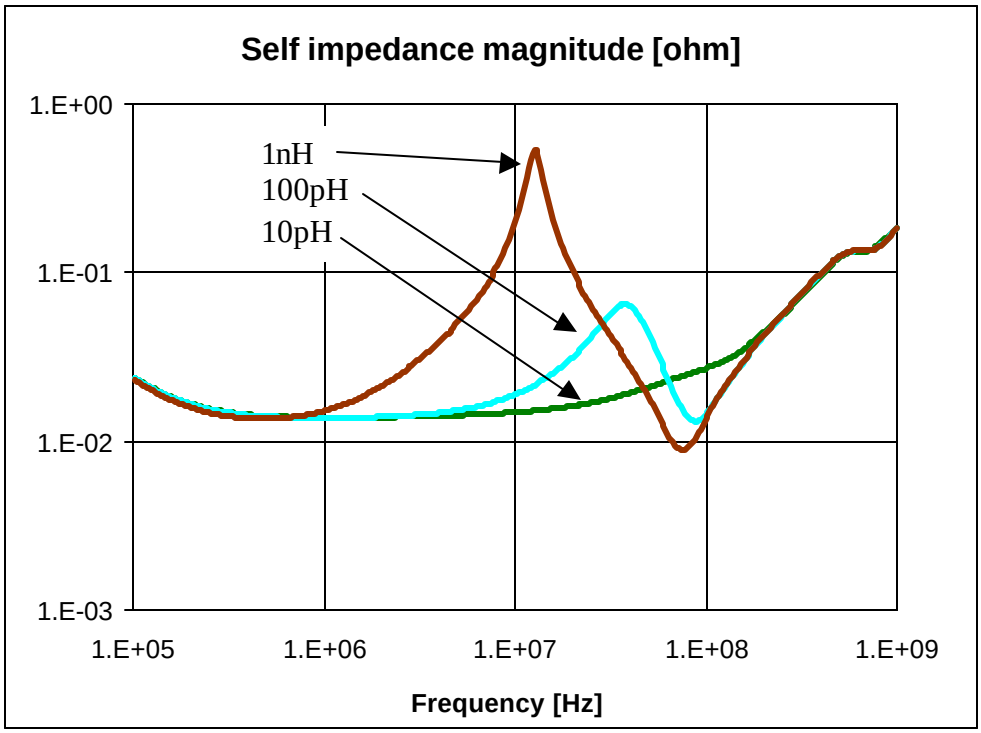
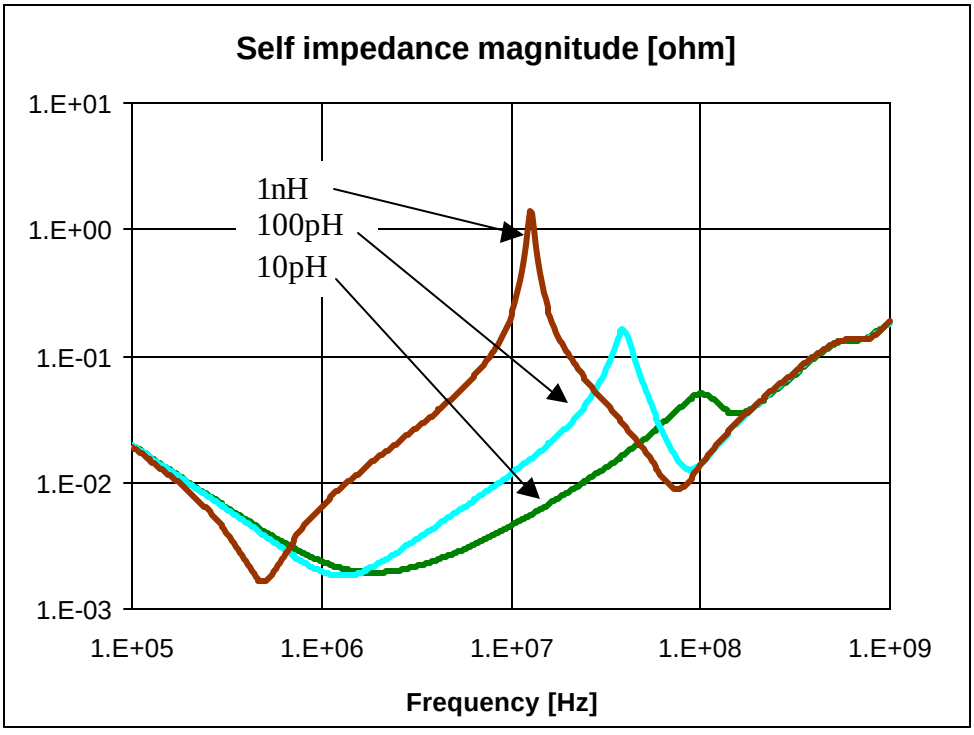


Figure 4. Normalized bulk-capacitance requirement versus $r=R_L/R_C$.



a)



b)

Figure 5.: Self-impedance magnitude at the center of one pair of power/ground planes with h=2mil separation, ε_r=4, with DMB elements along the board periphery. Fig 5.a: $R_L/N=Z_p$, Fig. 5.b: $R_L/N=0.1Z_p$. Parameter; L/N inductance of DMB elements.

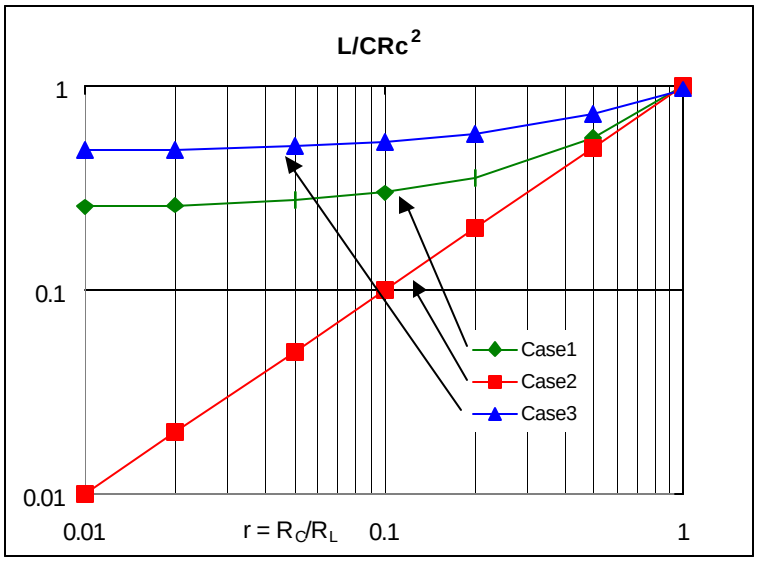


Figure 6. Normalized inductance requirement versus $r=R_C/R_L$.

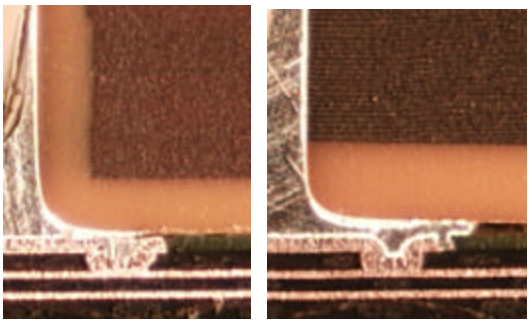


Figure 7.: Cross section of mounted capacitors showing the bottom cover thickness in 0612-size IDC package: 2.2uF part on the left (7.2 mils bottom cover) and 1uF part on the right (10 mils bottom cover). Layer2-layer3 laminate is 2-mil dielectric with one-ounce copper on either side.

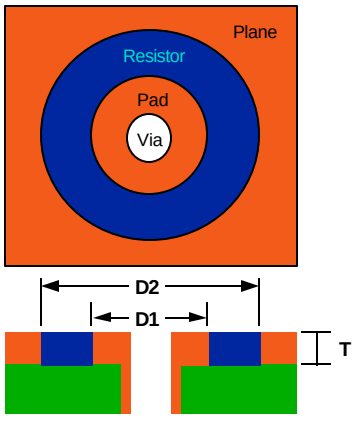


Figure 8: Construction of Annular Buried Resistor (ABR^{TM})

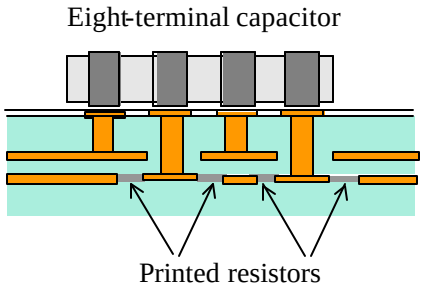


Figure 9: ARIES construction, shown in a cross-sectional side view. The multi-terminal capacitor is connected with blind vias to the power and ground planes below. Four ABR^{TM} embedded resistors on the lower plane set the ESR to the required value.

AVX Low inductance capacitors

Capacitor type	max. cap. [µF]	inductance [pH]	BQF [xE+03]	ESR min. mOhm	ESR max. mOhm
0612 LICC	10.00	325	31	6	1000
0508 LICC	6.80	250	27	5	1000
0306 LICC	2.20	200	11	4	1000
0612 IPC	4.00	150	27	6	N/A
0612 IDC 8 terminals	10.00	110	91	5	500
0508 IDC 8 terminals	6.80	90	76	4	500
0612 IDC 10 terminals	10.00	75	133	4	500
0508 IDC 10 terminals	6.80	65	105	3	500
1818 IDC 32 terminals	68.00	15	4533	1	TBD
LICA	0.13	25	5	15	N/A
HiFLI ™ 8x8	0.22	10	22	4	200
Ta capacitor	1000.00	3600	278	25	N/A
Best cap	4.00E+05	1400	285714	50	N/A

Figure 10: Maximnum capacitance, typical attached inductance, BQF and ESR range of some AVX capacitor families.

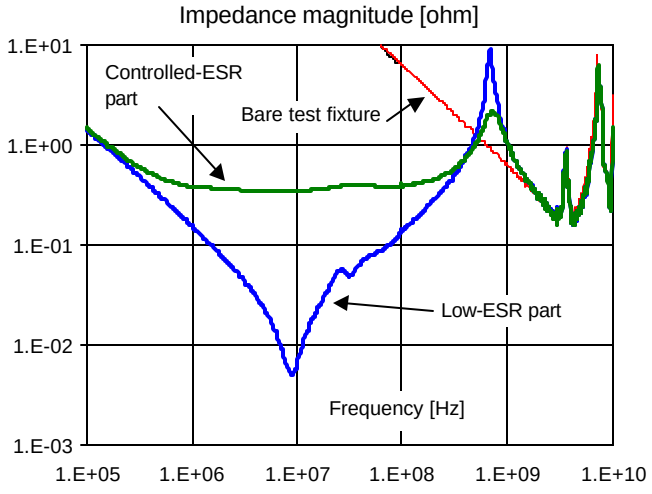


Figure 11. Measured impedance profile of AVX 1uF 0612-size low-ESR and controlled-ESR LICC capacitors.

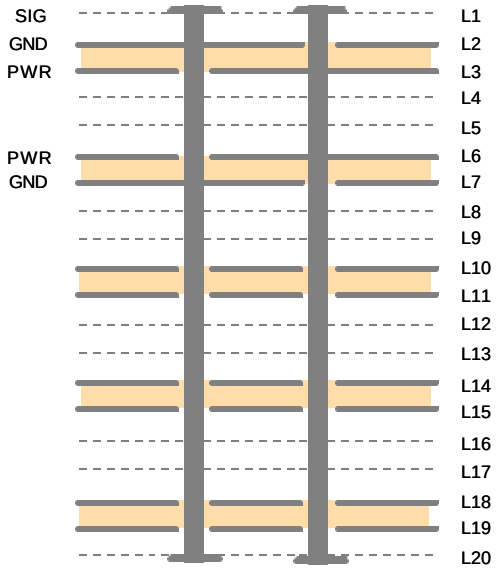


Figure 12.: Stackup of test boards. In the networks measured, only the upper two plane pairs (L2-L3, and L6-L7) are connected to test vias. The other six planes and eight signal layers were left floating.

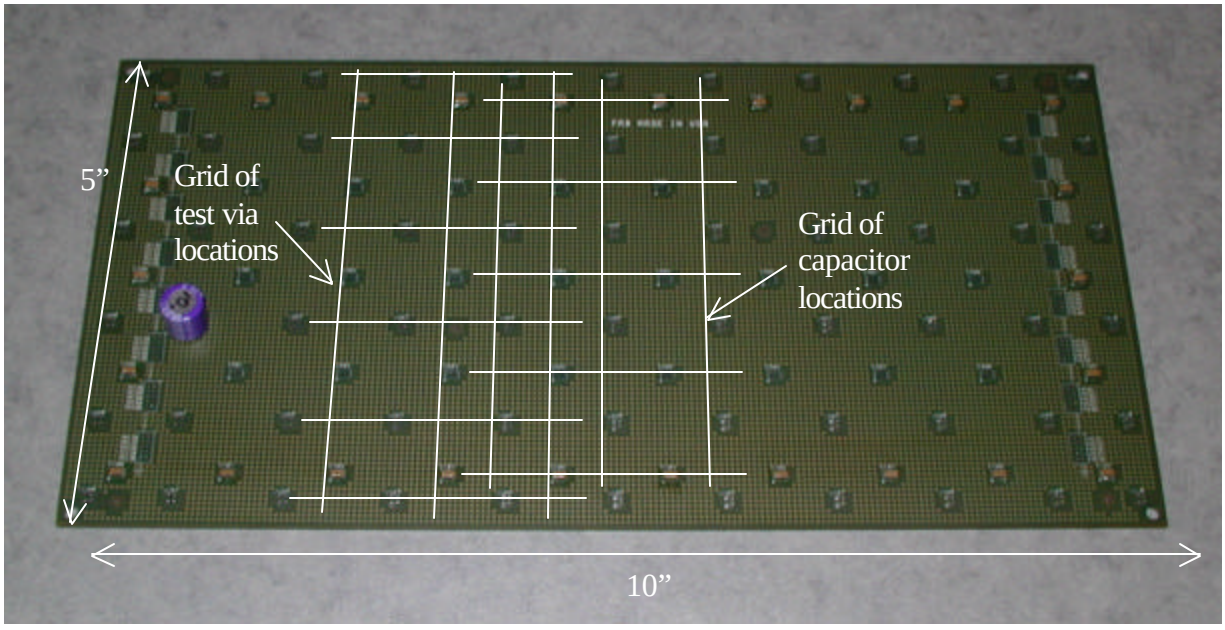


Figure 13: Photo of 10”x5” test board, with the test via and capacitor grids identified. Besides of the single bulk capacitor, there are 26 pieces of 2.2uF IDC parts on the outer ring of ARIES positions.

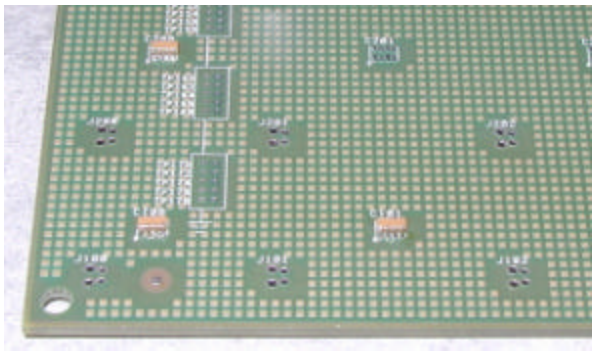


Figure 14: Close-up of test points and capacitor elements on the test board.

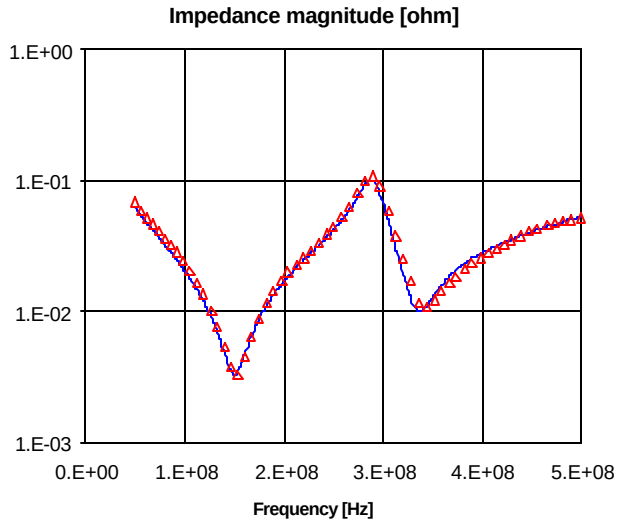


Figure 15.: Simulated (solid line) and measured (triangles) self-impedance magnitude of the bare test board, measured at the test point at x=4", y=3" from the lower left corner.

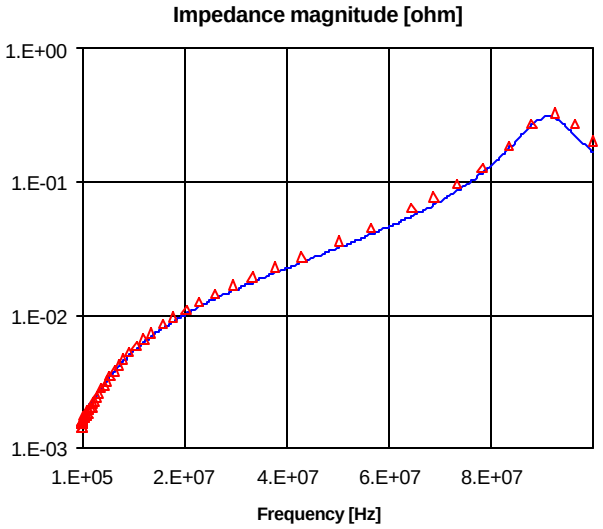
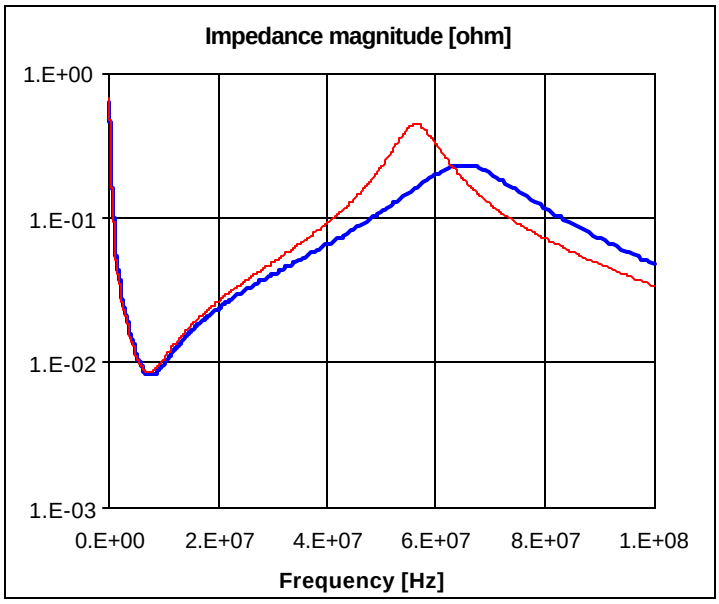
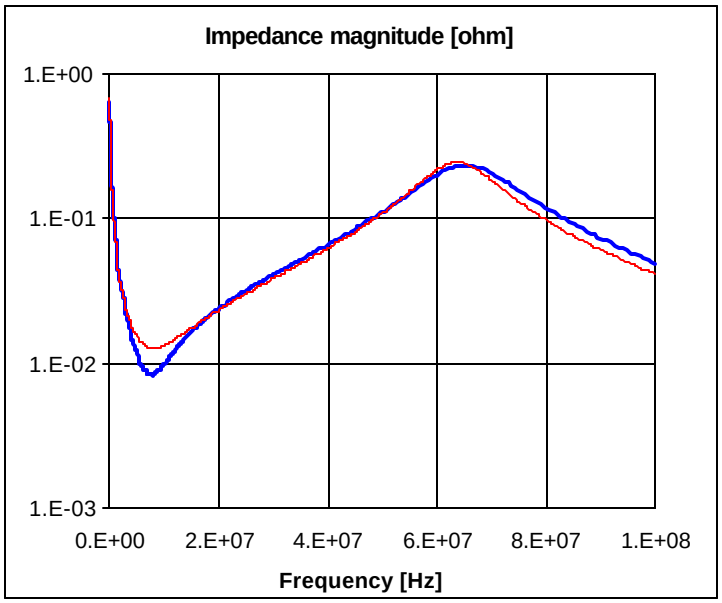


Figure 16.: Illustration of the degree of correlation obtained with the R-L via-pad model. Solid line: simulated, triangles: measured. The same via model yields similar good correlation at all of the tested plane locations, for both self and transfer impedances.



a)



b)

Figure 17.: Correlation at 8MHz (a) and 62MHz (b) between measured (heavy line) and simulated (thin line) impedance of test board with one piece of capacitor attached.

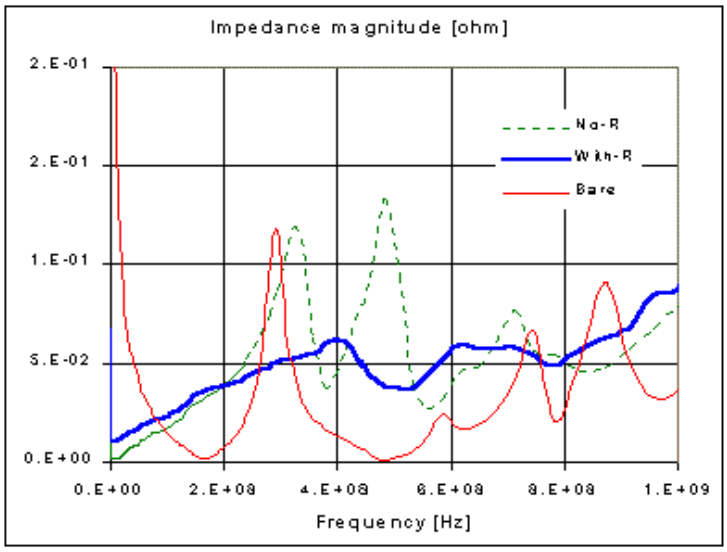
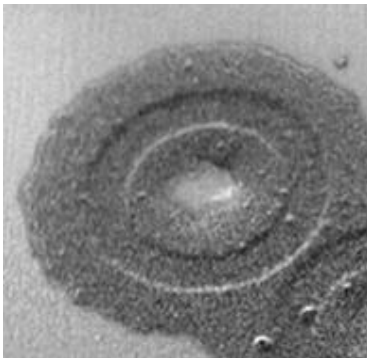
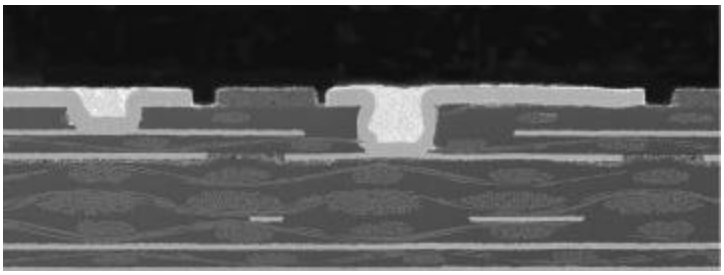


Figure 18: Self-impedance measured on the 10"x5" test board with 26 pieces of low-ESR IDC parts with and without embedded resistors. The three traces: a) thin continuous line: impedance of the bare board (for reference), b) dashed line: impedance of the same board without embedded resistors, and c) solid heavy line: impedance with embedded resistors. Note the reduction of impedance peak at 324 MHz from 0.119 ohms to 0.052 ohms, and at 480MHz from 0.133 ohms to 0.038 ohms.

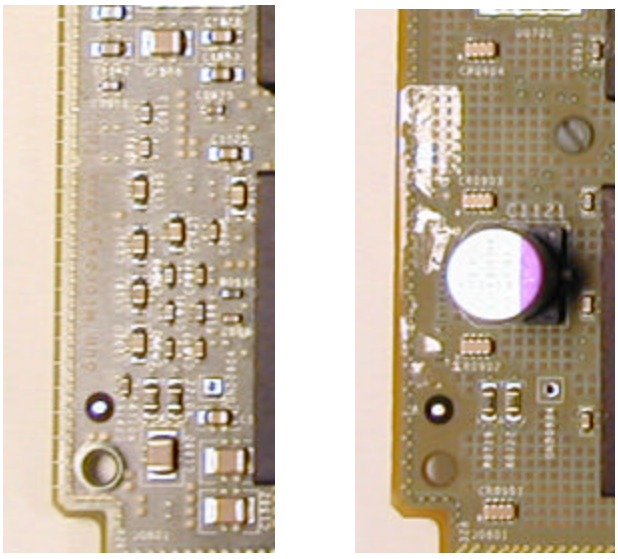


a)



b)

Figure 19: a) ABR^{TM} embedded resistor on inner layer, b) cross section at the printed resistor of the finished module card.



a., b.,

Figure 20: Illustration of savings in component count and board area on a module board: a) board detail of module with more than 250 pieces of mid-frequency bypass capacitors, and b) same module with 50 Distributed Matched Bypassing capacitors.

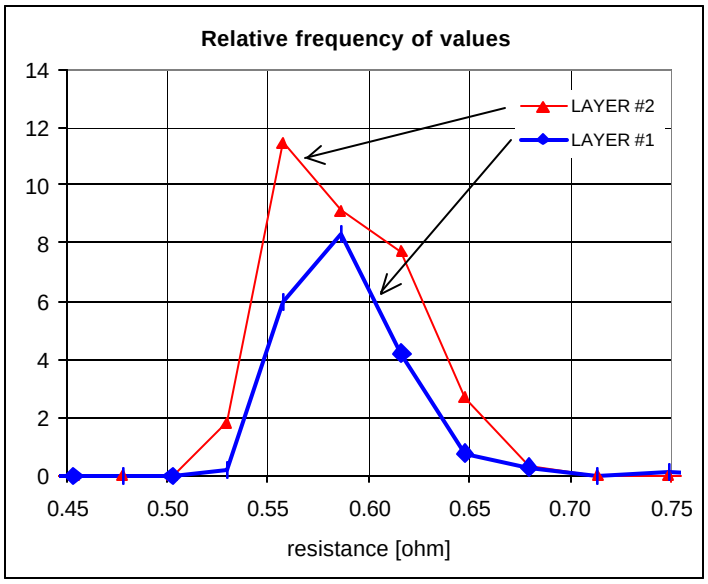


Figure 21.: Relative frequency of embedded resistance values measured on the two separate DMB layers of board shown in Fig. 20.