Distributed Waveform Generator: A New Circuit Technique for Ultra-Wideband Pulse Generation, Shaping and Modulation

Yunliang Zhu, *Member, IEEE*, Jonathan D. Zuegel, John R. Marciante, and Hui Wu, *Member, IEEE*

***Abstract*—A new circuit technique, the distributed waveform generator (DWG), is proposed for low-power ultra-wideband pulse generation, shaping and modulation. It time-interleaves multiple impulse generators, and uses distributed circuit techniques to combine generated wideband impulses. Built-in pulse shaping can be realized by programming the delay and amplitude of each impulse similar to an FIR filter. Pulse modulation schemes such as on-off keying (OOK) and pulse position modulation (PPM) can be easily applied in this architecture. Two DWG circuit prototypes were implemented in a standard 0.18 μm digital CMOS technology to demonstrate its advantages. A 10-tap, 10 GSample/s, single-polarity DWG prototype achieves a pulse rate of 1 GHz while consuming 50 mW, and demonstrates OOK modulation using 16 Mb/s PRBS data. A 10-tap, 10 GSample/s, dual-polarity DWG prototype was developed to generate UWB pulses compliant with the transmit power emission mask. Based on the latter DWG design, a reconfigurable impulse radio UWB (IR-UWB) transmitter prototype was implemented. The transmitter's pulse rate can be varied from 16 MHz range up to 2.5 GHz. The bandwidth of generated UWB pulses is also variable, and was measured up to 6 GHz (-10 dB bandwidth). Both OOK and PPM modulation schemes are successfully demonstrated using 32 Mb/s PRBS data. The IR-UWB transmitter achieves a measured energy efficiency of 45 pJ/pulse, independent of pulse rate.**

***Index Terms*—Arbitrary waveform generator, distributed circuits, pulse generation, pulse modulation, pulse shaping circuits, ultra wideband.**

I. Introduction

PULSE generation, shaping and modulation are critical functions in wireline communications, high speed instrumentation, and pulse radar systems. Recently, ultra-wideband (UWB) communications has emerged as one of the future generation wireless technologies, and generated new interests in high speed pulse generation and processing. Particularly, impulse radio UWB (IR-UWB) promises significantly higher data rate in low-cost, low-power wireless applications than conventional narrow-band systems such as Bluetooth [1] and Zigbee [2]. For example, IR-UWB has been specified as an alternative physical layer for the wireless connectivity in IEEE 802.15.4a standard, with a data rate up to 27.24 Mbps [3] as compared to Zigbee's 250 kbps. Compared to the more mature multi-band OFDM UWB, IR-UWB systems can have much simpler architectures, consume significantly less power, and are more versatile under different channel conditions.

As shown in Fig. 1(a), the UWB band spans 7.5 GHz (from 3.1 to 10.6 GHz), the largest bandwidth for any commercial wireless systems[1]. The transmit power is specified to very low, e.g., below -41.3 dBm/MHz in U.S. (Fig. 1(b), to avoid the interference with other existing wireless systems in the same frequency band. The challenge in building an IR-UWB system lies in two folds: (a) how to achieve the large signal bandwidth, or equivalently, how to generate and process the UWB pulses with sub-nanosecond time resolution; and (b) how to accomplish this with low power consumption and small circuit complexity, which translates into low cost. The latter requirements are particularly important for battery-powered IR-UWB systems in applications such as wireless sensor networks. A fully integrated IR-UWB transceiver in CMOS technologies are conceived as the solution to address such conflicting requirements, thanks to CMOS's well-known cost advantages, system-on-chip (SoC) capabilities, and aggressively improving device performance [4].

Within and nearby the UWB band, there already exist other wireless systems with much higher transmit power, e.g., 802.11a at 5.2 GHz with 4 dBm/MHz (Fig. 1(a). Hence there are stringent requirements on spectrum control and narrow-band interference suppression [5], [6]. To mitigate the interference problem with other wireless systems in the 5 GHz band, the UWB band is typically divided into two parts: a low band (3.1 to 4.8 GHz) and a high band (6 to 10.6 GHz), and either or both bands can be used [3]. Therefore, it is critical to generate UWB pulses which are (a) compliant with regulatory transmit power emission masks (Fig. 1(b), and (b) robust in a crowded narrow-band interference environment [7]. Both require a stringent control on the UWB pulse spectra, or equivalently, the pulse shapes.

Further, different regional regulations will require various pulse shapes or spectra, as shown in Fig. 1(b), therefore a

Manuscript received May 20, 2008; revised October 24, 2008. Current version published February 25, 2009. This work was supported by the U.S. Department of Energy (DOE) Office of Inertial Confinement Fusion under Cooperative Agreement No. DE-FC52-92SF19460, the University of Rochester, and the New York State Energy Research and Development Authority. The support of the DOE does not constitute an endorsement by the DOE of the views expressed in this paper.

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Digital Object Identifier 10.1109/JSSC.2009.2013770

[1]There is another allocated UWB band below 1 GHz mainly for imaging and localization applications, which is not the focus of this work.

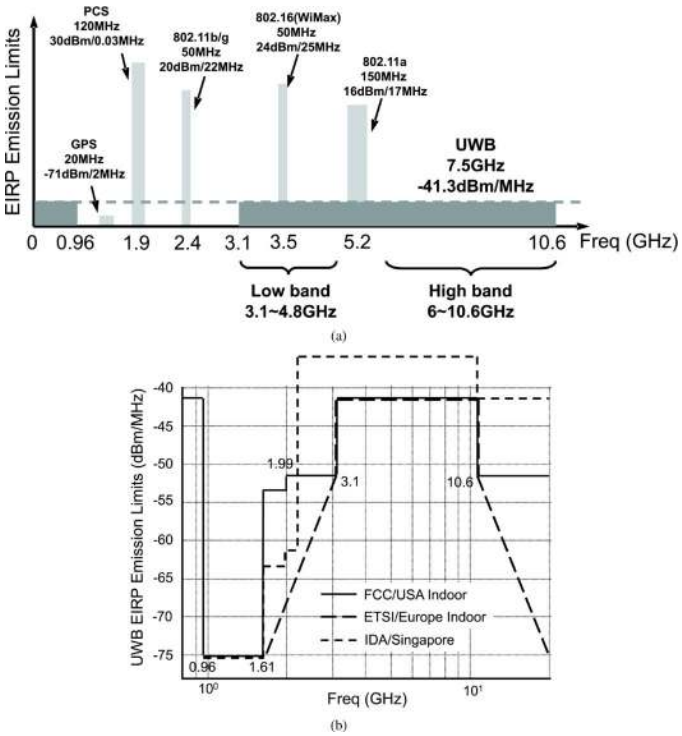

Fig. 1. UWB spectrum: (a) UWB band allocation, and other existing wireless networks; (b) UWB emission mask of different regions.

reconfigurable pulse generator, which can be tuned *in situ* after fabrication, is highly desirable. To reliably achieve the best system performance, a reconfigurable UWB pulse generator is also needed to accommodate process, voltage, and temperature (PVT) variations, which has become increasingly problematic in nanoscale CMOS technologies. Such adaptive architectures are becoming more attractive as CMOS technologies further scale, and even more critical as more emerging wireless systems such as WiMax [8] compete with IR-UWB applications on the spectrum usage.

Another adaptive method to improve the performance of an IR-UWB system is to use different modulation schemes according to the channel environment, type and amount of transmit data, as well as power budget [9]. For example, in a wireless sensor network, a simple modulation scheme such as pulse position modulation (PPM) can be used for a small amount of data like temperature at low data rate to save power, while a more advanced modulation such as quadrature phase shift keying (QPSK) would be more energy efficient to transmit a larger data package like video. Variable modulation capability, therefore, is highly desirable for an IR-UWB system, if it can be implemented without significant overhead in circuit complexity and power consumption.

In this paper, we present a new circuit technique, *distributed waveform generator* (DWG), for low cost, low power, reconfigurable, modulation-friendly UWB pulse generation. In Section II, conventional UWB pulse generation approaches are briefly reviewed. In Section III, the general DWG architecture is proposed based on the analysis of UWB pulse characteristics. We also analyze DWG's built-in pulse shaping and modulation capabilities, as well as its performance limitations. In Section IV, the design of two DWG prototypes in 0.18 μm standard digital CMOS are presented. The first prototype is a 10-tap, 10 GSample/s single-polarity DWG to demonstrate its pulse generation, filtering and modulation capabilities. The second prototype is an IR-UWB transmitter based on a 10-tap, 10 GSample/s dual-polarity DWG. In Section IV, measurement results are reported with example waveforms to show the reconfigurability and variable data rate. OOK and PPM modulation capabilities are also demonstrated.

II. UWB Pulse Generation Approaches

Currently, UWB pulse generators fall into three main categories, as shown in Fig. 2. In the first approach, a baseband pulse is generated using device characteristics, and then up-convert it to the target frequency band [10], [11]. Similar to conventional narrow-band systems, this carrier-based approach circumvents the difficult task of directly generating UWB pulses. The pulse spectrum is determined in the baseband, hence can be easily changed. However, circuit complexity and power consumption of the transmitter become prohibitively high for low cost, low power IR-UWB systems due to the need for a phase-locked loop (PLL) as the local oscillator (LO), and a mixer for up-conversion, both operating at multiple GHz range. Further, it is equally challenging to generate baseband pulses with large bandwidth, and hence the up-converted UWB pulses typically only occupy either the low band or part of the high band. Some clever circuit techniques can be applied to simplify the architecture and reduce the power consumption, e.g., by directly switching on and off an RF oscillator using the modulated baseband data instead of up-conversion using a mixer [12]. Due to the transient time to start and stop the oscillator, however, the generated pulse width is usually quite large (more than 3 ns in [12]), and hence generated UWB pulses can only occupy a small bandwidth (528 MHz in [12]).

A second approach is to generate a very short baseband pulse, which generally does not meet the spectra requirement of UWB systems, with even larger signal bandwidth than the first approach, and then shape it using a passive bandpass filter to the desired UWB pulses [13], [14]. In other words, it relies on the pulse shaping filter to generate the UWB pulses with specific pulse shapes and spectra. Again, due to the bandwidth limitation on the baseband pulse, the filtered UWB pulse usually occupies only the low-band. Further, passive filters are difficult to integrate on-chip due to the large component size. They also cause significant performance degradation due to the low quality factor (Q) of on-chip inductors, capacitors, and transmission lines. Therefore, these pulse shaping filters are typically implemented off-chip [15], and hence have very limited tuning capability after fabrication. A UWB transmitter based on this architecture, therefore, can only generate a specific pulse shape, and is hardly reconfigurable. Active FIR filters have also been proposed [6], [16]–[18], which tend to consume significantly amount of power due to the need to propagate and distributedly amplify a wideband impulse.

The third approach for UWB pulse generation is waveform synthesis based on high speed digital-to-analog converters

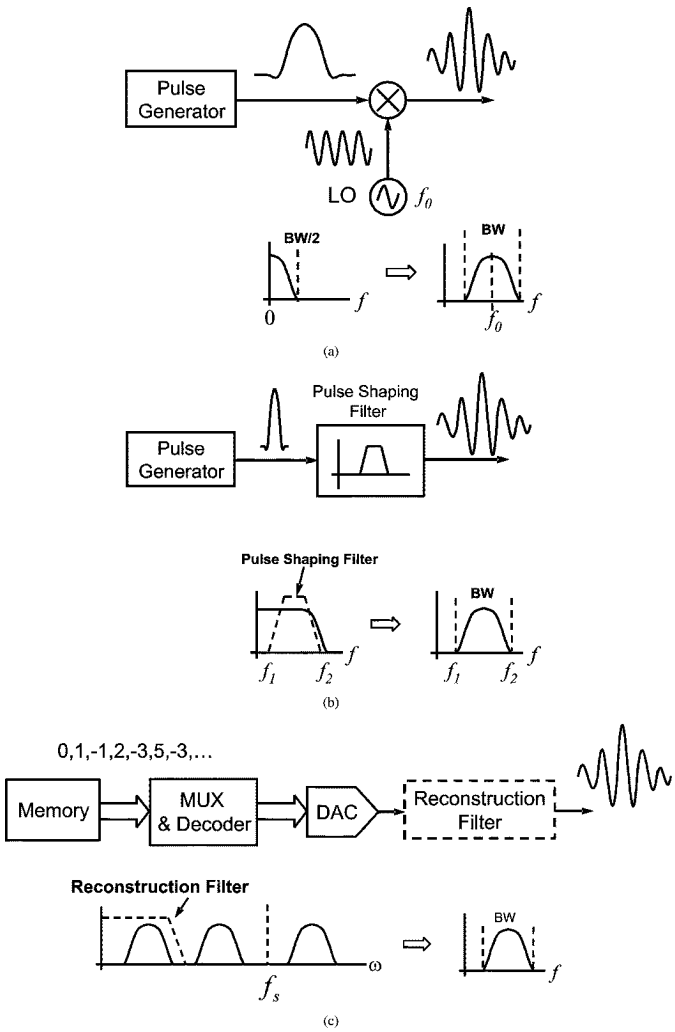

Fig. 2. Current IR-UWB pulse generation approaches: (a) up-conversion; (b) pulse shaping; (c) waveform synthesis. Both generated waveforms and pulse spectra are shown. Note that in the waveform synthesis approach, the spectrum is periodic over the sampling frequency f_s.

(DAC) [19]. High speed DACs with good resolution can generate almost arbitrary pulse shapes and hence are fully reconfigurable as UWB pulse generators. A DAC-based UWB pulse generator, however, requires Nyquist rate sampling, e.g., at least 10 GSample/s for the low band, and over 20 GSample/s for the high band. The high sampling rate poses a challenge not only for the DAC, but also for generating the input digital data stream, which usually requires power-hungry high speed digital circuits, such as current-mode logic, using advanced technologies such as SiGe BiCMOS [19]. Therefore, it is imperative to leverage some analog and RF techniques to reduce the sampling rate and power requirement in a waveform synthesis architecture. For example, UWB pulse generation has been demonstrated using multiple edge combiner or digital switching circuits [20], [21]. Although consuming relatively low power, these circuits did not achieve large bandwidth ($-10-$dB bandwidth of less than 2 GHz in [21]), and were only capable of generating a specific pulse shape (e.g., pseudo-raised-cosine pulse envelop [20]).

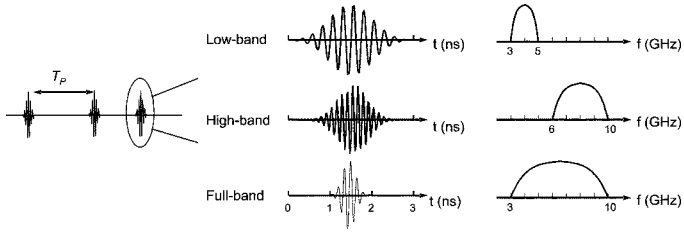

Fig. 3. IR-UWB pulse characteristics.

In this paper, based on the analysis of UWB pulse characteristics, we propose a new circuit technique, *distributed waveform generator* (DWG) [22]. Compared to the existing solutions, the DWG enables the generation of pulses with not only low power consumption, but also reconfigurable spectra and much larger signal bandwidth.

III. Distributed Waveform Generator

A. Rationale

As shown in Fig. 3, there are several distinctive features of IR-UWB pulses: (a) They have very short duration, less than 1 ns when the full 7.5 GHz bandwidth is utilized, or only 2 ns for the low band. (b) The large bandwidth translates into a fine time resolution, which requires a Nyquist sampling rate as high as 20 GSamples/s for the full band, and 10 GSample/s for the low band. (c) The pulse rate[2] $f_P = 1/T_P$ varies in a wide range from kHz to hundreds of MHz for different applications. (b) and (c) mean that the duty cycle of the transmit signal (UWB pulse train) can be as low as 0.001%. To save power, therefore, the pulse generator and other circuitry in the transmitter should operate only when a pulse is transmitted, i.e., they should be *duty cycled* [23]. This is a strong argument against the up-conversion approach in IR-UWB transmitters since it is highly inefficient to spend several microseconds to start and stop a PLL, and then transmit for only a few nanoseconds. (d) Pulse shapes are pre-determined and do not change in real time. Even in the case of adaptive pulse shape tuning, the adjustment is needed infrequently, e.g., when the system is powered up or during periodic channel estimations. All these characteristics make a time-interleaved DAC a good candidate for pulse generation of UWB pulses, as shown below.

The technique of *time interleaving* has been widely used in data converters to achieve higher sampling rate [24]. When multiple DACs are time-interleaved, the overall sampling rate increases to $F_s = f_s \cdot N$, where f_s is the sampling clock frequency controlling each DAC, and N is the number of DACs time-interleaved. For the same sampling rate F_s, therefore, the sampling clock frequency f_s is effectively lowered by N, and this would significantly reduce the power consumption of each DAC, considering that the power dissipation of CMOS digital circuits is

[2]Here we intentionally distinguish pulse rate from data rate or symbol rate since each pulse can potentially carry multiple bits of information, and each symbol can have multiple pulses. We also avoid using *pulse repetition rate* since it may cause confusion in the modulated case.

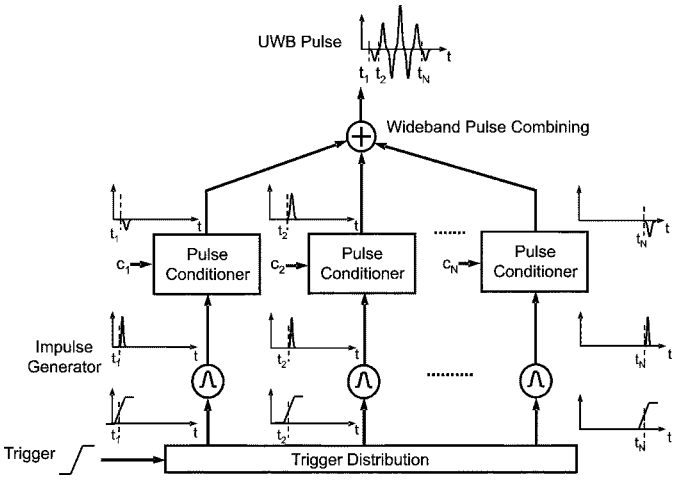

Fig. 4. Distributed waveform generator architecture.

proportional to the clock frequency. This power saving determines that the total power consumption of a time-interleaved structure remains largely constant even when N is large. Therefore, a time-interleaved DAC is well suited for the high sampling rate requirement of IR-UWB pulses.

Second, the low duty cycle and fixed pulse shapes of IR-UWB pulses mean that the input data rate can be very low. Indeed, the input data can be fixed values, if the number of DACs N is large enough so that the total sampling period T_s of the time-interleaved structure covers the whole UWB pulse width. In this case, generation and distribution of the high speed input digital data stream are not needed, and hence the power consumption of UWB pulse generation can be significantly reduced. For example, 10-way time interleaving is sufficient to generate a 1 ns UWB pulse with 100 ps time resolution, i.e., a sampling rate of 10 GSample/s.

On the other hand, the number of DACs N cannot be very large in a time interleaving architecture because of the bandwidth limitation at the output node. The pole at the output node of high-speed DACs usually dominates their settling time. Apparently, the settling time of each DAC in a time-interleaved architecture needs to be shortened correspondingly to accommodate N samples within each sampling clock cycle $T_s = 1/f_s = N/F_s$, i.e., the sampling period $t_s = 1/F_s = T_s/N$ needs to be greater than the settling time of each DAC, and this eventually limits F_s. Hence, new circuit techniques are needed to address the settling time problem to achieve the potential large number of DACs and high sampling rate.

Therefore, the challenges to generate UWB pulses using a time-interleaved architecture lie in (a) how to achieve high sampling rate with low power consumption, which essentially requires a large N; (b) how to overcome the limitation on the overall sampling rate due to settling time.

B. DWG Architecture

A DWG is a special time-interleaved circuit custom developed for IR-UWB pulse generation, which fully utilizes the properties of UWB pulses. Fig. 4 shows the generic architecture of the proposed DWG. In this architecture, a UWB pulse is generated by combining impulses[3] generated by multiple impulse generators in a time-interleaved fashion. The trigger signal is distributed to each impulse generator by the trigger distribution block, which enables impulses to be generated at specific sampling times. These impulses are then independently conditioned, i.e., changed to a desired pulse shape, polarity and amplitude, by a pulse conditioner block in each path (called *tap*), and then combined to form the output pulse waveform by a wideband pulse combining circuit. By changing the characteristics of each impulse generator and conditioner, different output pulse waveforms and spectra can be generated.

There are several distinctive properties of this DWG architecture: First, the trigger signal runs at the pulse rate f_P, which is usually much lower than the Nyquist sampling rate F_s. Note that F_s is determined by the trigger delay between adjacent taps, and is hence independent of f_P. Generally, low power digital delay lines can be employed for this trigger distribution. Second, the impulse generators are assisted by the pulse conditioner, and isolated from the output. Hence it can be implemented as a digital circuit, optimized for short settling time, and directly benefits from the fast switching characteristics of CMOS transistors. Third, in this architecture, large analog bandwidth is only required for the pulse conditioner and pulse combiner at the output. This is similar to the bandwidth challenge in wideband amplifiers, and can be addressed by leveraging distributed circuit techniques [25], as discussed in Sec.III-G below, and in the prototype DWG implementations. Lastly, a DWG is fully reconfigurable by changing the sampling time and pulse width of each impulse generator, and more importantly, by tuning the characteristics of each pulse conditioner.

C. Peak Sampling

Because UWB pulse spectra are of the bandpass type (Fig. 3), the lack of low-frequency components means that the time domain waveforms exhibit alternating peak and zero points. This property can be utilized to reduce the number of sampling points to be generated. Considering two sampling schemes shown in Fig. 5, to generate a UWB pulse using the full band, the Nyquist sampling requires 20 GHz sampling frequency as in Fig. 5(a). In *peak sampling*, the sampling points are located at the peak and zero points. Since the samples at zero points do not need to be generated, the sampling rate can be effectively reduced by half, to 10 GHz in Fig. 5(b). Note that this may introduce some distortion on the signal spectrum since peak and zeros points may not be uniformly distributed. The pulse spectra generated using Nyquist sampling at 20 GSample/s and peak sampling at 10 GSample/s are compared in Fig. 5(c), and the distortion is shown to be very small within 10 GHz bandwidth. Therefore, peak sampling is an effective scheme to reduce sampling rate in UWB pulse generation, and will be applied in DWG implementations to further reduce the power consumption.

[3]Here we use *impulse* to emphasize the pulse generated by each impulse generator is ultra-short, and to distinguish it from the overall generated UWB pulse.

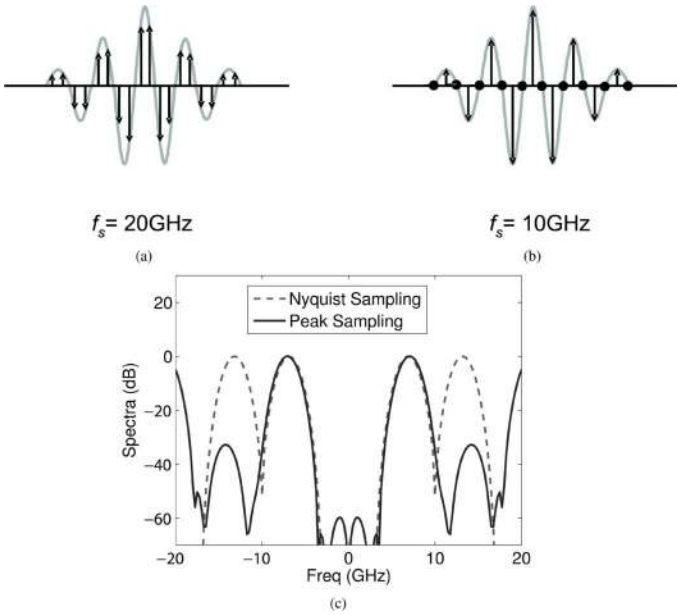

Fig. 5. Different sampling schemes to generate UWB pulse: (a) Nyquist sampling; (b) peak sampling; (c) spectra of the sampled signal using these two sampling schemes.

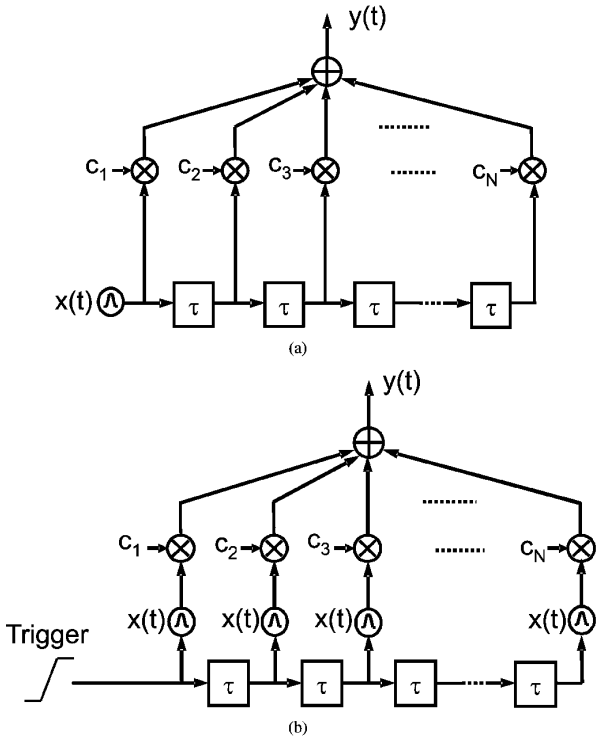

Fig. 6. Similar to (a) a generic transversal filter, a DWG can be considered (b) a transversal filter with the signal source embedded.

D. Built-In Pulse Shaping

A DWG can also be treated as a transversal finite impulse response (FIR) filter. In a generic transversal FIR filter, input signal $x(t)$ and its delayed versions are multiplied by different coefficients $c_1, c_2, \ldots, c_N$ and then summed to generate the output signal $y(t)$, as shown in Fig. 6(a). The transfer function of such a FIR filter is determined by the coefficients and the tap delay τ. To see the similarity between the FIR transversal filter and the DWG, the architecture of DWG is re-drawn in Fig. 6(b). Instead of having input signal $x(t)$ fed into the circuit, $x(t)$ is generated locally within each tap by the impulse generators. Note that each impulse generator is assumed to generate an identical impulse. The pulse conditioner can change the impulse amplitude, which is equivalent to multiplying each generated pulse $x(t)$ by a coefficient. So a DWG architecture can easily realize built-in pulse shaping functions.

The output of a DWG can be described in the time domain as

$$y(t) = \sum_{k=1}^{N} c_k x(t - \tau_k) \tag{1}$$

where c_k is the tap coefficient, and τ_k is the delay on the trigger distribution. Therefore, the output waveform $y(t)$ is determined by three factors, the coefficients c_k, the delay τ_k and the pulse shape $x(t)$ generated by each impulse generator. For a typical DWG with uniform tap delay τ, the frequency response is given by

$$Y(j\omega) = X(j\omega) \sum_{k=1}^{N} c_k \exp(-jk\omega\tau) = X(j\omega)H(j\omega) \tag{2}$$

where

$$H(j\omega) = \sum_{k=1}^{N} c_k \exp(-jk\omega\tau) \tag{3}$$

$X(j\omega)$ is the spectrum of the impulse signal $x(t)$, and $H(j\omega)$ is an FIR filter transfer function, which is determined by tap coefficients c_k and the tap delay τ. Equivalently, the DWG has an "impulse response" of

$$h(t) = \sum_{k=1}^{N} c_k \delta(t - k\tau). \tag{4}$$

Thus, the output signal spectrum $Y(j\omega)$ can be shaped by changing either $X(j\omega)$ or $H(j\omega)$. In practice, $X(j\omega)$ typically exhibits a low-pass response, and sets the maximum achievable high frequency of $Y(j\omega)$. To achieve large signal bandwidth for the generated UWB pulses, it is critical to minimize the pulse width of $x(t)$ and hence ensure $X(j\omega)$ would not limit $Y(j\omega)$. Under such conditions, $H(j\omega)$ will solely determine the pulse shape, and the DWG becomes fully reconfigurable. More importantly, the independence of $Y(j\omega)$ from $X(j\omega)$ will avoid the adverse effects of mismatch between tap responses.

Some example waveforms and spectra of $H(j\omega)$ for low-band and full-band UWB are shown in Fig. 7. The tap delay and number of taps are selected to be feasible for implementation using the DWG architecture. As in Fig. 7(a), to generate a low-band UWB pulse with 2.5 ns pulse duration, 20 taps with 130 ps tap delay is needed. For the full-band UWB pulse generation, 10 taps with 80 ps tap delay is used, as in Fig. 7(b).

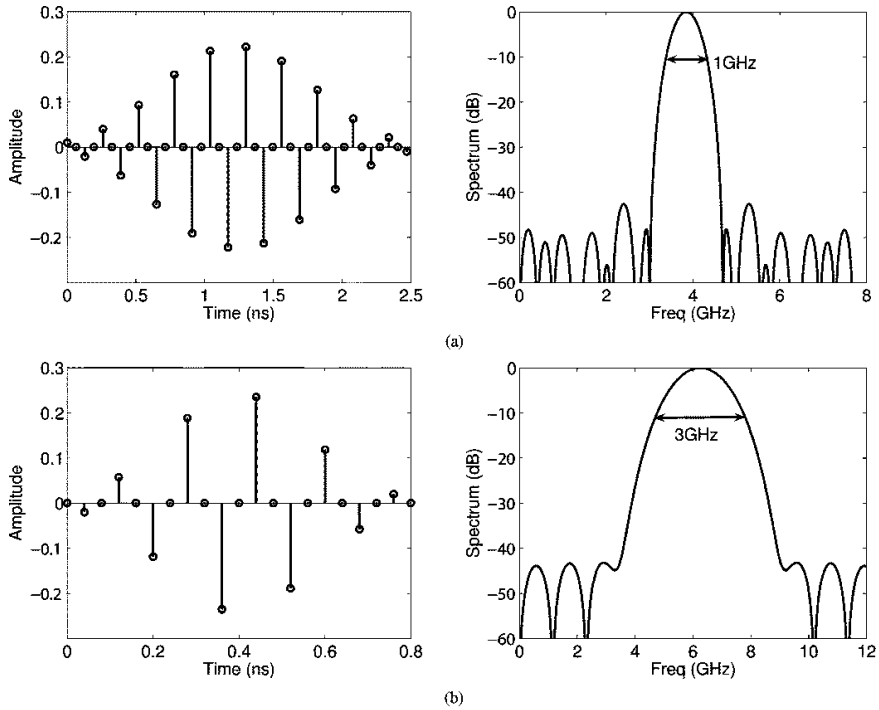

Fig. 7. IR-UWB pulses and spectra generated using ideal impulses and peak sampling (a) $\tau = 130$ ps and $N = 20$; (b) $\tau = 80$ ps and $N = 10$.

Therefore, a DWG can generate UWB pulses with reconfigurable spectra using this built-in pulse shaping capability.

E. Modulation Capabilities

Another advantage of the DWG architecture is that pulse modulation can be easily employed by performing modulation on the trigger signal, and directly control the on/off and position of generated UWB pulses. For example, as shown in Fig. 8, OOK modulation can be implemented by gating a pulse rate clock using the baseband digital data stream to generate an OOK modulated trigger to the DWG. Similarly, PPM modulation can be applied to the pulse rate clock signal by shifting the trigger position. The DWG enables the modulation to be done on the trigger digitally at the pulse rate *before* the pulse generation, instead of on the generated UWB pulses analogly as in a *post-generation* modulation scheme. This removes the need for an analog modulator with large RF bandwidth, and replace it with a low power digital modulator operating at the low pulse rate.

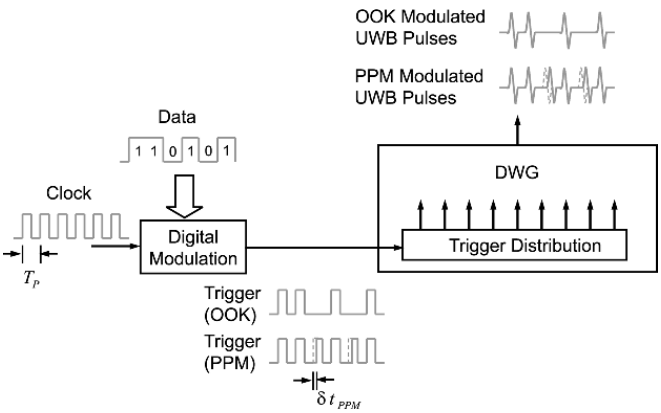

Fig. 8. OOK and PPM modulations are performed on the trigger signal in DWG.

F. Performance Limitations

There are several factors that ultimately limit the performance of a DWG. The first one is the response of each individual tap in the DWG, represented by $X(j\omega)$. After impulses are generated by the fast-switching impulse generators, the pulse conditioner still needs large analog bandwidth to process the impulses. In the circuit design part of this paper, we will show that the bandwidth of the pulse conditioner is the limiting factor for pulse shape accuracy in DWG. Second, the use of time-interleaving requires accurate timing control, which is mostly determined by the trigger distribution block. Systematic delay mismatch and jitter in the trigger distribution can cause waveform distortion and introduce error terms into the FIR response $H(j\omega)$. Third, the analog bandwidth of the pulse combining block is very critical because limited bandwidth can attenuate the pulse amplitude and slow down the rise/fall time of the waveform. To address this issue, a distributed circuit topology based on on-chip transmission lines is utilized in the prototype DWG implementations. Both the pulse combining bandwidth and timing jitter limit the number of taps for time-interleaving in the DWG architecture, which eventually set an upper limit on the maximum achievable pulse duration.

G. Wideband Pulse Combining

To achieve the large analog bandwidth needed for pulse combining in DWG, we can utilize a wideband circuit technique, *traveling wave power combining*, which is widely used in distributed amplifiers [25]. In this case, an on-chip transmission

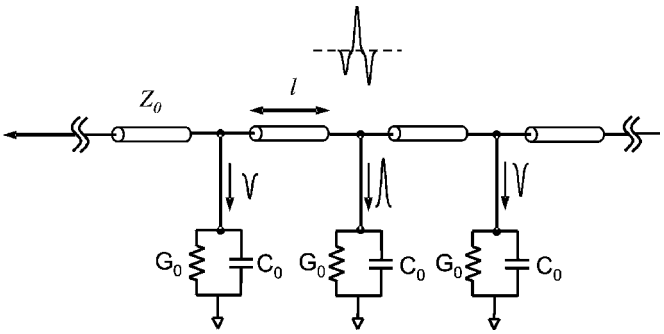

Fig. 9. Loaded transmission line for wideband pulse combining.

line is used to combine the conditioned impulses from each pulse conditioner. The output impedance of the pulse conditioner is modeled as parallel G_0 and C_0, as in Fig. 9, which load the transmission line. Conditioned impulses form a traveling wave on the loaded transmission line. Such a distributed circuit structure extends the bandwidth at the output node since the parasitic capacitance and conductances of all pulse conditioner effectively become part of the *loaded* transmission line structure. The output conductances of pulse conditioners need to be minimized to reduce the loss. If we assume that loss can be neglected, the bandwidth of the output node is mainly determined by the cut-off frequency of the capacitively loaded transmission line, which can be expressed as [26]

$$f_c = \frac{1}{\pi\sqrt{L\left(\frac{C+C_0}{l}\right)}} \tag{5}$$

where L and C represent the series inductance and shunt capacitance per unit length of the *unloaded* transmission line, and l is the length of transmission line per tap. Thus, the cut-off frequency f_c only depends on the transmission line parameters (L, C, l) and C_0, independent of N. So the settling time is not degraded for a large N are employed in the DWG architecture. In practice, loss introduced by the transmission line itself and G_0 eventually limits the achievable bandwidth.

Because the loaded transmission line needs to impedance match the load which is 50 Ω typically for a UWB antenna or test instruments, it is important to analyze the effective characteristic impedance of the loaded transmission line

$$Z_L = \sqrt{\frac{R+j\omega L}{(G+j\omega C)+\left(\frac{G_0}{l}+\frac{j\omega C_0}{l}\right)}} \tag{6}$$

which is lower than that of the *unloaded* transmission line (Eqn. 6 without G_0, C_0). Thus, the unloaded transmission line needs to designed as a high impedance line with low loss, so that the loaded impedance Z_L can achieve the desired impedance (50 Ω), while allowing a large N. Due to the lossy silicon substrate and restrictive design rules, this poses significant challenges, and a new on-chip transmission line configuration is needed, as shown in Section IV.

Note that in the DWG, the timing control function is realized by the trigger distribution block. So the transmission line based pulse combining block does not need to generate delay to meet the power combining requirement, which is different from the transmission lines employed in conventional distributed amplifiers. Thus, the design of transmission line can be optimized for bandwidth and impedance matching without the constraint from delay.

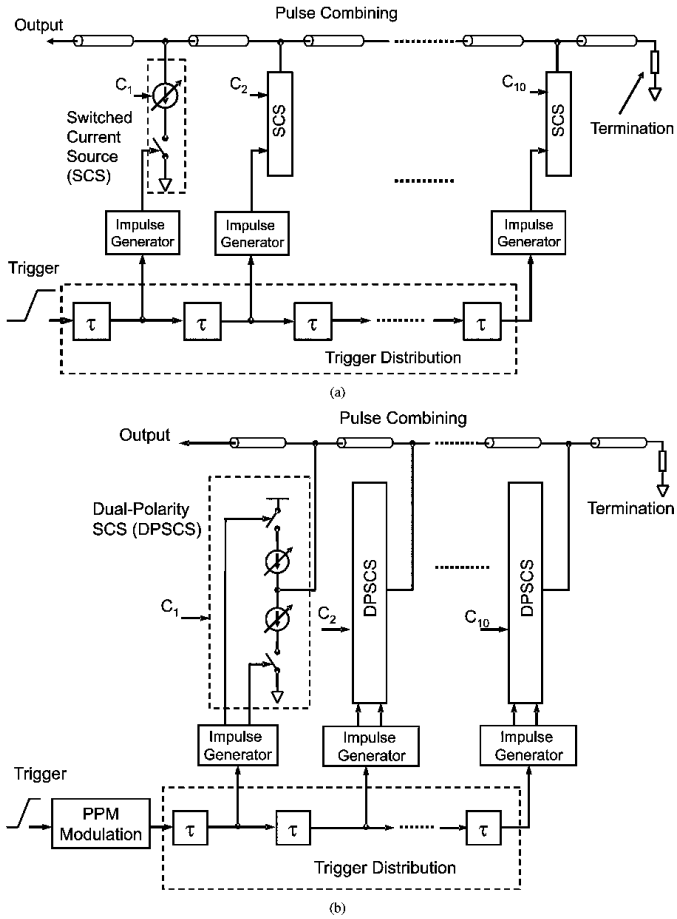

Fig. 10. (a) Schematic of the single-polarity DWG; (b) Schematic of the dual-polarity DWG.

IV. Circuit Implementation

Two DWG prototypes have been implemented: a single-polarity one for proof of concept, and a dual-polarity one as an IR-UWB transmitter. Fig. 10 shows the schematic of both prototypes. Dual-polarity pulse generation is more desirable for IR-UWB transmitter because UWB pulses are bandpass signals with no DC component, and hence peak sampling can be employed to reduce the sampling frequency, as discussed in Sec.III-C, which requires both positive and negative sample impulses.

In both DWG prototypes, to achieve low power and large tuning range, an asynchronous, current-starved active delay line [27] is used for trigger distribution (Fig. 11). To achieve 10 GSample/s sampling rate (peak sampling) for the whole band, the delay per stage is designed to be nominally 100 ps, and can be tuned by varying the delay-tuning voltage V_{dt} in each delay element to change the fall time of the current-starved inverter. In both prototypes, a single V_{dt} is used for all delay elements and hence the tap delay is uniform. Non-uniform tap

TABLE I
SIMULATED AVERAGE TAP DELAY AND STANDARD DEVIATION (PS)

(a) Single polarity DWG

Temperature	Process corner		
($^\circ C$)	Slow	Typ	Fast
-30	103.86 / 0.058	75.33 / 0.026	61.19 / 0.045
27	112.81 / 0.255	80.17 / 0.062	57.24 / 0.068
55	114.50 / 0.079	82.21 / 0.093	62.95 / 0.037
110	117.43 / 0.105	85.75 / 0.101	66.09 / 0.128

(b) Dual polarity DWG

Temperature	Process Corner		
($^\circ C$)	Slow	Typ	Fast
-30	87.24 / 0.148	63.81 / 0.084	50.20 / 0.071
27	95.38 / 0.070	70.43 / 0.091	55.19 / 0.054
55	98.89 / 0.062	73.35 / 0.108	57.48 / 0.053
110	104.83 / 0.160	78.53 / 0.169	61.62 / 0.151

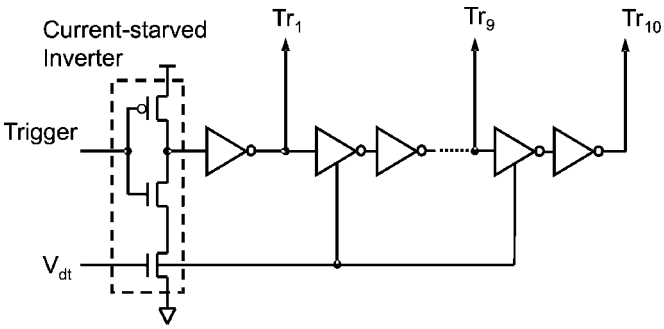

Fig. 11. Active delay line for trigger distribution.

delay can be implemented by employing independent delay tuning for each tap.

The timing accuracy of the DWG is determined by the delay line in both prototypes, and hence is affected by process, voltage and temperature (PVT) variabilities. Table I shows the tap delay variations with temperature and process corners in simulation. The temperature variation is relatively small, while the process variation is noticeable. Delay tuning by V_{dt} can be utilized to compensate for these variations, e.g., during the start-up calibration. A delay-locked loop (DLL) can also be used to improve the timing accuracy over PVT variations.

Impulse generators are implemented as digital switching circuits in both DWG prototypes to utilize the fast switching speed of CMOS transistors and save power. In the single-polarity DWG prototype, the impulse generator is designed based on a glitch generator [28], as shown in Fig. 12(a). At the rising edge of the trigger, a short pulse is generated by the NAND operation of the input step signal and its delayed version. Another NMOS transistor M_3 is added into the feedback path as a voltage controlled resistor. By varying the pulse width tuning voltage

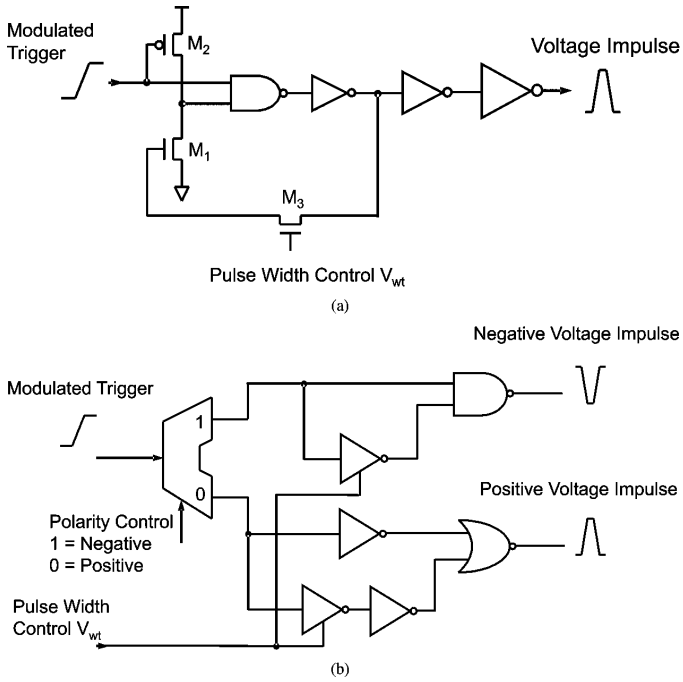

Fig. 12. Impulse generator of (a) the single-polarity DWG and (b) the dual-polarity DWG.

V_{wt}, the time constant of this charging path changes, which tunes the generated pulse width.

The impulse generator in the dual-polarity DWG is designed to generate both positive and negative impulses, as shown in Fig. 12(b). When a rising edge arrives at the trigger input, if the polarity control signal is high, it is steered to the upper signal path, and a short negative impulse is generated by the NAND operation of the input step signal and its delayed version, and vice versa. Since both impulse generators are triggered by the rising edge, return-to-zero coded baseband data can directly drive the DWG to implement the OOK modulation. Note that pulse width tuning is achieved by controlling the amount of delay for the delayed input step signal through a current-starved inverter.

Due to the use of static CMOS logic for trigger distribution and impulse generators, achievable minimum tap delay and pulse width are determined by the propagation delay of full swing signals along CMOS gates. Smaller delay and faster rise time can be achieved by using the current mode logic (CML) at the cost of static power consumption and extra CML-CMOS conversion circuits. For IR-UWB applications, the CMOS implementation proves to be sufficiently fast.

As shown in Fig. 13(a), a switched current source (SCS) is used in the single-polarity DWG prototype for pulse conditioning, specifically amplitude tuning and voltage-to-current conversion. The latter is needed to drive the low impedance (50 Ω) of test instruments or an off-chip antenna. The voltage impulse from the impulse generator switches on and off M_{SW}, and hence generates a current impulse through M_1 and M_2. The amplitude tuning, is achieved by changing the reference current I_{ref} of a cascode current mirror, which ensures the accuracy of I_{ref}. When I_{ref} is low, i.e., the tap coefficient c_k is a very small value, the pole associated with node X becomes

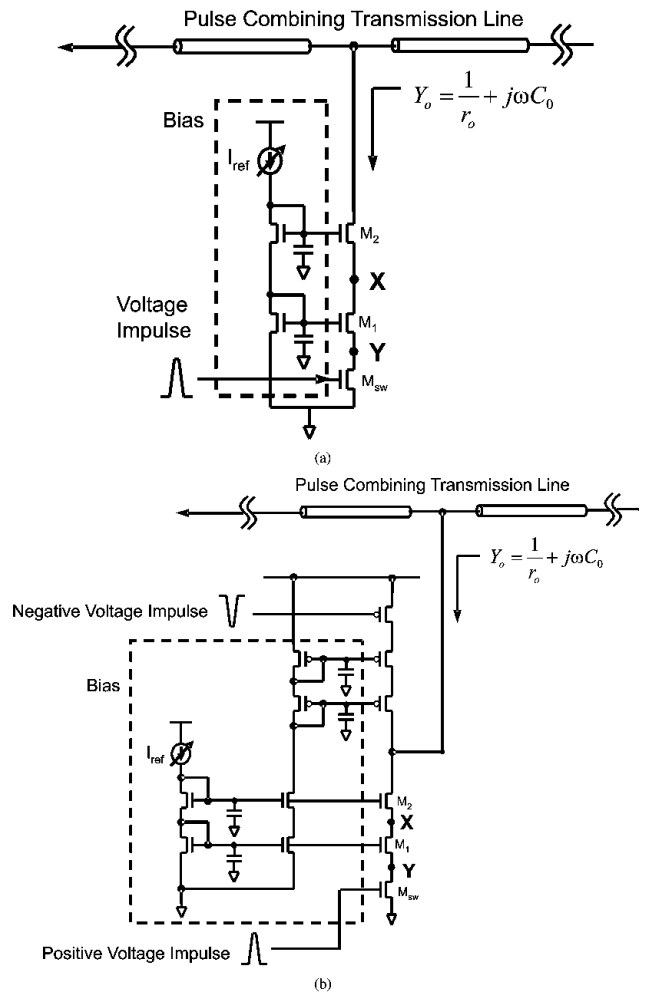

Fig. 13. Schematic of the (a) single-polarity and (b) dual-polarity switched current source for analog amplitude tuning. Part of the output transmission line for pulse combining is also shown.

the dominant pole since the transconductance of transistor M_2 is reduced significantly due to the small current value, as shown in the following equation:

$$\omega_{p,X} = \frac{g_{m2}}{C_X} = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}. \quad (7)$$

The bandwidth reduction caused by this dominant pole distorts the impulse shape, and sets the lower bound of the dynamic range. Note that the pole associated with mode Y is always at very high frequency because of the small on-resistance of the switching transistor M_{SW}. The upper bound of the dynamic range is set by the power consumption limit in our prototypes. The dual-polarity SCS (DPSCS) used in the dual-polarity DWG as shown in Fig. 13(b) has similar circuit topology and performance limitation.

The outputs of all the SCSs are connected to an output transmission line for pulse combining and impedance matching (Fig. 13). In both prototypes, the output transmission line is implemented as a multilayer coplanar waveguide (CPW) transmission line, in which the signal line is built on the top metal layer (M6), and ground planes are built on a different metal layer (M5). The MCPW has lower loss and larger bandwidth than LC artificial transmission lines [29], and can easily satisfy the design rules and metal density requirements in standard CMOS technologies. The output impedance is matched to 50 Ω, which enables the DWG to drive the antenna or test instruments directly.

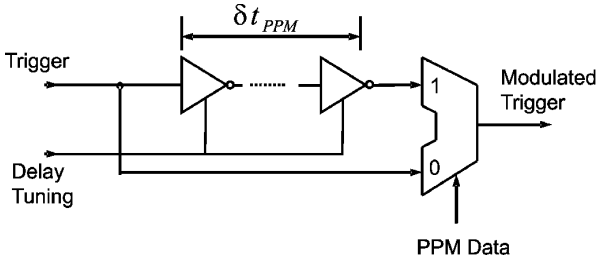

Fig. 14. Schematic of the PPM modulator in the IR-UWB transmitter.

A digital PPM modulator shown in Fig. 14 is added in front of the dual-polarity DWG in the IR-UWB transmitter prototype (Fig. 10(b)). Considering the DWG generates UWB pulses at the rising edge of each trigger signal, the binary PPM is implemented by applying the trigger signal to signal paths and in one path delaying the trigger signal by a time delay δt_{PPM}, followed by a 2:1 multiplexer to select one of these two delayed trigger signals to determine the pulse position.

Both DWG prototypes were fabricated in a commercial standard 0.18 μm digital CMOS technology with low-resistivity substrate. The chip micrograph of the single-polarity DWG and dual-polarity DWG based IR-UWB transmitter prototypes are shown in Fig. 15. Note that the chip area excluding the pad frame is considerably smaller than a typical distributed circuit, e.g., a distributed amplifier [30].

V. Measurement Results

Characterizations of DWG prototypes are performed in both the time domain using a 50 GHz sampling oscilloscope and the frequency domain using a spectrum analyzer. For example, the test setup for the PPM modulation using the IR-UWB transmitter prototype is shown in Fig. 16. Sinusoidal signals from a continuous-wave (CW) signal source is power split into two. One is used as the input trigger for the DWG and the other is used as the trigger for the sampling oscilloscope. External bias tees are used at the input and output of the DWG to provide proper DC bias. Modulation signal is generated using an arbitrary waveform generator (AWG),[4] which is synchronized with the CW signal source by its 10 MHz internal clock. In the OOK test, the AWG instead of the CW signal source is used to directly trigger the DWG, which is not shown in Fig. 16.

A. 10-Tap Single-Polarity DWG

Fig. 17 shows the impulse generated by each tap at the single-polarity DWG output. The tap delays of all ten taps are measured between the middle points of rise edges, and shows good uniformity. The average tap delay is 104 ps with a standard deviation σ of 15.1 ps, which corresponds to a sample rate of 10 GSample/s.

[4]A pulse pattern generator would be ideal in this test, if not limited by the instruments available in our lab.

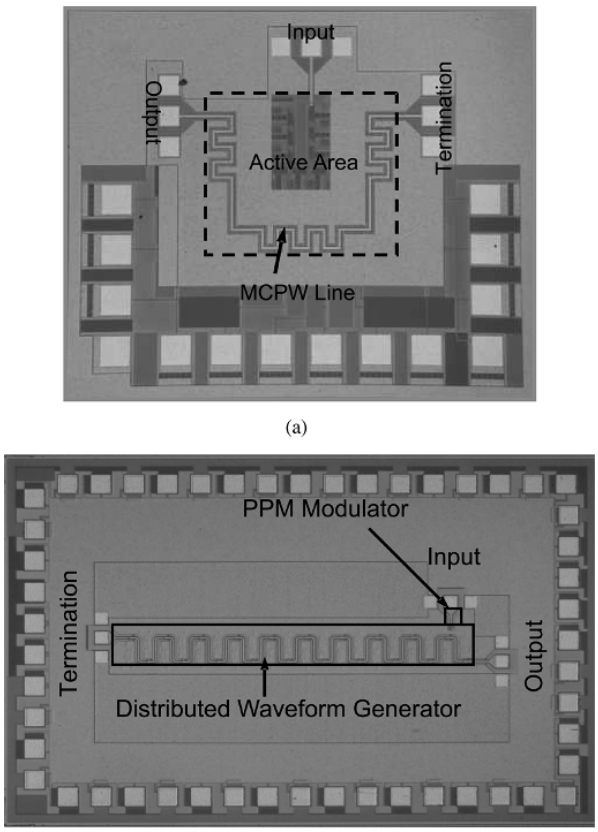

Fig. 15. Chip micrographs of (a) the single-polarity DWG prototype. The chip size is 1.48 mm × 1.24 mm, including pads. The active area is 0.68 mm × 0.5 mm; (b) the dual-polarity DWG based IR-UWB transmitter. The chip size including pad frame is 2.8 mm × 1.8 mm. The active area is 1.6 mm × 0.2 mm.

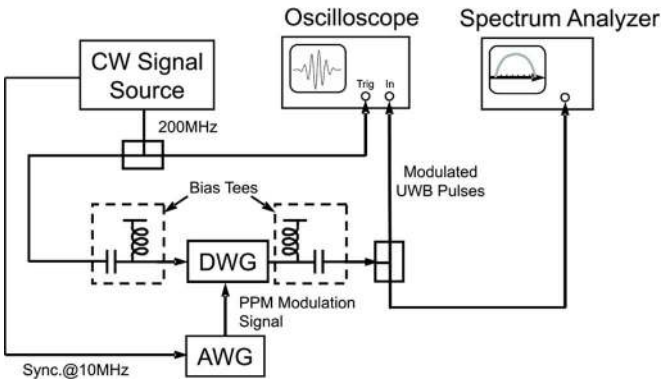

Fig. 16. Test setup for the PPM modulation using the dual-polarity DWG based IR-UWB transmitter prototype.

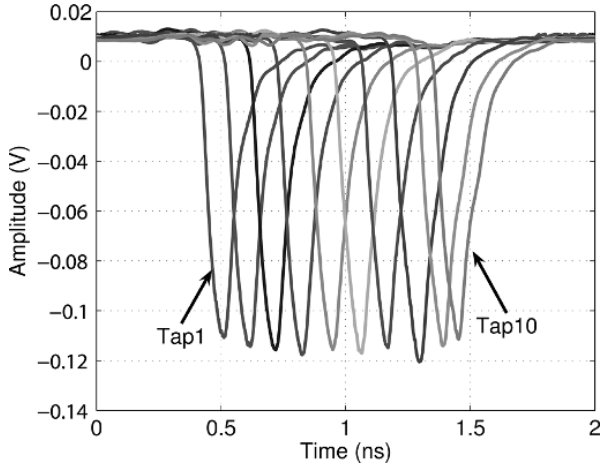

Fig. 17. Impulses generated by each tap of the single-polarity DWG.

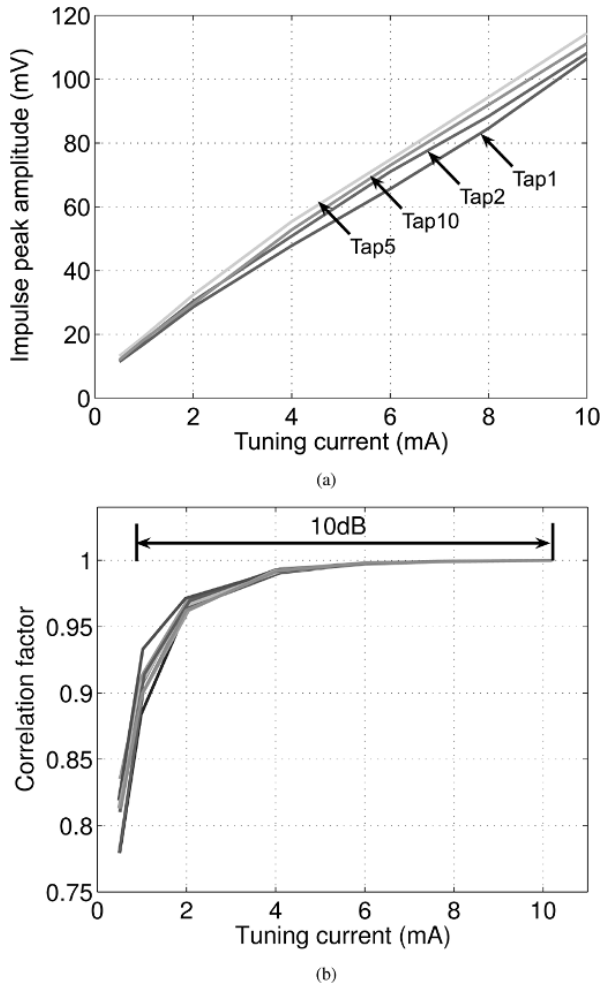

Fig. 18. (a) Pulse amplitude tuning and (b) corresponding pulse shape change.

Note that because the last delay element does not have a load, the delay of tap 10 (73 ps) is much smaller than others. Without tap 10, σ of the tap delay reduces to 7.2 ps. On average, the rise time (10%–90%) is 79 ps with a σ of 3.8 ps, the fall time (90%–10%) is 177 ps with a σ of 3.2 ps, and the minimum pulse width is 140 ps with a σ of 4.6 ps. By varying V_{wt} (Fig. 12(a)), the pulse width of all taps can be tuned from 140 ps to 1 ns. The average tap delay can be tuned over a range of 104 ps to 144 ps, which provides the capability of changing the sampling rate. Characterization results are summarized in Table II. Note that in the following measurements, the DWG is biased to achieve minimum delay and minimum pulse width.

By varying I_{ref} in the SCS, the individual output impulse amplitude can be independently tuned. The pulse amplitude tuning has good linearity as shown in Fig. 18(a), and also conserves the

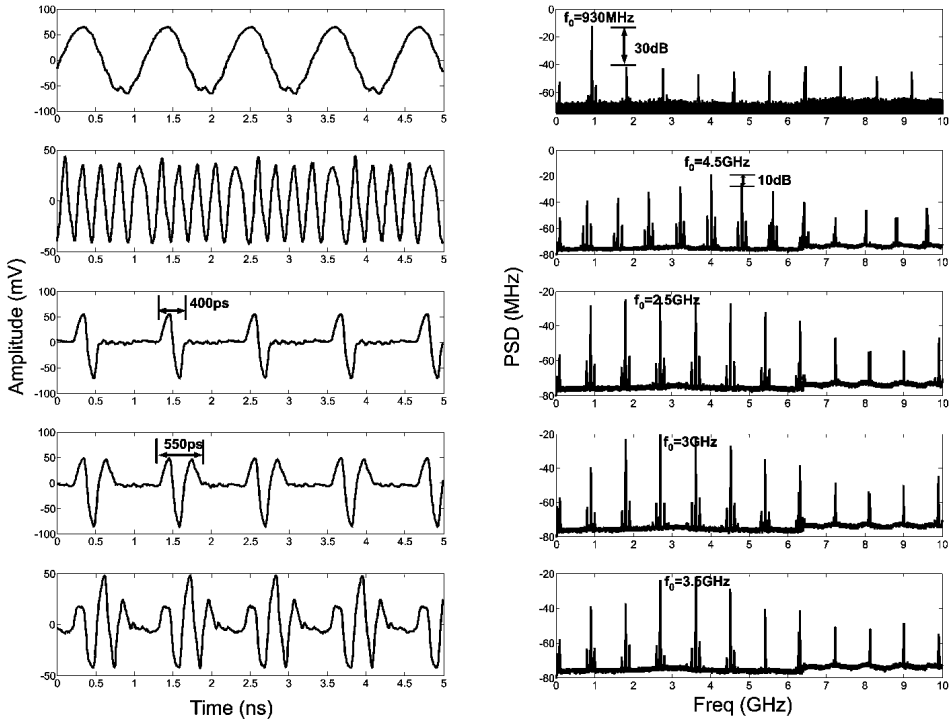

Fig. 19. Example waveforms synthesized using the prototype DWG using all 10 taps.

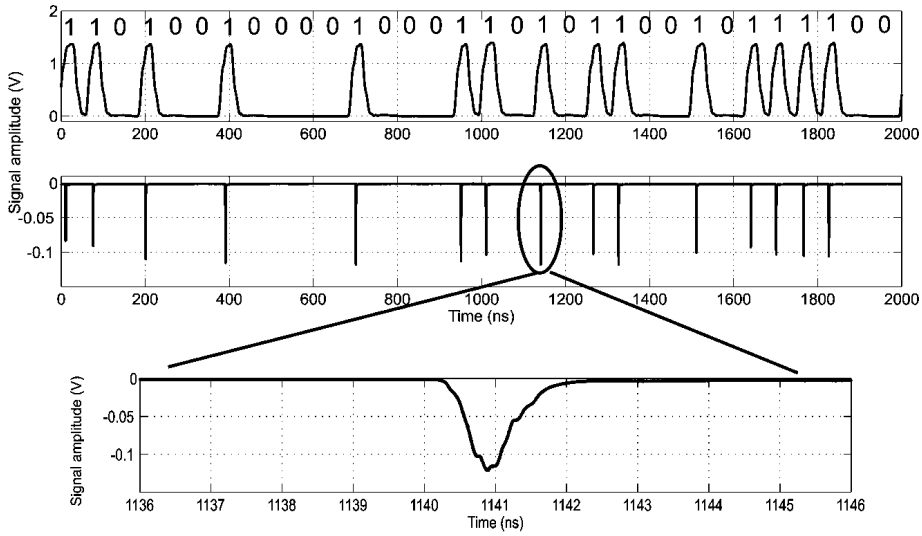

Fig. 20. Output waveform of the prototype DWG driven by PRBS data. The small fluctuation on the waveform amplitude is caused by the limited number of sampling points (4096) in the measurement window.

pulse shape very well, which is quantified using the correlation factor defined below:

$$\text{Correlation factor} = \frac{\int_{-\infty}^{+\infty} y(t) \cdot y_{\max}(t) dt}{\sqrt{\int_{-\infty}^{+\infty} y^2(t)\, dt} \cdot \sqrt{\int_{-\infty}^{+\infty} y_{\max}^2(t)\, dt}} \tag{8}$$

where $y(t)$ is the pulse shape to be quantified, and $y_{\max}(t)$ is the pulse shape with maximum amplitude, which is used as a reference. The DWG can achieve a dynamic range of about 10 dB, given that the correlation factor needs to be larger than 0.9, as shown in Fig. 18(b).

Jitter performance is characterized at the DWG output for each generated impulse. Due to the small duty cycle of the impulse train, self-triggered [31] jitter measurement cannot be performed. So the DWG trigger is also used to trigger the oscilloscope (Fig. 16). The measured RMS jitter values of all 10 taps are in the range of 2.2 ps to 2.4 ps, and the peak-to-peak jitter values are in the range of 13.8 ps to 14.6 ps. The measurement system has an RMS jitter of 1.6 ps (measured). So the additive RMS jitter from the prototype DWG is only 1.6 ps, much smaller than the normal 100 ps tap delay. Therefore, the pulse shape distortion caused by the jitter is negligible.

TABLE II
IMPULSE GENERATED BY THE SINGLE-POLARITY DWG

	Min. (ps)	Max. (ps)	Mean (ps)	σ (ps)
Tap Delay w/o tap 10	73	129	104	7.2
Rise Time	73	86	79	3.8
Fall Time	170	183	177	3.2
Min. Pulse Width	132	143	140	4.6
RMS Jitter	2.2	2.4	2.26	0.2
P-P Jitter	13.8	14.6	14.1	1.3

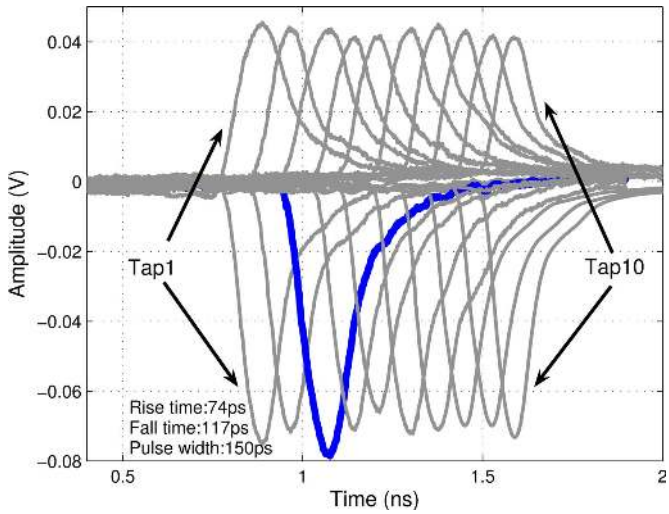

Fig. 21. Impulses generated by each tap of the dual-polarity DWG, with Tap 3 highlighted and annotated.

Fig. 19 shows synthesized sinusoidal waveforms and UWB waveforms with their corresponding spectra. Note that the pulse rate is 1 GHz in all cases and the spectra are for the pulse train, which explain the periodic peaks. The first sinusoidal waveform has a fundamental frequency of 930 MHz, and the SFDR is 30 dBc. The second sinusoidal waveform has a center frequency at 4.5 GHz, close to the Nyquist rate. The UWB pulses include a monocycle, a doublet and a 5th-order Gaussian derivative, with the center frequency from 2.5 to 3.5 GHz. Since the prototype is designed with single-polarity pulses, these pulses are actually generated with DC offset, which is not shown in Fig. 19 because of the AC coupling in the test setup (Fig. 16). This also causes some asymmetry in the waveform and distortion in the spectrum.

Fig. 20 shows the OOK modulation of the prototype DWG driven by a 32-bit, 16 Mbps pseudo random bit stream (PRBS) generated by the AWG. Each output pulse has a Gaussian shape. This demonstrates that OOK modulation can be easily achieved if the DWG is driven by the return-to-zero coded baseband data. The DWG's power consumption is proportional to the pulse rate, which is about 25 mW at 500 MHz and 50 mW at 1 GHz. Therefore, the energy efficiency of the single-polarity DWG prototype is 50 pJ/pulse.

TABLE III
IMPULSES GENERATED BY THE DUAL-POLARITY DWG

	Min. (ps)	Max. (ps)	Mean (ps)	σ (ps)
Tap Delay	90	98	94	3.1
Rise Time	66 (-)	75 (-)	70 (-)	3.2 (-)
	71 (+)	82 (+)	76 (+)	4.1 (+)
Fall Time	106 (-)	117 (-)	112 (-)	3.5 (-)
	121 (+)	135 (+)	127 (+)	5.2 (+)
Min. Pulse Width	112 (-)	125 (-)	120 (-)	4.6 (-)
	126 (+)	144 (+)	132 (+)	6.2 (+)
RMS Jitter	2.4	2.6	2.48	0.26
P-P Jitter	14.2	15.8	14.7	1.6

B. Dual-Polarity DWG Based IR-UWB Transmitter

Similar to the single-polarity DWG, the dual-polarity DWG prototype is first characterized in the time domain. The impulses generated by all taps at 200 MHz pulse rate (sinusoidal trigger) are shown in Fig. 21 and summarized in Table III[5]. Thanks to the optimized design, this DWG prototype achieves shorter tap delay, faster rise/fall time and narrower impulse width than the single-polarity one. The uniformity of the tap delay also improves to only 3.1 ps standard deviation. Note that the performance of negative impulses is better than positive impulses because NMOS transistors are used in the SCSs for negative impulses while PMOS for positive impulses. The measured RMS jitter of all impulses is 2.4 ps to 2.6 ps, and the peak-to-peak jitter is 14.2 ps to 15.8 ps. The input trigger signal has a measured RMS jitter of 1.6 ps. Both include the jitter from the oscilloscope trigger circuitry. Hence the average jitter generation in the prototype transmitter is only about 1.7 ps, which is negligible for IR-UWB applications.

Fig. 22 shows three representative UWB waveforms generated by the dual-polarity DWG, and their frequency spectra. The first UWB waveform (Fig. 22(a)) is a monocycle with a duration of 0.5 ns, generated by tap 3,4. The corresponding spectrum has a -10 dB bandwidth of 6 GHz. The second UWB waveform (Fig. 22(b)) is a doublet with a duration of 0.6 ns, generated by tap 1,2 and 3. The corresponding spectrum has a center frequency of 3 GHz and a -10 dB bandwidth of 5 GHz. Better frequency resolution can be achieved using more taps. For example, Fig. 22(c) shows a UWB waveform with a pulse duration of 0.8 ns and 70 mV voltage swing, generated by tap 1 to 8. It shows a well matched frequency spectrum with the transmit emission mask. The -10-dB bandwidth of the signal spectrum covers 3 GHz to 9 GHz, with the peak at 6 GHz. At 10 GHz, the power spectrum density only drops by about -14 dB. The large signal bandwidth can provide more signal power and processing gain, so the spectrum efficiency is improved. Dash-dot line curves in the spectrum plots are the spectra calculated using FIR filter transfer functions $H(j\omega)$ and measured impulses $x(t)$.

[5]Note that due to the unexpected large metal resistance, the output transmission line impedance is off from 50 Ω at low frequencies, and hence there is a relatively long tail in the generated impulses. In the fall time calculation, we measure the fall time from 80% to 20%, and then multiply it by 1.33 to get the conventional 90%–10% fall time value.

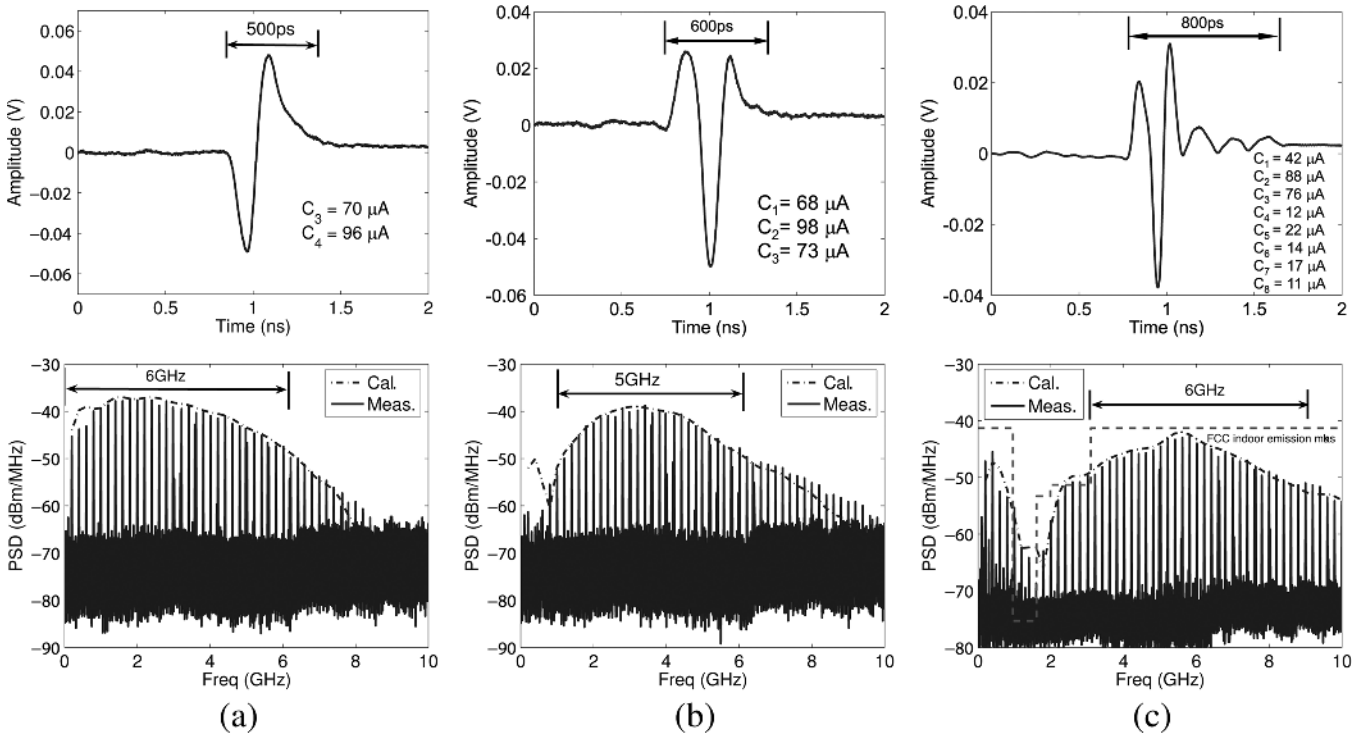

Fig. 22. Measured waveforms and their spectra from the dual-polarity DWG: (a) monocycle, (b) doublet, and (c) a UWB pulse. Note that the spectra are measured from the pulse train using a spectrum analyzer (Fig. 16).

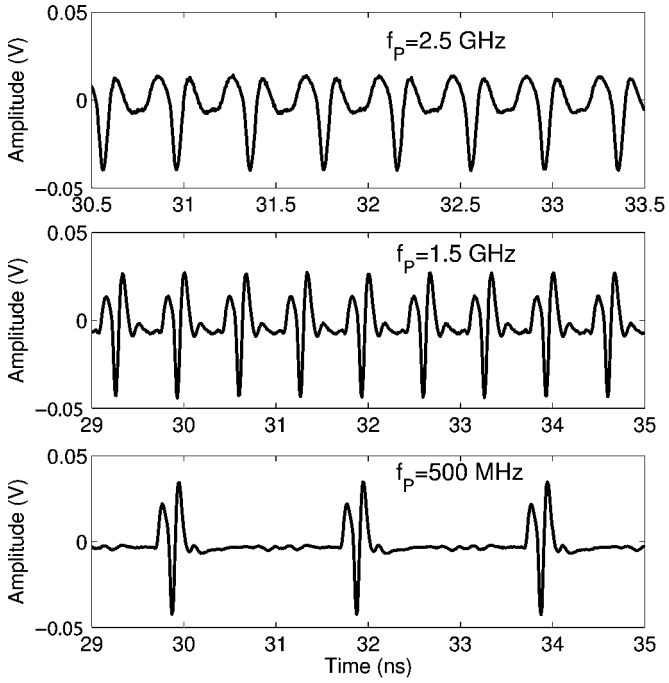

Fig. 23. Measured generated pulse waveforms at 2.5 GHz, 1.5 GHz and 500 MHz pulse rate.

They match well with measured spectra which measures the pulse train and covers the whole pulse cycle 5 ns. Note that in the time-domain measurement, the waveforms have a length of 2 ns, which is shorter than the 5 ns pulse cycle. This effectively introduces a windowing function to the pulse waveform. This windowing effect has been removed in the calculated spectra. These generated waveforms with different spectra demonstrate the reconfigurability of DWG based transmitter.

To demonstrate the transmission at variable pulse rate up to GHz, the transmitter prototype is tested at pulse rate higher than the nominal design value (500 MHz, 1.5 GHz and 2.5 GHz). Generated UWB pulse waveforms are shown in Fig. 23. Pulse shape is well maintained for up to 1.5 GHz pulse rate. In the 2.5 GHz case, since the period is only 400 ps, generated pulses are little distorted compared to lower pulse rate cases.

Both OOK and PPM modulations are tested for the transmitter prototype. Fig. 24(a) shows the OOK modulation of the transmitter driven by a 32-bit, 32 Mbps PRBS. Fig. 24(b) shows the generated UWB pulses modulated with binary PPM. The δt_{PPM} is tunable from 200 ps to 400 ps (400 ps in Fig. 24(b)). In this test, the DWG is driven by 200 MHz clock signal and modulated by 40 MHz square wave. Output UWB sequences without and with PPM modulation are both shown to demonstrate position shift when the modulation signal is applied. The power consumption of the transmitter is proportional to the pulse rate and the energy efficiency is about 45 pJ/pulse.

Table IV summarizes the performance of both DWG prototypes, which demonstrate important features including low power consumption, large signal bandwidth, variable data rate and modulation capabilities.

VI. Conclusion

In this paper, we have presented *distributed waveform generator* (DWG), a new time-interleaving circuit technique for UWB pulse generation, shaping and modulation, based on the analysis of UWB pulse characteristics. Peak sampling scheme is

TABLE IV
PERFORMANCE SUMMARY

DWG Prototypes	Single-polarity	Dual-polarity
Time Resolution	104 ps-150 ps	94 ps-190 ps
Transmitted Power	-9dBm	-7dBm
Pulse Width	0.8 ns	0.8 ns
Pulse Bandwidth (-10 dB)	5GHz (0.5-5 GHz)	6GHz (3-9 GHz)
Power Consumption	50 pJ/pulse	45 pJ/pulse
Data Rate	up to 1.1 Gbps (variable)	up to 2.5 Gbps (variable)
Modulation	OOK	OOK, PPM
Technology	0.18μm Digital CMOS	0.18μm Digital CMOS
Supply	1.8V	1.8V

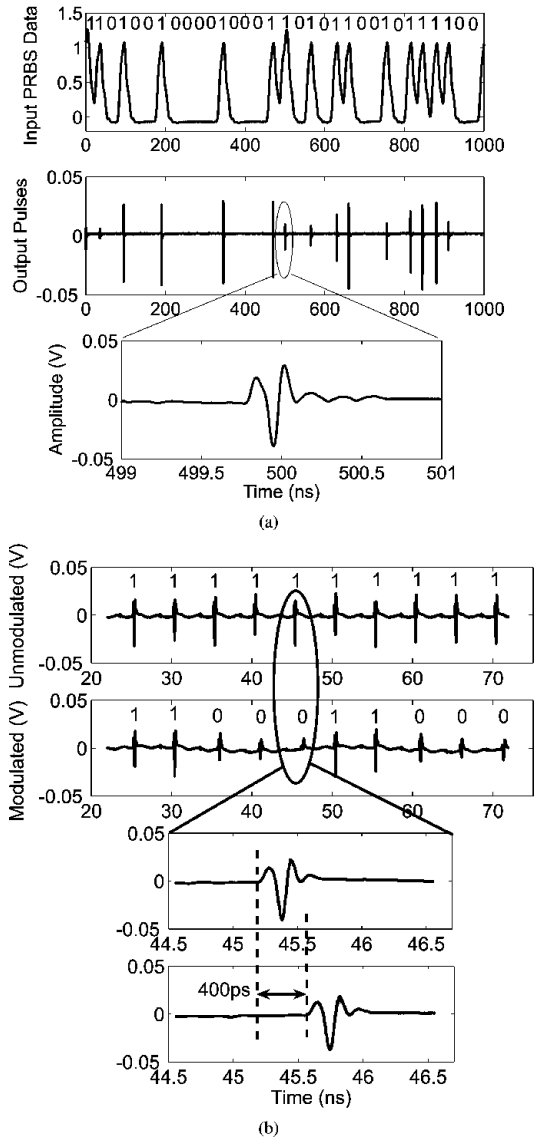

Fig. 24. (a) OOK modulation using 32 Mbps PRBS data; (b) measured PPM output waveforms modulated at 40 MHz, driven at 200 MHz pulse rate. The fluctuation on the waveform amplitude is caused by the limited number of sampling points (4096) in the measurement window.

proposed to reduce the high sampling rate. Thanks to the short duration of UWB pulses, the generation and distribution of high speed input digital data stream are no longer needed in a DWG, which simplify the system architecture and reduce the power consumption significantly. An on-chip transmission line is used at the output node to combine all the generated impulses to form the UWB pulse. Such a distributed circuit technique solves the settling time issue in the time-interleaved DAC, and helps the DWG to achieve large bandwidth. Two DWG prototypes have been developed as demonstrations. A 10-tap, 10 GSample/s, single-polarity was designed and implemented in a 0.18 μm standard digital CMOS technology. Measurement results demonstrated its capability of generating various pulse shapes with 100 ps resolution and OOK modulation. Based on a dual-polarity DWG with optimized design, an IR-UWB transmitter prototype is also demonstrated for UWB pulse generation up to 2.5 Gbps pulse rate. Digital modulation schemes such as OOK and binary PPM are implemented in the transmitter prototype, and demonstrated using 32 Mbps PRBS data. The transmitter consumes 45 pJ/pulse, independent of the data rate.

The DWG prototypes are compared with GSample/s DACs reported recently in Table V. In this comparison, two figure of merits (FOM) for energy efficiency are calculated for each circuit (both the smaller the better). FOM1 emphasizes more on the dynamic range (number of bits) than FOM2. Implemented in a low cost CMOS technology, the DWG achieves comparable performance in terms of sampling rate, and dynamic range while consuming less power. Note that the dynamic range of DWGs is limited by the analog amplitude tuning in the SCS, and can be further improved by using the DAC assisted approach [32]. Also note that in these FOMs, there is a factor missing, i.e., the output power, which is not typically required for DACs, but important for the UWB transmitter applications.

We also compared the DWG based IR-UWB transmitter with other IR-UWB transmitter reported recently in Table VI. Among them, the DWG-based transmitter achieves the largest bandwidth, the highest data rate, the highest transmitted power and one of the best energy efficiency.

ACKNOWLEDGMENT

The authors thank B. Chatterjee, A. Bahai, P. Holloway, M. Bohsali, J. Yu, A. Shah, V. Abellera, P. Misich, and J. Wan of National Semiconductor for their support in chip fabrication.

TABLE V
PERFORMANCE COMPARISON WITH OTHER REPORTED HIGH-SPEED DACS

Ref.	Power Dissipation P_D (mW)	Number of Bit N	F_s (GS/s)	FOM1 (pJ/S)	FOM2 (pJ/S)	Technology
[33]	12	5	10	0.0375	0.24	$0.18\mu m$ SiGe
[19]	360	6	20	0.28	3	$0.18\mu m$ SiGe
[34]	29	6	3	0.151	1.61	$0.13\mu m$ CMOS
[35]	190	8	12	0.0618	1.98	$0.09\mu m$ CMOS
[36]	1014	6	22	0.72	7.68	$0.13\mu m$ SiGe
[37]	455	4	30	0.92	3.75	$0.25\mu m$ SiGe
[38]	150	4	10	0.94	3.75	$0.13\mu m$ CMOS
[39]	660	3	40	2.75	5.5	$0.12\mu m$ SiGe
Single-Polarity DWG	50	3	10	0.625	1.66	$0.18\mu m$ CMOS
Dual-Polarity DWG	45	3	10	0.563	1.5	$0.18\mu m$ CMOS

$$FOM1 = \frac{P_D}{2^N \cdot F_s}; \quad FOM2 = \frac{P_D}{N \cdot F_s}$$

TABLE VI
PERFORMANCE COMPARISON WITH OTHER IR-UWB TRANSMITTERS.

Ref.	Pulse Bandwidth -10dB (GHz)	Transmit Power (dBm)	Energy Efficiency (pJ/pulse)	Pulse Rate	Modulation	Technology
[10]	2	-9	210	500 MHz	BPSK	$0.18\mu m$ CMOS
[13]	2	-9	190	100-400 MHz	PPM	$0.18\mu m$ CMOS
[23]	2	N/A	47	up to 50 MHz	PPM	$90nm$ CMOS
[14]	2	N/A	62.5	160 MHz	PPM, BPSK	$0.13\mu m$ CMOS
[21]	3	N/A	41	750 MHz	BPSK	$0.18\mu m$ CMOS
This work	6	-7	45	up to 2.5 GHz	OOK, PPM	$0.18\mu m$ CMOS

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