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Distribution of Interface States in MOS Systems Extracted by the Subthreshold Current in MOSFETs under Optical Illumination

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In this paper, we propose a novel subthreshold current method using the optical current-voltage (I-V) curve for interface-state extraction. The new method is simpler and more accurate than the conventional interface-state extraction methods in MOSFETs. Based on the photonic high-frequency capacitance-voltage response of MOS capacitors and the conventional subthreshold current method, an improved characterization method is reported for the analysis of interface-states in MOS systems. An optical source with a photonic energy $E_{ph} = 0.943$ eV (wavelength = 1314.5 nm) is employed for optical subthreshold current characterization of interface-states distributed in the photo-responsive energy-band. By using the optical subthreshold current and dark subthreshold current, we obtained a U-shaped distribution for the interface-trap density (D_{it}) in N-type and P-type MOSFETs.

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I. INTRODUCTION

It is well known that the interface traps at the Si/SiO_2 interface in MOS (metal-oxide- semiconductor) structures play an important role in determining the threshold voltage (V_T), the channel carrier mobility (μ), and the transconductance (g_m) of MOSFETs (metal-oxide-semiconductor field effect transistors). Therefore, accurate modeling and characterization of interface traps throughout the band-gap is one of the most important topics for improving the robustness of devices and their integrated circuits with MOS capacitors and MOSFETs. Enormous effort has been expended for accurate characterization of interface traps in MOSFETs. However, most of the previously used methods required a complicated measurement procedure or mechanism [1–3].

In very large-scale integrated (VLSI) circuits, MOS device dimensions are largely scaled down in order to improve speed and performance. Due to such aggressive scaling, the thickness of the gate dielectric has been reduced below 4 nm down to 2 nm. These gate dielectrics are subject to very high electric fields during circuit operation. Therefore, ultra-thin gate dielectrics need to have very high dielectric strengths and excellent interface properties [4]. Also, scaling of MOSFETs in VLSI circuits requires a steady increase in channel doping levels and improvements in the oxide reliability. Channel doping in the high 10^{17} cm^{-3} range is already usual, and dopant densities above 10^{18} cm^{-3} are being investigated [5].

For development of MOS ultra-large-scale integration (ULSI) technology to improve the performances of high-speed digital and mixed analog-digital signal processing circuits and low-voltage operation, circuit designers require accurate MOSFET model parameters for use in circuit simulators [6]. Therefore, the interface-trap is one of the most important parameters for the reliability and for the modeling of MOS devices. Traditionally, this parameter has been evaluated from MOS capacitors by using a capacitance-voltage (C-V) measurement or conductance technique or deep-level transient spectroscopy (DLTS) [7,8]. These techniques are not suitable to estimate interface traps in the small gate areas of scaled MOSFETs, owing to the fact that they need a larger MOS capacitor area so as to ensure a high D_{it} measurement resolution. On the other hand, it has been reported that a mean D_{it} can be estimated from the subthreshold characteristics in good quantitative agreement with the other techniques mentioned above and the charge pumping (CP) technique [9]. The simple direct-current measurement procedure of the subthreshold characteristics makes the technique of subthreshold analysis attractive.

In this paper, a new subthreshold analysis technique, namely, the optical subthreshold current method (OSCM), is presented for the extraction of MOSFET interface traps. Based on the photonic high-frequency

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capacitance-voltage (C-V) response of MOS capacitors and the conventional subthreshold current method, the result for the subthreshold gate voltage shows extreme peak characteristics with respect to the drain current in the subthreshold region. In this way, the difference in the gate voltage in the subthreshold region directly demonstrates the magnitude of the interface traps. We propose a novel and accurate interface-trap extraction method using the optical current-voltage (I-V) curve and the optical subthreshold current model as a means to achieve the accurate results for the small gate areas of scaled MOSFETs. The basic principle of this method is introduced, and its validity is verified by the extraction experiments on n-channel and p-channel MOSFET devices.

II. ILLUMINATION CHARACTERISTICS AT INTERFACE-STATES IN MOS SYSTEMS

In this section, we will describe the characteristics of interface-states and optical capacitance-voltage curve for deep depletion in the MOS structure with illumination.

1. Characteristics of Interface-states

Some impurities or defects can be inadvertently incorporated into the oxide during oxide growth or subsequent processing steps. This results in the oxide being contaminated with various types of charges and traps. Four different types of charges have been identified in thermally grown oxides on a silicon surfaces. These charges are shown schematically in Fig. 1. They are interface-trapped charges Q_{it}, fixed-oxide charges Q_f, oxide-trapped charges Q_{ot}, and mobile ionic charges Q_m. All of these charges are very dependent on the device fabrication process [10–15].

Figure 2 shows the energy-band diagram of a semiconductor at the oxide-semiconductor interface. The periodic nature of the semiconductor is abruptly terminated at the interface so that allowed electronic energy levels will exist within the forbidden band-gap. These allowed energy states are referred to as interface-states. Charge can flow between the semiconductor and interface-states, in contrast to the fixed-oxide charge. The net charge in these interface-states is a function of the position of the Fermi level in the band-gap. In general, acceptor states exist in the upper half of the band-gap, and donor states exist in the lower half of the band-gap. An acceptor state is neutral if the Fermi level is below the state and becomes negatively charged if the Fermi level is above the state. A donor state is neutral if the Fermi level is above the state and becomes positively charged if the Fermi level is below the state. The charge of the interface-states is then a function of the gate voltage applied across the MOS capacitor.

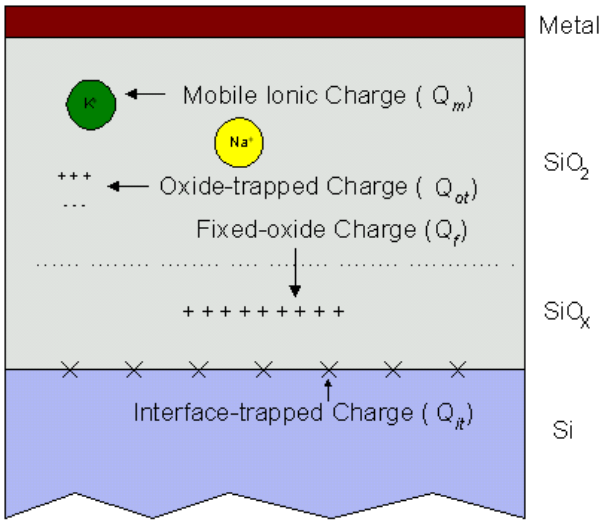

Fig. 1. Distribution of charges inside the gate SiO_2.

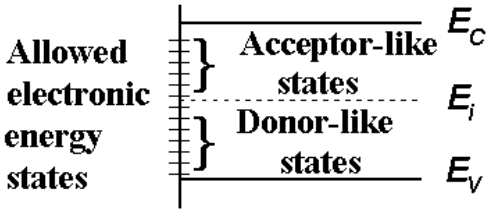

Fig. 2. Schematic diagram showing interface-states at the oxide-semiconductor interface.

Figure 3(a) shows the energy-band diagram in a p-type semiconductor of a MOS capacitor biased in the accumulation condition. In this case, there is a net positive charge trapped in the donor states. Now, let the gate voltage change to produce the energy-band diagram shown in Fig. 3(b). The Fermi level corresponds to the intrinsic Fermi level at the surface; thus, all interface-states are neutral. This particular bias condition is known as midgap. Figure 3(c) shows the condition at inversion in which there is now a net negative charge in the acceptor states [15,16].

2. Photonic High-frequency C-V Characteristics of MOS Capacitors in Deep Depletion

Photonic high-frequency capacitance-voltage (H-F C-V) characteristics of MOS capacitors with $t_{ox} = 23$ nm and $W \times L = 300 \times 300\ \mu m^2$ were measured with a small-signal frequency, $f = 500$ kHz, at a slow DC sweep rate = 1 mV/s [1,2]. Due to the limited contribution of photo-generated excess channel carriers only from the interface-states at the Si/SiO_2 interface under illumination at $\lambda =$ 1314.5 nm, the gate capacitance in the inversion mode ($|V_G| > |V_T|$) increases little and shows negligible variation with increasing optical power (P_{opt}). However, due

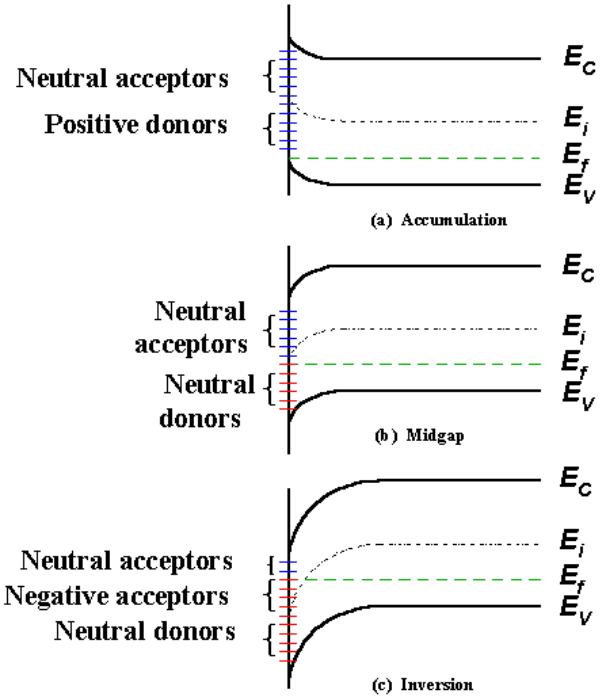

Fig. 3. Energy-band diagram in a p-type semiconductor showing the charge trapped in the interface-states when the MOS capacitor is biased (a) in accumulation, (b) at midgap, and (c) at inversion.

to the abundant contribution of photo-generated excess carriers from the valence band to the conduction band under illumination at $\lambda = 850$ nm, the gate capacitance in the inversion region significantly increases, but its variation is also negligible with increasing P_{opt}. Therefore, slow-sweep-rate H-F C-V characteristics of MOS capacitors under optical illumination are not suitable for the characterization when either $E_{ph} > E_g$ or $E_{ph} < E_g$ [1, 2]. Photonic deep-depletion (DD) H-F C-V curves for an optical input with $\lambda = 1314.5$ nm are shown in Fig. 4, and a schematic energy-band diagram is shown in Fig. 5 for N- and P-MOS capacitors.

III. OPTICAL SUBTHRESHOLD CURRENT METHOD (OSCM)

In this section, we will describe the main idea by comparing the dark subthreshold (conventional method) with the optical subthreshold method.

1. Conventional MOSFET Subthreshold Current Method

The drain current of MOSFETs operated at gate voltages below threshold (subthreshold) can be written as

$$I_D = I_{Th} \exp\left(\frac{V_{GS} - V_{TN}}{\eta V_{th}}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right), \quad (1)$$

where I_{Th} is a constant that depends on temperature, device dimensions, and substrate doping density; η, given by $\eta = 1+(C_D+C_{it})/C_{ox}$, accounts for the charge placed on the gate that does not result in an inversion layer charge. Some gate charge is imaged as space-charge-region charge, and some as interface-trap charge. Ideally, $\eta = 1$, but $\eta > 1$ as the doping density increases ($C_D \sim N_A^{1/2}$), and the interface-trap density increases ($C_{it} \sim D_{it}$) [10,11,13,14].

The usual subthreshold plot is one of $\log(I_D)$ versus V_G for $V_D \gg V_{th}$. The measurement is simple to do, requiring merely a current-voltage measurement of a MOSFET. Such a plot has a slope of $q/[\ln(10)\eta \mathrm{kT}]$. The slope is usually expressed as the subthreshold swing (S), which is the gate voltage necessary to change the drain current by one decade and is given by

$$S = \frac{\ln(10)\eta kT}{q} \approx 60\eta(T/300) \ \ \mathrm{mV/decade}. \quad (2)$$

The interface-trap density, obtained from a plot of $\log(I_D)$ versus V_G, is

$$D_{it} = \frac{1}{q}\left(\frac{qS}{2.3kT} - 1\right)C_{ox} - \frac{C_D}{q}, \quad (3)$$

requiring accurate knowledge of C_{ox} and C_D. An additional complication is the dependence of the slope on surface potential fluctuations. This is the reason that this method is usually used as a comparative technique in which the subthreshold slope of a device is measured, the device is degraded, *e.g.*, by hot-electron stressing or energetic radiation, and then the subthreshold slope is measured again. The change in the slope is easier to interpret than the slope itself [10,11,13,14].

A subthreshold MOSFET curve is shown in Fig. 6. The threshold voltage V_T is determined by using various techniques. When such a device is stressed, typically the slope decreases, the subthreshold swing increases, and the curve shifts due to oxide-trapped charge and interface traps. For the SiO_2-Si interface, interface traps in the upper half of the band-gap are acceptors, and those in the lower half are donors with the demarcation between the two occurring at about half the band-gap [8,10,12, 13].

2. Optical MOSFET Subthreshold Current Characteristics

As mentioned above, subthreshold operation without illumination can be described by Eq. (1). In this section,

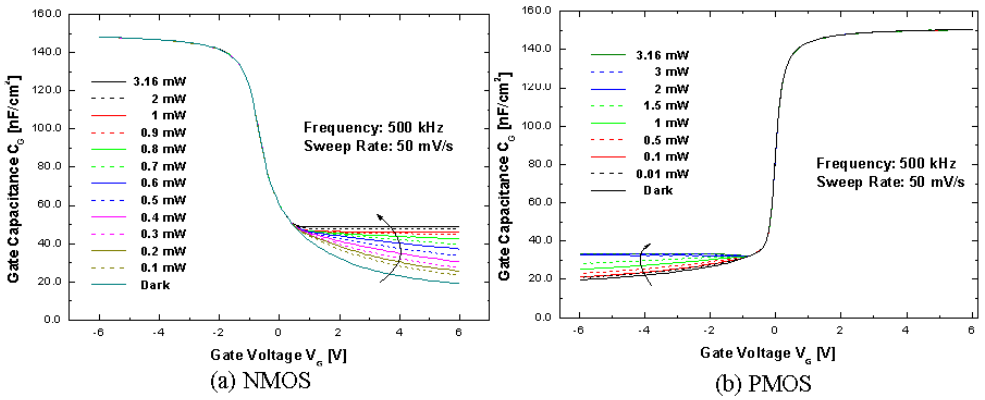

Fig. 4. Photonic DD HF-CV characteristics with $\lambda = 1314.5$ nm.

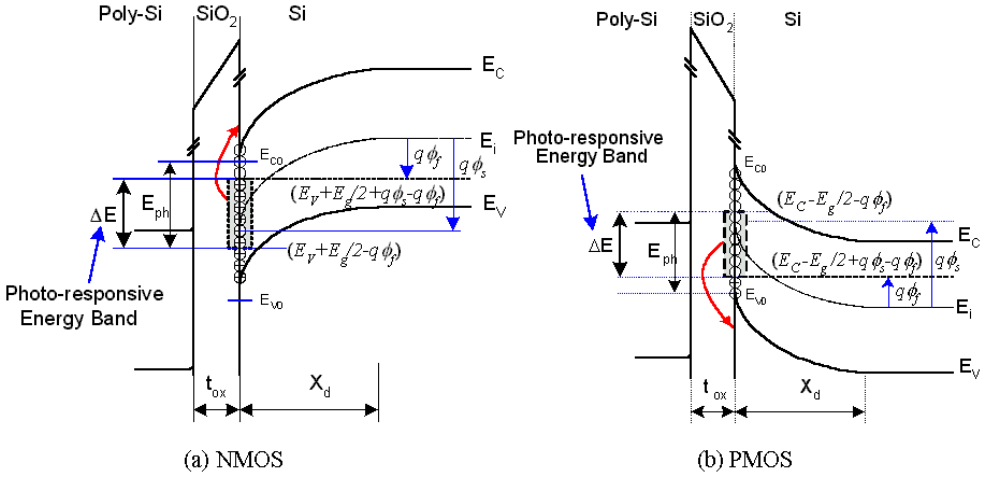

Fig. 5. Energy-band diagram of MOS capacitors under optical illumination.

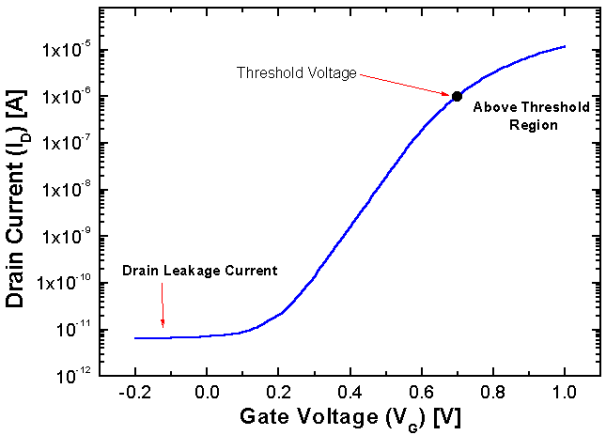

Fig. 6. MOSFET subthreshold current characteristics.

Eq. (1) will be modified as Eq. (4), and illumination is expressed as Eqs. (6) ∼ (8).

$$I_{D,Dark} \cong I_{Do} \exp\left(\frac{V_{GS} - V_{TNo}}{\eta_{Dark} V_{th}}\right) \quad for \quad V_{DS} > 3V_{th} \sim 0.08V, \tag{4}$$

where

$$\eta_{Dark} = 1 + \frac{C_d}{C_{ox}} + \frac{C_{it,Dark}}{C_{ox}},$$

$$I_{Do} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right)\left(\frac{C_d}{C_{ox}}\right) V_{th}^2 = \mu_{eff} C_d \left(\frac{W}{L}\right) V_{th}^2, \tag{5}$$

and the subthreshold operation with illumination can be expressed as

$$I_{D,Photo} \cong I_{Do} \exp\left(\frac{V_{GS} - V_{TN,Photo}}{\eta_{Photo} V_{th}}\right) \quad for \quad V_{DS} > 3V_{th} \sim 0.08V, \tag{6}$$

$$\eta_{Photo} = 1 + \frac{C_d}{C_{ox}} + \frac{C_{it,Dark}}{C_{ox}} + \frac{C_{it,Photo}}{C_{ox}} = \eta_0 + \frac{C_{it,Dark}}{C_{ox}} + \frac{C_{it,Photo}}{C_{ox}}, \tag{7}$$

$$\eta_0 = 1 + \frac{C_d}{C_{ox}}, \quad V_{TN,photo} = V_{TNo} - \Delta V_{TN}, \tag{8}$$

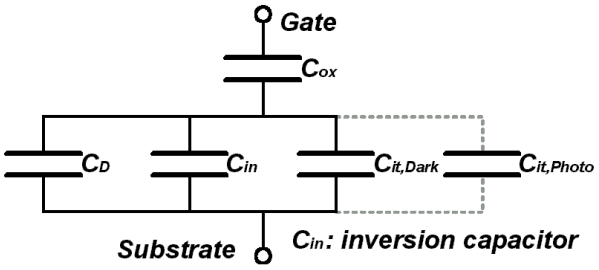

Fig. 7. Equivalent circuit for illumination (dash line) and no illumination (solid line).

$I_{D,Photo}$ is the subthreshold current with illumination, and η_{Photo} adds $C_{it,Dark}$ to $C_{it,Photo}$ which is generated by the interface traps. The ideality factors can be obtained

$$\frac{1}{\eta_{Dark}} \cong \left(\frac{V_{th}}{V_{GS}-V_{TNo}}\right) \ln\left(\frac{I_{D,Dark}}{I_{Do}}\right) \quad (9)$$

under the dark condition and

$$\frac{1}{\eta_{Photo}} \cong \left(\frac{V_{th}}{V_{GS}-V_{TN,photo}}\right) \ln\left(\frac{I_{D,Photo}}{I_{Do}}\right) \quad (10)$$

under optical illumination. Consequently, C_{it} can be obtained from the difference between the ideality factors as

$$C_{it,Photo} = (\eta_{Photo} - \eta_{Dark}) C_{ox}, \quad (11)$$

and the interface-trap density (D_{it}) can be finally obtained from

$$D_{it} = \frac{\Delta C_{it,Photo}}{q} = \frac{C_{ox}(\Delta\eta_{Photo} - \Delta\eta_{Dark})}{q}. \quad (12)$$

An equivalent circuit model with optically generated interface capacitances under illumination is shown in Fig. 7. We note that C_d, C_{in}, and $C_{it.Dark}$ depend on the gate voltage (V_{GS}) or the surface potential (ϕ_{ss}). However, $C_{it,Photo}$ only depends on the photo-generated carriers in the optically responsive energy-band, which is modulated by the gate voltage (V_{GS}). As mentioned above, this method does not require accurate knowledge of the subthreshold slope or many device geometry parameters.

IV. EXPERIMENTAL RESULTS

The optoelectronic current-voltage characteristics of poly-Si gate MOSFETs with $W \times L = 30 \times 1.2\ \mu\text{m}^2$ were measured with an optical source (ILX Lightwave Co., Model 7200, $\lambda = 1314.5$ nm), a cascade probe station, and an HP4145B semiconductor parameter analyzer, as shown below Fig. 8. We probed current-voltage characteristics of MOSFETs both under a dark condition and under illumination.

In addition, the threshold voltage was measured by using the transconductance peak method, and measured

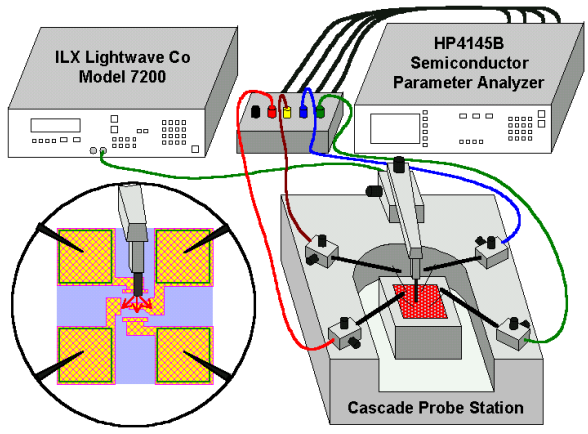

Fig. 8. Experimental setup.

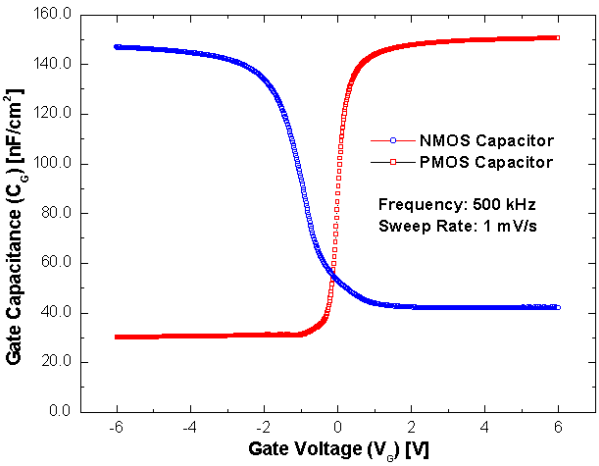

Fig. 9. Measured capacitance-voltage (C-V) curves.

C_{ox} was 150 nF/cm^2, as shown below Fig. 9. Combining the subthreshold currents and the gate capacitances measured under dark and optical inputs (Fig. 10 for N- and P-MOS systems) [1, 2], we obtained the interface-trap density (D_{it}) for an MOS system. For V_{DS} larger than 3 V_{th} (~80 mV), the V_{DS}-dependent term may be neglected in the I-V characteristics [8, 10, 13]. The extracted interface-trap density (D_{it}) is shown in Fig. 11 and shows a typical U-shaped distribution in the energy-band between E_V and E_C.

V. CONCLUSION

A new subthreshold analysis technique, namely, the optical subthreshold current method (OSCM), has been presented for extracting the interface traps in MOSFET devices. The interface-trap density can be readily determined from the given formulation by observing the optical subthreshold current in the subthreshold region. The method does not require accurate knowledge of the

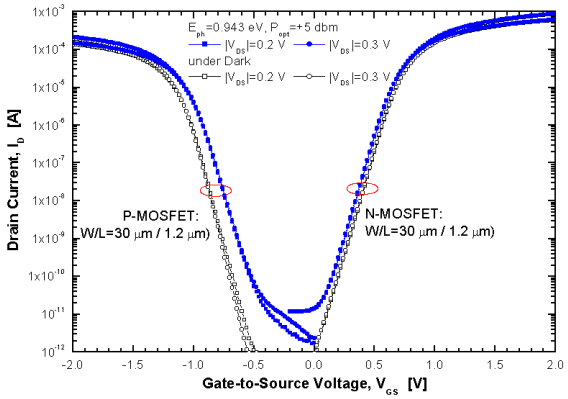

Fig. 10. Subthreshold I_D-V_{GS} characteristics of an N- & P-channel MOSFETs under dark and sub-band gap photonic excitation.

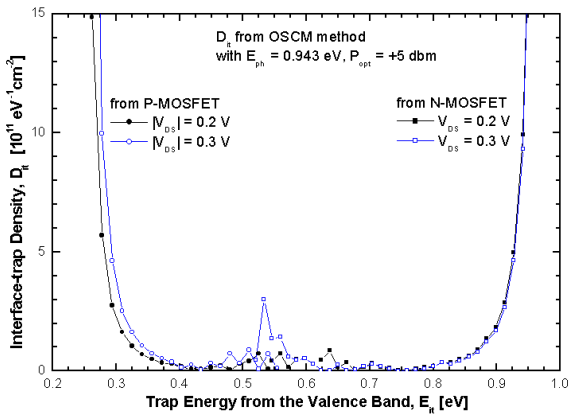

Fig. 11. Extracted interface-trap densities.

subthreshold slope and of many device geometry parameters. The validity of the technique has been verified by using the measured parameter, the optical current-voltage characteristics, and the U-shaped distribution of the interface-trap density (D_{it}) for n-channel and p-channel MOSFET devices. In applications, this method is expected to have many advantages because it is an accurate and simple method.

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