

DNL ADC Testing by the Exponential Shaped Voltage

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Abstract—Testing of ADC differential nonlinearity by the histogram method requires a signal generator with extremely low distortion and high stability. In this paper, the new type of stimulus signal is proposed, which simplifies the task. The testing signal has an exponential form and can be generated simply by discharging the capacitor across the resistance. The resulting digital samples from the output of the tested ADC allow estimation of the best fitted exponential signal by the proper three-parameter method. The histograms from the data record and from the best fitted exponential approximation allow calculation of the differential nonlinearity.

Index Terms—ADC testing, exponential stimulus, histogram method.

I. INTRODUCTION

THE deviation of actual ADC transfer characteristic from the ideal one is described by differential nonlinearity (DNL) and integral nonlinearity (INL). These parameters can be tested by standardized methods [1], which are generally categorized into two groups—static and dynamic methods. The static method requires the high-accuracy dc calibrator and voltmeter. Moreover, the test process consumes a lot of time.

The second method, based on the dynamic histogram analysis, is faster, and for that reason, it is applied more frequently. The dynamic histogram enables assessment of the acquired sample distribution for a known stimulus signal (most often sinewave), carrying information about the actual $DNL[k]$ of the ADC. However, the high accuracy of the required stimulus signal generator analogous to the dc calibrator, is the bottleneck of this standardized method of ADC DNL dynamic testing. Just the harmonic stimulus signal with extremely stable amplitude and frequency, usually in addition filtered by the high-quality pitch-off analog filter, achieves the accuracy limits, necessary for common-resolution (10–14 bit) ADC testing. Because of common testing generator quality limits, insufficient for the common ADC test, the end users have problems to assess the ADC parameters correctly. Moreover, the robustness of testing generators excludes them from implementation as an embedded block on the ADC chip for the automatic diagnostic process.

The histogram method has a known drawback. The various origins, interfering input voltage and the additive thermal noise to the testing signal tend to equalize the code bin width $W[k]$ in the ADC under test and hide $DNL[k]$ errors in the histogram shape. For these reasons, the testing stand, besides high accu-

racy of the stimulus signal shape, requires high reduction of the electromagnetic interference generated on the ground wires. The calibrating generator should be powered independently from other instruments and connected star-like at the ground terminal of the ADC input.

The new testing method based on the histogram is described in this paper. The novelty of the developed test method is in replacing the standard sinusoidal test signal by an exponential waveform, generated by the discharging of a capacitor across the ADC input resistance. The advantages of such a signal are

- simple generation of the very precise shape, close to ideal one;
- simple accurate generator circuitry in comparison with standard electronic harmonic signal generator;
- easy circuit implementation convenient for implementation on ADC chip;
- star-like connection of discharging capacitor avoids additional interference links across the ground wires and power supply circuit.

The acquired digital samples from the output of the ADC under test allow estimation of the best fitted input exponential waveform. The code occurrence for the real code bin width in comparison with the ideal one from the estimation for the fitting allows determining the $DNL[k]$ for any code level k .

II. GENERATION OF STIMULUS VOLTAGE

The stimulus signal generator with galvanic separation from the control unit is shown in Fig. 1. The independent supply voltage V_{ST} is connected to the parallel RC circuit by an electronic switch. The voltage memorized on capacitor C is discharged across the resistance R connected in parallel to the ADC input resistance R_{IN} and resistance R_C that represents the ohmic losses in the real capacitor. All the mentioned resistances result in the total discharging resistance R_{tot} . The ADC input bias current generates an offset voltage V_{off} on the R_{tot} . Its value represents the final steady voltage level given by the stimulus voltage [Fig. 1(b)]. In the case that the V_{ST} value is above the ADC input range, the initial part of the ADC data record, corrupted by the switch-induced glitches, can be removed. The wideband noise superimposed on the stimulus signal is self-suppressed by filtering effects of the capacitor. The shape of the discharging calibration voltage for the capacitor model according to Fig. 1 is

$$V_{IN} = V_{off} + (V_{ST} - V_{off}) e^{(-t/R_{tot}C)} \quad (1)$$

where V_{ST} is starting voltage, V_{off} is offset, C is discharged capacitance, and R_{tot} is total discharging resistance. The dif-

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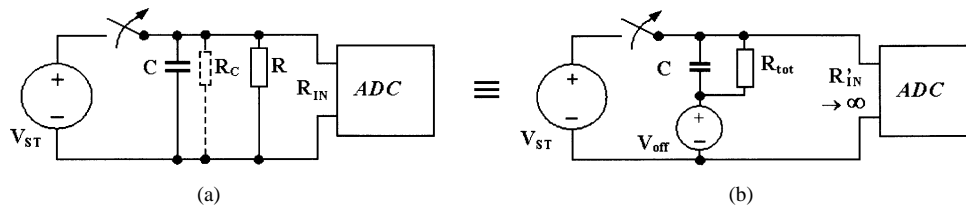


Fig. 1. (a) Circuit generating exponential stimulus signal. (b) Equivalent circuit.

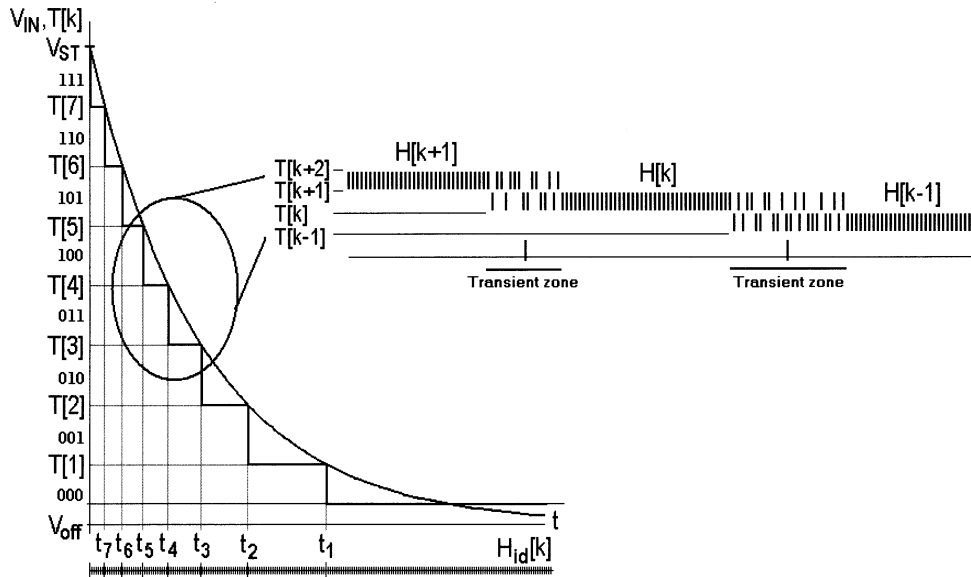


Fig. 2. ADC data record for exponential stimulus signal.

ferential nonlinearity of the tested ADC is estimated from the histogram of the registered samples using the well-known formula [1]

$$DNL[k] = \frac{H[k]}{H_{id}[k]} - 1 \text{ [LSB]} \quad (2)$$

where $H[k]$ represents the actual number of output codes in the record with the value equal to k . $H_{id}[k]$ is the number of occurrences for the ideal exponential shape of the stimulus signal

$$H_{id}[k] = R_{tot} C f_S \ln \left(\frac{(k+1)Q - V_{off}}{kQ - V_{off}} \right) \text{ for } k = (2^N - 2), \dots, 1 \quad (3)$$

where f_S is the sampling frequency. The Q is the ideal code bin width defined in [1]. The exact values of parameters of the real exponential stimulus signal are unknown. Their best estimation can be done by the three-parameter least square fitting procedure from the record (Fig. 2).

The developed fitting algorithm is similar to the known four-parameter estimation of the best-fitted harmonic function [1]. Let us consider the data flux of M samples recorded in the vector form $Y = [y(1), y(2), \dots, y(M)]^T$. The ideal stimulus signal can be approximated by the function:

$$\tilde{y}[m] = B + Ae^{-\alpha m} \text{ for } m = 1, \dots, M \quad (4)$$

where, according to (1)

$$B = \frac{V_{off}}{Q}; \quad A = \frac{V_{ST} - V_{off}}{Q}; \quad \alpha = \frac{1}{R_{tot} C f_S}$$

α is the inverted time constant normalized to the actual value of the sampling frequency. These parameters can be found by minimizing the following function:

$$\frac{1}{M} \sum_{m=1}^M [y[m] - B - Ae^{-\alpha m}]^2 = \varepsilon^2(A, B, \alpha). \quad (5)$$

The value ε^2 represents the quantization noise power.

The approximated shape allows determining the ideal occurrences for the k -th code bin

$$H_{id}[k] = \frac{1}{\alpha} \ln \left(\frac{k+1-B}{k-B} \right) = T_k \cdot f_S, \quad (6)$$

where T_k is the stimulus signal transition time through code bin k . The final value of $DNL[k]$ is given by (2). The accuracy of the resulting $DNL[k]$ depends on the number of samples M and on the offset value B . The relative uncertainty δ of the code bin width determination for code k is

$$\delta = \frac{1}{H_{id}[k]} = \frac{1}{M \frac{T_k}{T_{tot}}} \quad (7)$$

where T_{tot} is the total transition time of the exponential stimulus through the ADC full range. The worst case for the exponential stimulus test represents the ADC highest code $k = 2^N - 1$. Substituting (6) into (7) and consecutively modifying, the required number of samples M in the record for the desired test uncertainty δ as a fraction of the code bin width in the DNL determination is given as follows:

$$M \geq \left\lceil \frac{\ln(-B) - \ln(2^N - 1 - B)}{\delta (\ln(2^N - B) - \ln(2^N - 1 - B))} \right\rceil. \quad (8)$$

TABLE I
DEPENDENCE OF RELATIVE STANDARD DEVIATION OF CODE BIN OCCURRENCE
FREQUENCY ON EXPONENTIAL STIMULUS TIME CONSTANT (SAMPLING
FREQUENCY = 1, $M = 10^5$, 10 BITS ADC RESOLUTION, GAUSSIAN NOISE
WITH STD = 1 LSB) ACQUIRED BY SIMULATION

Inverted time constant α	Code	Relative std of code occurrence frequency
25e-6	1020	0.14
5e-6	1020	0.1
1e-6	1020	0.09
triangular	any	0.09
sinewave	512	>0,11*

* according to the chosen ADC range overdrive

The noise sensitivity of the developed method in comparison with methods based on the sinewave and triangular test signal was studied by the simulation. The relative standard deviation of the code bin occurrence frequency was chosen to be the assessing criterion. The comparison of standard deviation for the worst cases (the lowest code occurrence frequency): the border codes for the exponential stimulus and the middle codes of the full scale for the sinewave, proved the similar noise sensitivity in general (Table I). Choosing the better timed shape of the exponential stimulus with the longer time constant in comparison with the record time, and the convenient value B , the statistics can be improved because of flattening the histogram. The histogram can close to the histogram of the theoretically ideal, triangular stimulus that has uniform code occurrence distribution over the full ADC range. Applying the convenient shape of the exponential stimulus evidently results in decreasing the code occurrence relative standard deviation for the exponential stimulus in comparison with the sinewave for a given record length M (Table I).

The main disadvantage of the exponential stimulus signal—the different occurrence of output samples for each code level k , which causes different statistical uncertainty in the histogram measurement, can be overcome by modification of the proposed method. The ADC full range can be divided into some consecutive subranges tested individually by the stimulus signals with different time constants. Finally, the full-range DNL can be reconstructed by linking the subrange DNLs together. The advantage of such a method is higher accuracy of DNL estimation and the relatively small number of samples M to be acquired.

III. EXPERIMENTAL RESULTS

The proposed method has been experimentally verified for the ADC embedded on the microcontroller chip—ADuC812 by Analog Devices. The test setup is shown in Fig. 3. The capacitor was made up of a bank of capacitors with small dielectric absorption. The reed relay was used as the switch. Experiments were performed for the ADC with and without the input buffering amplifier embedded on the evaluation board.

The ADC input range was divided into a few consecutive subranges, as it is shown in Table II and Fig. 4 with the goal to increase the statistics for the estimation of code bin width (see above). The partial DNLs (Fig. 4) measured in the subranges were finally linked on the sub-range borders with the aim to

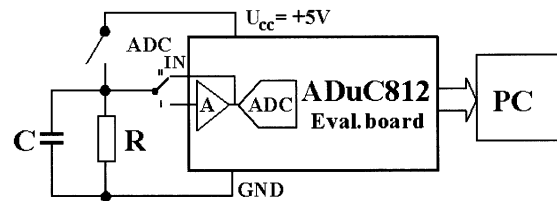


Fig. 3. Setup for exponential wave testing with (pos. 1) and without (pos. 2) buffering amplifier.

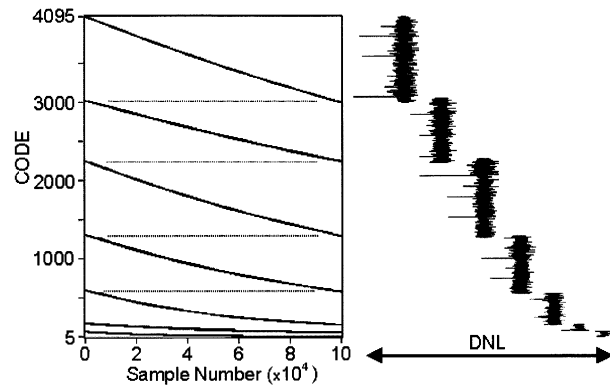


Fig. 4. Generated exponential subparts and measured DNL from the histogram of the data record.

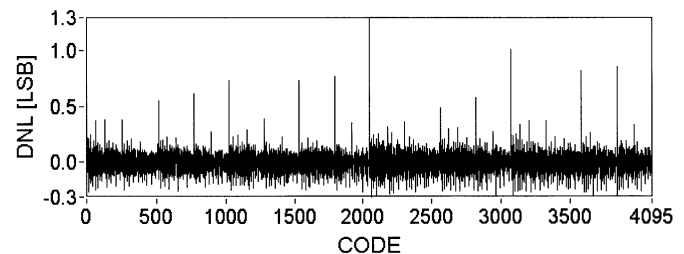


Fig. 5. DNL of ADuC812 by exponential testing without buffering amplifier.

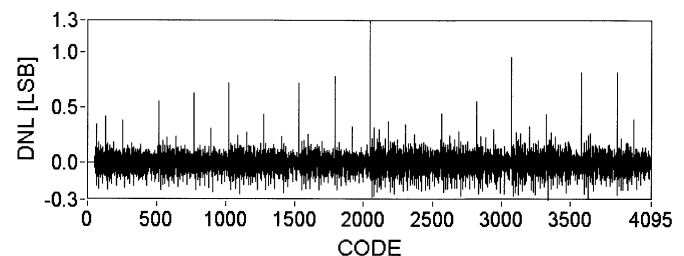


Fig. 6. DNL of ADuC812 by exponential testing with buffering amplifier.

obtain the final $DNL[k]$ for the full input voltage scale. The achieved results (Figs. 5 and 6) were compared with those acquired by the standard histogram method (Fig. 7) with the harmonic stimulus signal [1] generated by the Stanford Research DS360 Calibrator.

IV. CONCLUSION

The authors proposed and verified a new simple histogram method for dynamic testing of ADC differential nonlinearity based on the exponential stimulus signal. The exponential testing signal is easy to generate with the required accuracy using a high-quality capacitor. Moreover, the circuit generating

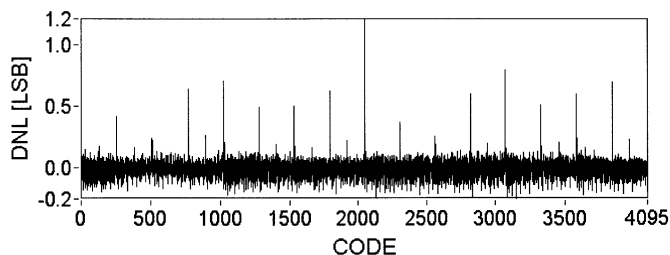


Fig. 7. DNL of ADuC812 measured by the standardized histogram test (sinewave with frequency 3,377 Hz, sampling frequency 27 kHz, and number of samples $2 \cdot 10^6$).

TABLE II
SPLITTING OF THE FULL-SCALE RANGE

Number of samples = 100000, $V_{REF}=2.5V$			
Without amplifier		With amplifier	
$C=9.3\mu F$		$C=6.5\mu F$	
Codes	$R[\Omega]$	Codes	$R[\Omega]$
4094-2994	∞	4091-2997	4M7
3020-2237	∞	3090-2133	3M9
2250-1292	3M9	2200-1268	2M7
1310-577	1M8	1300-601	1M8
600-152	820k	650-158	1M0
172-59	680k	200-51	820k
70-5	390k	—	—

such stimulus signal is ideally decoupled from any interfering sources and control computer. The test signal is approximated from the ADC data record by the best-fitted exponential function. The comparison of experimental results achieved by the proposed testing method and by the standardized histogram method for the harmonic stimulus signal showed a good coherence.

The low quality of the capacitor in the generating circuit can result in additional parasitic exponential components in the stimulus signal. The experiments show acceptable accuracy of this method for the ADC with 12-bit resolution and high-quality capacitors commonly available on the market. The higher testing accuracy requires either a capacitor with

extraordinary high quality or a more complex capacitor model, which results in a complicated fitting procedure of the stimulus signal shape by a multicomponent exponential function.

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