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Dopingless 1T DRAM: Proposal, Design, and Analysis

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ABSTRACT In this paper, we have proposed a dopingless 1T DRAM (DL-DRAM) that utilizes the charge plasma concept. The proposed device employs a misaligned double-gate architecture to store holes and differentiates between the two logic states. The source, drain, backgate, and frontgate workfunctions are optimized to achieve the required concentration profiles in an intrinsic silicon body. Using TCAD simulations, we have analyzed the read/write mechanism in the device. Our study shows that the mechanism of current transport during reading operation depends strongly on the source workfunction. When the source workfunction is less than 4.5 eV the transport mechanism during reading is dominated by drift-diffusion. However, when the source workfunction is greater than 4.5 eV, the transport mechanism during read is dominated by band-to-band tunneling (BTBT). In general, when the dominant mechanism of current transport is BTBT, the retention time and the read-1/0 current ratio is higher, and the sense margin is lower in the case in which the dominant mechanism of current transport is drift-diffusion. Due to the avoidance of doping, the proposed DL-DRAM is expected to be free from random dopant fluctuation. Moreover, high temperature annealing processes required after ion implantation can be avoided. The lower thermal requirements of a DL-DRAM opens the possibility of fabricating DRAMs using processes which are compatible with bio-materials and opto-electronics and in ensuring bottom MOSFET and interconnects preservation in 3D VLSI integration.

INDEX TERMS DRAM, dopingless, sense margin, retention time, charge plasma.

I. INTRODUCTION

Dynamic random access memory (DRAM) has been at the forefront of low cost and large scale memories. Earlier, DRAMs used 1 transistor and 1 capacitor (1T-1C) to store data. Over the years, the demand for larger memories has shifted the research to capacitorless single-transistor 1T DRAMs which have the storage capacitor mechanism built into them. Conventional MOSFET structures that utilize floating body capacitance and body charging effects have been proposed to be used as a 1T-DRAM [1], [2]. Tunnel field-effect transistors (TFET) because of their excellent subthreshold swing and weak temperature dependence are also being extensively explored for 1T-DRAM applications [3]–[9].

With scaling down of technologies, the density of transistors increases and more bits of information can be stored in the same chip area. However, there are several fabrication and design challenges at advanced process nodes [10]. Random dopant fluctuation (RDF) has been identified as a major obstacle to device scaling [11], [12]. RDF is the variation in the number and position of dopants in the channel, source and drain regions. It has been shown that, due to RDF, there is a large variation in the threshold voltage in an array of DRAM cells [13]. Since the retention time (RT) of a DRAM is determined by its threshold voltage, RDF can result in a significant decrease in the RT. Furthermore, the impact of RDF in a Floating Body Cell (FBC) based DRAM is shown to aggravate at smaller device dimensions [14]. Additionally, in a DRAM that utilizes impact ionization for its operation, RDF strongly affects the impact ionization rate and consequently the electrical characteristics are adversely affected. Similarly, RDF has a strong impact on the band-to-band tunneling (BTBT) rate in a TFET and can have detrimental effects on the characteristics of DRAMs based on the BTBT

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phenomenon [15], [16]. Further, it has been demonstrated that RDF results in a large variation in the leakage current in a DRAM [17]. Therefore, the refresh time of an array of DRAMs, which is determined by the DRAM cells that are more susceptible to variations such as RDF, increases. For a Silicon-on-Insulator-based 1T DRAM, the critical parameters contributing to the variability are silicon film thickness, thickness of the buried oxide and RDF [18]. These variations can reduce the RT in a DRAM by 63% for the $22 - nm$ technology node. Therefore, the problem of RDF needs to be addressed for DRAMs, especially at smaller device dimensions.

Recently, many groups have proposed dopingless devices to tackle RDF. As dopingless devices do not use external dopants, they can be fabricated without using ion implantation. Dopingless Field-effect transistor (FET), tunnel field effect transistor (TFET), Zero-slope and zero-impact ionization FET(Z^2-FET) and bipolar charge plasma transistors (BCPT) have been proposed in literature [19]–[22]. A dopingless device implementing a charge plasma diode is experimentally demonstrated in [23] and [24].

In this paper, we propose a Dopingless DRAM (DL-DRAM) implemented using charge plasma concept and is expected to be free from RDF. To the best knowledge of the authors, a dopingless DRAM is being proposed for the first time in the literature. Furthermore, high temperature annealing processes required after ion implantation can be avoided [20]. The lower thermal requirements of a DL-DRAM opens the possibility of fabricating DRAMs using processes which are compatible with bio-materials and opto-electronics [20]. Moreover, in 3D integrated circuits, avoiding high temperature process in DRAM fabrication can address the challenge of realizing memories at the top level without impacting the electrical characteristics of the bottom one [27], [28].

The proposed DL-DRAM employs a misaligned double-gate architecture. In a typical misaligned-gate architecture, the backgate has a stronger control over storing charge carriers in the write operation and the frontgate has a stronger control over the current in the read operation [7]. Fabricating misaligned-gate structures is possible using electrical vernier shifting proposed in [27]. A vertical FinFET-like structure where the top gate has been removed using etching or chemical mechanical polishing can also be used [28]. After the top gate removal, the misalignment in the gates can be patterned using different gate masks [7]. In the proposed DL-DRAM, the device employs tunneling-based read mechanism for source workfunction $\phi_s > 4.5\ eV$ and drift-diffusion for source workfunction $\phi_s < 4.5eV$.

The rest of this paper is organized as follows. In section II, the device structure of the proposed DL-DRAM and the simulation model are described. In section III, the operating mechanism of the DL-DRAM is explained in detail. In section IV, the characteristics of the proposed device is described, highlighting its unique features. In section V, the comparison of the proposed DRAM with other reported DRAMs is done. Finally, in section VI, conclusions are made.

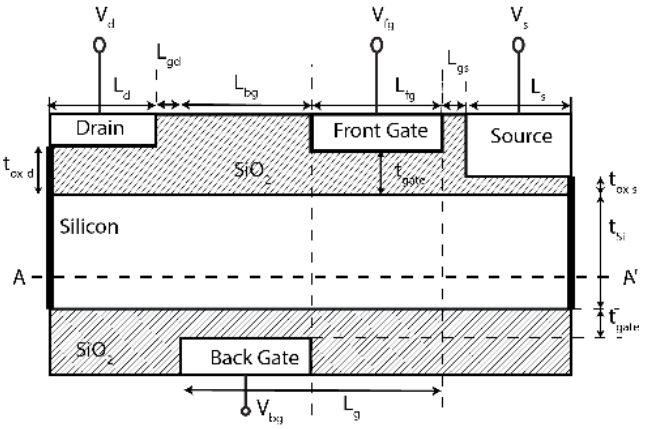

FIGURE 1. Cross-sectional view of the proposed dopingless DRAM (DL-DRAM).

TABLE 1. Device parameters used in simulation of DL-DRAM.

Parameter	Value
Silicon film thickness (t_{si})	10 nm
Gate oxide thickness (t_{gate})	3 nm
Back-gate/Front-gate length (L_{bg}/L_{fg})	100 nm
Front-gate workfunction (ϕ_{fg})	4.17 eV
Back-gate workfunction (ϕ_{bg})	5.25 eV
Drain–substrate oxide thickness (t_{ox-d})	3 nm
Source–substrate oxide thickness (t_{ox-s})	0.5 nm
Gap between front-gate and source (L_{gs})	15 nm
Gap between back-gate and drain (L_{gd})	10 nm
Drain workfunction (ϕ_d)	3.9 eV
Source workfunction (ϕ_s)	3.9-5.93 eV
Source/Drain Length (L_s/L_d)	50 nm

II. DEVICE STRUCTURE AND SIMULATION MODELS

The cross-sectional view of the proposed Dopingless DRAM (DL-DRAM) is shown in Fig. 1 and the corresponding device parameters are listed in Tab. 1. The device employs a thin-film intrinsic silicon. The silicon body thickness t_{si} is less than the Debye length limit $L_D = \sqrt{\epsilon_{si} V_T / qN}$, where ϵ_{si} is the dielectric constant of silicon, V_T is the thermal voltage and N is the carrier concentration in the silicon body. A small t_{si} ensures that the induced concentration profiles in the source and the drain regions remain constant across the silicon body [23].

In the proposed device, we have two misaligned gates, one at the front or top surface and one at the back or bottom surface. The workfunction of the front and the back gates are taken as 4.17 eV and 5.25 eV, respectively. These workfunctions can be obtained using n^+ poly, p^+ poly or suitable metal gates [29], [30]. The existence of low workfunction

TABLE 2. Optimized programming biases.

Operation	V_{fg}(V)	V_{bg}(V)	V_d(V)	V_s(V)
Write-1	0	-3	0	0
Write-0	0	3	0	0
Read	2	1.1	1	0
Hold	0	-0.8	0	0

frontgate leads to accumulation of electrons under the frontgate. Similarly, the existence of high workfunction backgate leads to accumulation of holes under the backgate. At equilibrium, the electron concentration is $7 \times 10^{17}\ /cm^3$ in the channel under the frontgate and the hole concentration is $4 \times 10^{17}\ /cm^3$ in the channel under the backgate. The length of the top and the bottom gates is taken as 100 *nm*. A larger gate length simplifies the understanding of the physical phenomenon in the device.

In a DL-DRAM, the drain and the source regions are formed using the charge plasma concept. An electron or hole plasma can be formed in a device by choosing appropriate workfunction of the source, the drain and the gate material. A silicon dioxide layer is inserted between source–substrate and drain–substrate to avoid the possibility of silicide formation [20]. A thinner source–substrate oxide allows obtaining a higher concentration of holes in the induced source region facilitating band-to-band tunneling (BTBT) [20]. It is worthy to point out that negligible current flow through these oxides because a low resistance path exists through the induced source/drain regions. In this work, the drain workfunction is fixed to 3.9 eV and the source workfunction is varied between $3.9 - 5.93\ eV$. A workfunction of 3.9 eV can be obtained using Hafnium and a workfunction of 5.93 eV can be obtained using Platinum [20]. A low workfunction leads to the formation of an electron-rich region around the drain. For a source/drain workfunction of 3.9 eV, simulation shows that the electron concentration is approximately $1 \times 10^{18}\ /cm^3$ near the source/drain regions. The fabrication of source and drain contacts can be done using sputtering, as described in [24]. Notably, thermal treatment should be avoided to suppress metal-silicide formation and resultant variation in the effective workfunction [24].

In this work, all simulations are done using Silvaco ATLAS version 5.22.1.R in two-dimensional mode [31]. To account for the mobility variations due to concentration and electric field, Lombardi mobility model has been included [31]. We have also included concentration dependent Shockley-Read-Hall (SRH) recombination model [31]. Furthermore, we have included the non-local BTBT model to account for the tunnelling phenomenon observed in certain modes of operation [31]. We have calibrated the tunneling model by reproducing the results presented in [20] and also validated our simulation model using the results presented for a DRAM in [7]. For simplicity, we have not considered interface traps and tunneling through thin oxide in this work, similar to previous studies [6]–[9], [20]–[22]. We have taken the temperature as 300 K throughout this study.

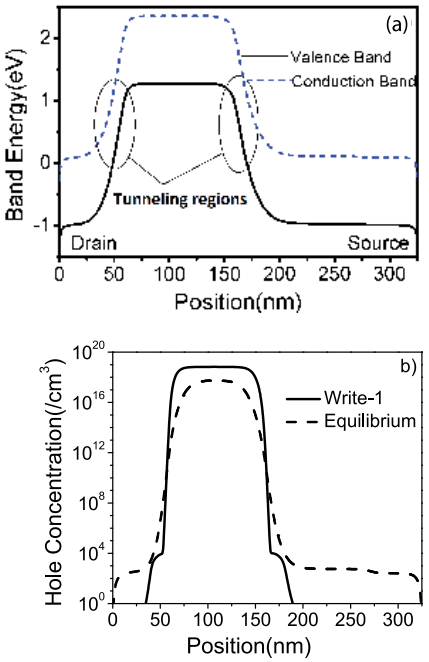

FIGURE 2. For write-1 operation (a) The conduction band and the valence band align to allow BTBT. The band diagram is plotted along the cutline AA′ marked in Fig.1 (2nm above back interface) (b) Hole concentration at equilibrium and after write-1 operation of 50 *ns* along the cutline AA′.

III. DEVICE OPERATING MECHANISM

A. WRITE

The mechanism of current transport and storage of data is different in write-1 and write-0 cases. We describe them separately in the following paragraphs.

1) WRITE-1

The write-1 is done by applying a negative voltage of $-3\ V$ at the backgate while keeping all other terminal voltages at zero. This creates a potential well under the backgate in the silicon body. The potential well is enclosed by two reverse-biased junctions, as shown in Fig. 2(a). A sharp band-bending and the overlap between the valence band and the conduction band allows BTBT to occur, as shown in Fig. 2(a). As a result, the electrons tunnel from the backgate region towards the drain region and towards the frontgate region. The tunneling away of electrons from the potential well further accumulates holes and the electron concentration at the backgate decreases. The holes move into the backgate region from the drain region and the frontgate region. There is a vertical drift of holes as well from the top of the backgate region to the bottom of the backgate region due to the applied negative potential at the backgate. However, the vertical component of hole drift current is less than the horizontal component. This increases the hole concentration in the backgate region from $4 \times 10^{17}\ /cm^3$ to $2 \times 10^{18}\ /cm^3$, as shown in Fig. 2(b).

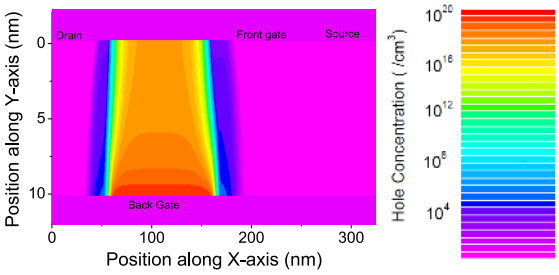

FIGURE 3. The hole concentration profile after 50 *ns* of write-1 operation for $\phi_S = 3.9\ eV$.

The 2-D hole concentration profile after write-1 is shown in Fig. 3, illustrating that the region of stored charges in DL-DRAM is above the backgate. The BTBT rate decreases with increase in write-time and a stable value of hole concentration in the potential well is reached after the write-1 cycle.

2) WRITE-0

The write-0 is performed on application of $+3\ V$ at the backgate while keeping all other terminal voltages at zero. The positive potential expels out the holes from the backgate region. The expelled holes spread out towards the source. The hole concentration in the backgate region declines with time due to recombination in the silicon body and at the source–silicon interface. The hole concentration profile after write-0 is shown in Fig. 4(a). The positive potential at the backgate leads to an increase in the electron concentration at the backgate region due to drift from the drain region and the frontgate region. The potential well that was created during write-1 operation is no longer available. The potential profiles after write-1 and write-0 are compared in Fig. 4(b).

B. HOLD

After writing a data into the DRAM, the data needs to be held for some time. During the hold operation, the holes are stored in the potential well in the silicon body at the backgate that was created during write-1 operation. A bias condition that retains these holes for a longer time will result in a higher RT. Therefore, a small negative voltage is applied at the backgate to hold the holes in the potential well. However, the bias under the hold condition should also ensure that the '0' and '1' states are distinguishable, as explained in the next section. The hole concentration at the bottom of the backgate region is around $1.6 \times 10^{18}\ /cm^3$ after a hold operation of 1 *ms*. Thus, a thin silicon body of 10 *nm* is also able to sustain the potential well required for holding the holes. During hold-1 the electron concentration in the backgate region gradually increases as the negative potential applied at the backgate during hold operation is not sufficient to sustain the BTBT occurring during write-1 which was responsible for draining the electrons from the backgate region. During hold-0, the negative potential at the backgate expels out some of the electrons which drifted into the backgate region during write-0. As a result, the electron concentration in the backgate region decreases during hold-0.

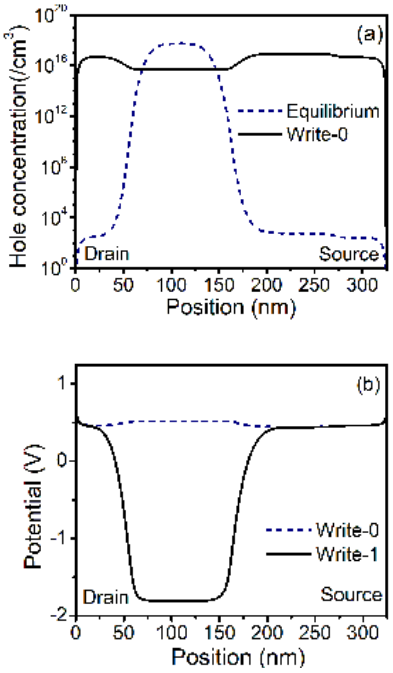

FIGURE 4. For write-0 operation (a) Hole concentration profile along the cutline AA′ marked in Fig. 1 after write-0 of 50ns (b) Potential profile along the cutline AA′ marked in Fig. 1 after write-1 and write-0 of 50ns. There is no potential well to store charge in write-0.

C. READ

During read operation, a positive potential of $V_d = 1\ V$ is applied, followed by $V_{fg} = 2\ V$ and $V_{bg} = 1.1\ V$. Our simulations show that the mechanism of reading is different when the workfunction of the source (ϕ_s) is low and when it is high. Therefore, we discuss the read mechanism for the two cases: $\phi_s < 4.5\ eV$ and $\phi_s > 4.5\ eV$.

1) $\phi_S < 4.5\ eV$

When $\phi_s < 4.5\ eV$, the dominant mechanism of current transport is drift-diffusion of carriers in the bulk, followed by recombination at the source, both during read-1 and read-0.

- **Read-1:** The bias $V_{bg} = 1.1\ V$ switches-ON the transistor. The positive drain voltage and the positive backgate voltage drives away holes from the drain region and the backgate region towards the source region and into the bulk. Furthermore, the higher concentration of holes in the backgate compared to the frontgate region causes diffusion of holes towards the source region. Thus, the stored holes are disturbed during read operation, similar to a conventional 1T/1C DRAMs [8]. The charges in the potential well can be restored by writing back into the cell right after the read operation. The holes flowing into the frontgate region and source region encounter a large concentration of electrons existing there, recombine with them and are lost [8]. The holes being injected

into the frontgate and the source regions are minority carriers in the region. Electrons are the majority carriers in the device and drift/diffuse into the drain region. The positive frontgate voltage induces a high concentration of electrons below the frontgate in the channel and near the source region. However, the positive drain voltage pulls the electrons away towards the drain region and the backgate region. As a result, the electrons redistribute such that almost a constant electron concentration is achieved throughout the device. The recombination current and the drift-diffusion current of the electrons together yield a high current in read-1.

- **Read-0:** During read-0, the hole concentration in the backgate region is less than the equilibrium value as shown in Fig. 4(a). As a result, the threshold voltage of the transistor is greater in read-0 condition compared to read-1 condition [32]. Therefore, a lower current flows in read-0 compared to read-1. Moreover, the absence of holes under backgate in read-0 condition results in a smaller flux of holes from the backgate region towards the bulk and the source regions. Therefore, smaller recombination rate exists under read-0 condition compared to read-1 condition. This results in a smaller recombination current in read-0. Thus, we are able to distinguish between logic '1' and '0' based on the read currents.

2) $\phi_S > 4.5\ eV$

- **Read-1:** As the source workfunction increases, the concentration of holes in the source region increases. As a result the junction between the channel region under the frontgate and the source becomes reverse biased during read operation. This reverse biasing causes alignment of the conduction and the valence bands energy levels near the above-mentioned junction and enables BTBT of electrons from the source into the channel, as shown in Fig. 5. These electrons that tunnel through the source–channel junction are pulled by the positive drain voltage towards the drain terminal and, thus, contribute to the drain current. This decreases the electron concentration in the source region drastically. Further, the hole concentration at the backgate region decreases gradually in read mode due to recombination with the tunneled electrons. However, due to high tunnel resistance, the drain current is small in this case compared to $\phi_s < 4.5\ eV$. As ϕ_s is increased, the tunneling probability increases because of the increase in energy overlap window and decrease in the tunneling width, as shown in Fig. 5.
- **Read-0:** When '0' is read, drain current flows due to BTBT. However, the current is smaller during read-0 due to greater tunneling width and smaller energy overlap, as shown in Fig. 6. Further, a lower hole concentration at the backgate during read-0 increases the effective energy barrier seen by the drifting electrons in the channel, as shown in Fig. 6. As a result, read-0 current is smaller than read-1 current.

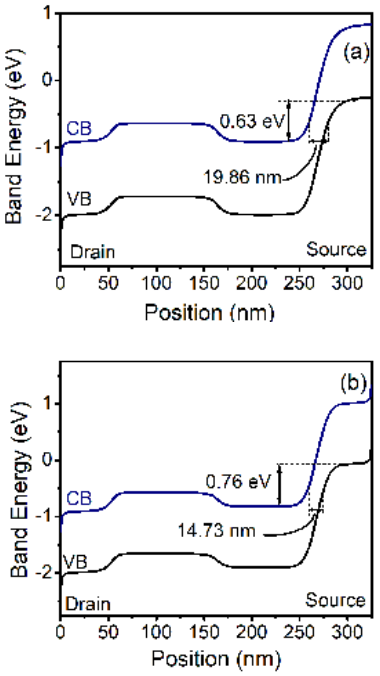

FIGURE 5. Band diagrams along the cutline AA′ marked in Fig. 1 during read-1. The energy band overlap values and the minimum tunneling width are indicated. (a) $\phi_S = 5.0\ eV$ (b) $\phi_S = 5.5\ eV$.

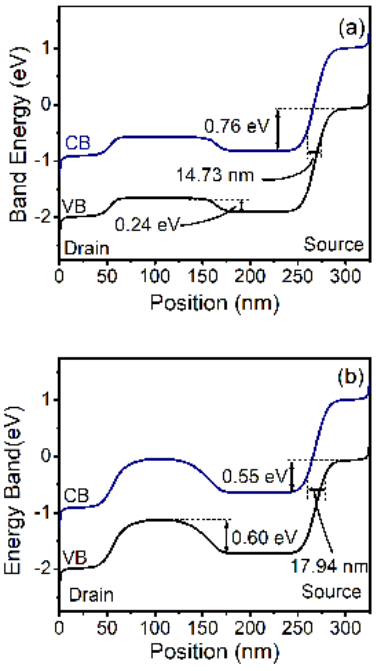

FIGURE 6. Band diagrams along the cutline AA′ marked in Fig. 1 for $\phi_S = 5.5\ eV$. Energy barrier heights, energy overlap window and minimum tunneling width are indicated (a) read-1 (b) read-0.

It is important to point out that the read mechanism in DL-DRAM is BTBT, which, in general, supports a low drain current due to the large bandgap of silicon [33]. The ON-state current of the DL-DRAM (at $V_d = 1\ V$, $V_{fg} = V_{bg} = 2\ V$) is 39.6 $nA/\mu m$, which is quite low. Therefore, it is important

to evaluate the effect of dopingless structure on the ON-state current. A doped device similar to the DL-DRAM (with a source doping of $1 \times 10^{20}\ /cm^3$ and drain doping of $1 \times 10^{20}\ /cm^3$) was simulated. The ON-state current of the doped DRAM (at $V_d = 1\ V$, $V_{fg} = V_{bg} = 2\ V$) is $30\ nA/\mu m$, which is similar to that of the DL-DRAM. Further, the impact of source/drain lengths (L_s and L_d) in DL-DRAM was assessed by varying them from 50 *nm* to 200 *nm*. It was found that the source/drain parasitic resistance of the DL-DRAM has negligible effect on the ON-state current. The source and drain resistances are in series with the tunnel resistance at the source–channel junction [34]. Since source–channel tunnel resistance is much larger compared to the source/drain parasitic resistance, the impact of source/drain parasitic resistance and the dopingless structure has negligible impact on the ON-state current in a DL-DRAM working in the BTBT mode.

IV. DEVICE CHARACTERISTICS

A. DEVICE BIAS AND PARAMETER OPTIMIZATION

The device parameters and the bias conditions can be optimized to obtain a high sense margin (SM) and the RT. It was found that the SM increased with a decrease in the source workfunction ϕ_s. The highest SM of 169 μA was obtained for $\phi_s = 3.9\ eV$. Therefore, the bias conditions were optimized for $\phi_s = 3.9\ eV$, as explained below.

1) V_{bg} IN HOLD OPERATION

The voltage V_{bg} applied during hold operation can be optimized to achieve the best retention time. Retention time (RT) is defined as the time taken for the SM to fall to 50% of its original value. Recombination of holes with electrons degrades the stored logic '1', while generation of electron–hole pairs due to BTBT degrades logic '0'. Since holes are stored during write-1, a small negative voltage at the backgate can facilitate retaining holes for a longer duration by maintaining the potential well. However, a large negative voltage during hold operation would corrupt the state '0'. The RT for different hold voltages are shown in Fig. 7(a). The highest RT of 70 *ms* is obtained at a hold voltage of $-0.8\ V$. However, depending on the hole concentration at the backgate during write-1, the optimum value of the hold voltage can be different. As a result, the backgate voltage at which the maximum RT is obtained is different for different ϕ_s. For instance, the optimal hold voltage for $\phi_s = 4.5\ eV$ and $\phi_s = 5.93\ eV$ are found to be $-0.4\ V$ and $-0.6\ V$, respectively.

2) V_{bg} IN READ OPERATION

The read current and the SM depend on the V_{bg} applied during read operation. The dependence of the read-1/read-0 current on V_{bg} is shown in 7(b). Both read-1 and read-0 current increase with increased V_{bg}. This can be attributed to the increase in the carrier concentration in the device due to increased V_{bg}. However, the increase in read-0 current is greater than the increase in the read-1 current, when V_{bg} is too high. When V_{bg} is lower than the threshold voltage then the read-0 current is quite low, and when V_{bg} becomes appreciably higher than the threshold voltage then a large read-0 current is observed. However, the threshold voltage of the transistor is lower in read-1 condition than in read-0 condition, as explained in the previous section. Consequently, for read-1 case, when $V_{bg} > 0.4V$ the transistor is already in the super-threshold region and a high read-1 current is obtained. As a result, the SM (i.e. the difference between the read-1 current and the read-0 current) increases with increase in V_{bg}, reaches a maximum at $V_{bg} = 1.1\ V$ and then decreases for $V_{bg} > 1.1\ V$.

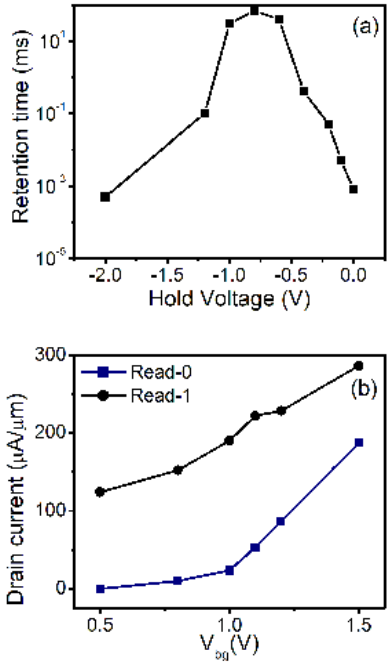

FIGURE 7. (a) Variation of RT with hold voltage for $\phi_s = 3.9\ eV$. The maximum RT of 70 *ms* is obtained at $-0.8\ V$ (b) Variation in read-1 and read-0 drain current with backgate voltage (V_{bg}) ($\phi_s = 3.9\ eV$).

3) GAP BETWEEN BACK-GATE AND DRAIN (L_{gd})

As L_{gd} is increased, the read current and the SM is found to decrease, both for $\phi_s = 3.9\ eV$ and $\phi_s = 5.93\ eV$, as shown in Fig. 8(a). This can be attributed to the increase in the series resistance in the channel due to drain-gate underlap. Therefore, $L_{gd} \approx 0$ maximizes SM in the DL-DRAM. As L_{gd} is increased, the RT is found to increase, for both $\phi_s = 3.9\ eV$ and $\phi_s < 5.93\ eV$, as shown in Fig. 8(b). This behavior can be explained on the basis of reduced drain current leading to slower dissipation of the stored charges.

4) GAP BETWEEN FRONT-GATE AND SOURCE (L_{gs})

As L_{gs} is increased, the read current and the SM is found to decrease, for $\phi_s < 4.5\ eV$. This can again be attributed to the increase in the series resistance in the channel due to source-gate underlap. However, when $\phi_s > 4.5\ eV$ (in this case BTBT near the source dominate), a peak SM of

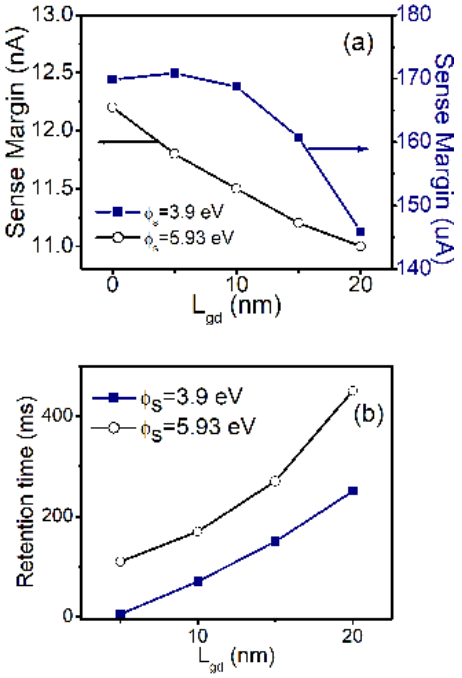

FIGURE 8. Variation of a) SM b) RT with L_{gd} (L_{gs} = 15nm).

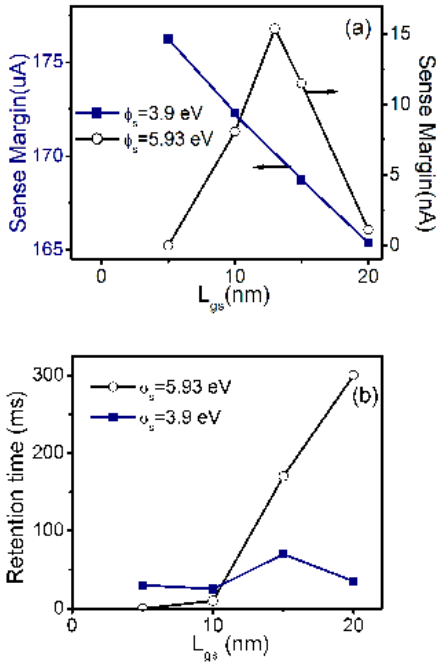

FIGURE 9. Variation in a) SM and b) RT with L_{gs} (L_{gd} = 10 nm).

15.4 nA is obtained at $L_{gs} = 13\ nm$, as shown in Fig. 9(a). As L_{gs} is increased, the minimum tunneling width increases and the read current is expected to decrease. However, when L_{gs} is increased, the energy window or conduction-valence band overlap also increases, leading to an increase in read current. Thus, due to the two competing factors, the impact of L_{gs} on the SM exhibits a trend shown in Fig. 9(a). For instance, the SM decreases when $L_{gs} < 13\ nm$ because the

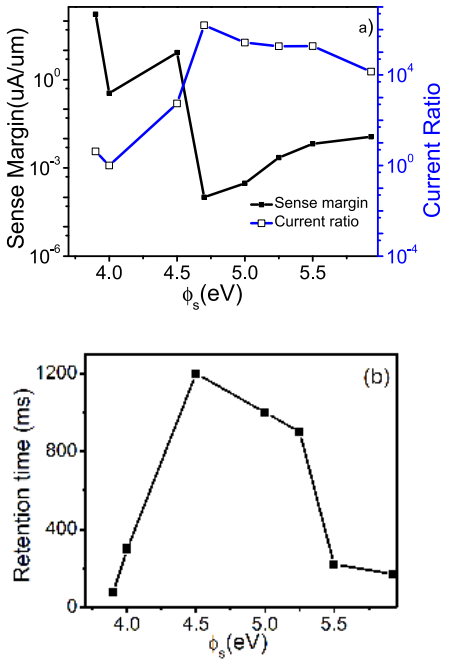

FIGURE 10. Effect of source workfunction ϕ_S on (a) SM and one/zero current ratio (b) RT.

impact of decrease in conduction-valence band overlap is dominant over the decrease in the minimum tunneling width. The variation in RT with L_{gs} is shown in Fig. 9(b). As L_{gs} is increased, in general, the RT increases which can be attributed to a decreased drain current and slower dissipation of the stored charges.

5) DRAIN-SUBSTRATE OXIDE THICKNESS (t_{ox-d})

As the oxide thickness over drain t_{ox-d} is increased, the drain current decreases due to a lower concentration of electron in the induced drain region. As a result, there is a slower loss of charge and the RT increases. However, when $t_{ox-d} > 3.5\ nm$, the impact of further increasing t_{ox-d} becomes greatly reduced. Moreover, due to decrease in drain current, the SM decreases with an increase in t_{ox-d}. Therefore, $t_{ox-d} = 3\ nm$ is chosen, which achieves a high RT, along with a moderate SM.

6) SILICON FILM THICKNESS (t_{si})

For $\phi_s < 4.5\ eV$, as t_{si} is increased, the read-1 current is found to decrease due to diminished gate control. For $\phi_s > 4.5\ eV$ also, as t_{si} is increased, the read-1 current is found to decrease due to decreased BTBT. As a result, in general, the SM decreases with increase in t_{si} in a DL-DRAM. Moreover, typically, the RT of DL-DRAM increases as t_{si} is increased. This is primarily because of slower degradation of state '0' by the accumulation of holes in thicker devices.

B. IMPACT OF SOURCE WORKFUNCTION ϕ_S

The source workfunction ϕ_s plays the most important role in governing the read-mechanism of the DL-DRAM. Therefore,

the electrical parameters such as the SM, read-1/read-0 current ratio and the RT depend strongly on ϕ_s. The dependence of these parameters on ϕ_s is shown in Fig. 10 and the following inferences can be made:

1) When the dominant mechanism of current transport is drift-diffusion in the read-mode ($\phi_s < 4.5\ eV$), the SM decreases as the ϕ_s is increased. When the dominant mechanism of current transport is BTBT in the read-mode ($\phi_s > 4.5\ eV$), the SM increases as the ϕ_s is increased. However, the trend is opposite for the RT in both the cases. The RT of the DRAM decreases as the ϕ_s is tuned to get an increased SM. Therefore, in both the mode of operation (drift-diffusion or BTBT) a designer needs to make a trade-off between the SM and the RT.
2) In general, when the dominant mechanism of current transport is BTBT, the RT is larger and the SM is smaller than in the case in which the dominant mechanism of current transport is drift-diffusion. Therefore, when a designer prefers lower refresh rates, a ϕ_s that would make the read-mechanism BTBT would be desirable. A longer RT can improve the efficiency of the system by reducing the overhead of the refresh cycle [35]. However, if a higher read-current and SM is required then a ϕ_s that would make the read-mechanism drift-diffusion would be desirable. It is also important to point out that when a ϕ_s is chosen such that the read-mechanism is BTBT then a higher read-1/read-0 current ratio can be obtained.

C. SCALABILITY OF A DL-DRAM

Since a DL-DRAM is proposed to be used in future, it is important to assess its scalability and behavior at smaller gate lengths. The variation of SM with total gate length is shown in Fig. 11 (a). For $\phi_s = 3.9\ eV$, as the channel length is decreased, initially the SM increases due to the increase in both the read-0 and the read-1 current resulting from the lowering of the barrier seen by the drifting electrons. However, at very small channel lengths, the read-0 current increases more rapidly compared to read-1 current, leading to a decrease in the SM. For $\phi_s = 5.93\ eV$, as the channel length is decreased, the read-1 current decreases and the read-0 current increases, leading to a decrease in the SM. Fig. 11 (b) shows the RT of a DL-DRAM as the total gate length is decreased from 600 *nm* to 100 *nm*. As the length of the DL-DRAM is decreased, the volume of silicon available for storing holes decreases. Therefore, with the reduction in gate length, the RT of a DL-DRAM decreases. However, even for a total gate length of 100 *nm* the RT is 62 *ms* for $\phi_s = 3.9\ eV$ and 110 *ms* for $\phi_s = 5.93\ eV$.

It is worth pointing out that an important metric for a DRAM is its density. To estimate the density of the proposed DL-DRAM and the area of the unit cell, firstly we analyze the impact of the width of the device on the SM and the RT. We found that the RT does not change appreciably with the width of the device and the SM decreases with the decrease in the width of the device. For a DL-DRAM of width 200 *nm* and total gate length 200 *nm*, the SM is 34 μA and the RT is 70 *ms* for $\phi_s = 3.9\ eV$. In a unit memory cell design that shares the source line, the area factor can be estimated as $12F^2$ [3]. Since MOSFET-based DRAMs exhibit an area factor of $6F^2$, the results indicate that DL-DRAM also requires improvement in area factor to be competitive with the MOSFET-based DRAMs [3], [7], [36].

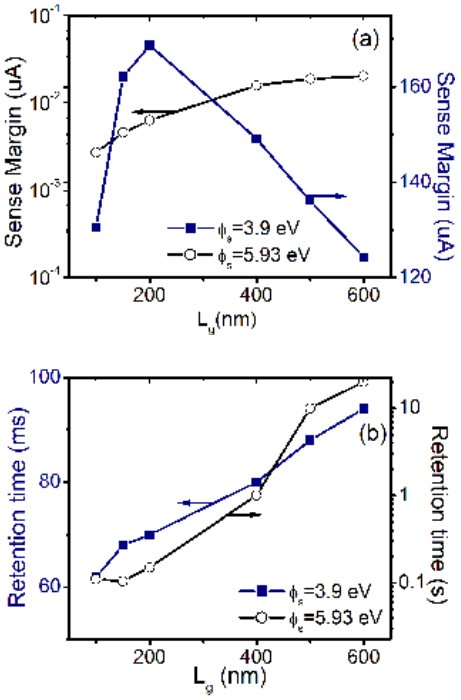

FIGURE 11. Variation in a) SM and b) RT with total gate length (L_g). The top and the bottom gate lengths are $L_g/2$.

D. IMPACT OF VARIATIONS

The proposed DL-DRAM is expected to tackle variations due to RDF. However, it is important to assess the impact of other sources of variability in a DL-DRAM. Two important sources of variations expected in a DL-DRAM are: a) misalignment of the top and bottom gates b) workfunction variations of source, drain and gates.

Our simulations show that the misalignment of the top and the bottom gates by ± 5 *nm* leads to a decrease of SM from 169 *uA* to 161 *uA* and a decrease in the RT from 70 *ms* to 64 *ms* for $\phi_s = 3.9\ eV$. The maximum decrease in the SM is observed when the bottom gate shifts towards the source side (keeping the top gate at the same position) for $\phi_s = 3.9\ eV$. However, when a DL-DRAM operates in the BTBT mode, the impact of gate misalignment is more severe. The maximum decrease in the SM is observed when the top gate shifts towards the drain side creating gate-source underlap. This is expected since a gate-source underlap leads to a large increase in the tunnel width and the consequent reduction in

TABLE 3. Comparison of DL-DRAM with other emerging 1T DRAMs.

No.	Reference	Channel Length (nm)	SM	RT (ms)
1	UTBOX TFET [3]	600	$20\ nA$	NA
2	Fin-based TFET [4]	200	$10\ nA$	10
3	DGTFET [7]	270	$30\ nA$ $(85^\circ C)$	1200
4	Z^2-FET [38]	400	$40\ uA$	>500
5	Z^2-FET [34]	600	$70\ uA$	5500
6	This Work ($\phi_s = 3.9\ eV$)	225	$169\ uA$	70
7	This Work ($\phi_s = 5.93\ eV$)	225	$12\ nA$	170

the drain current [37]. A gate-source underlap of 5 *nm* reduces the SM from 11.5 *nA* to 1.2 *nA* and the RT from 170 *ms* to 6 *ms* for $\phi_s = 5.93\ eV$. Therefore, when a DL-DRAM is designed to operate in BTBT mode, then the gate-source underlap is detrimental to DRAM operation similar to a TFET.

In the proposed device, the workfunction of the gates, source and drain can exhibit variations. For instance, the variations in the size and the orientation of metal grains can lead to workfunction variations and impact the electrical characteristics of a DL-DRAM. To quantify the impact of the workfunction variations in a DL-DRAM, ideally a statistical approach should be taken [13], [38], [39]. However, for simplicity, we have estimated the impact of workfunction variations in a DL-DRAM by varying the workfunction by $\pm 0.1\ eV$. The simulation results show that the impact of workfunction variations is stronger for the bottom gate than the top gate. This is expected since the bottom gate has a greater control over the potential well that stores charge. For a $\pm 0.1\ eV$ variations in workfunction of the bottom gate, the SM reduces by 18% and the RT reduces from 70 *ms* to 21 *ms*. Moreover, the source workfunction variations have a greater impact on the SM and the RT, than the drain workfunction variations. The impact of source workfunction on the SM and the RT is already illustrated in Fig. 11. Therefore, it is highly desirable to control the variations in workfunction of the bottom-gate and the source in a DL-DRAM.

V. COMPARISON WITH OTHER EMERGING 1T DRAMS

Tab. 3 compares important attributes of a DL-DRAM operating in two modes with other 1T DRAMs proposed in literature and employ conventional doping. In drift-diffusion mode of operation ($\phi_s = 3.9\ eV$), the SM of the proposed device is greater than the SM of other emerging devices, though the RT is low. In the BTBT mode of operation ($\phi_s = 5.93\ eV$), the SM is in order of tens of nano-amperes which is of similar order as reported for other emerging DRAMs operating on the same principle. The RT in BTBT mode of operation is greater than drift-diffusion mode of operation, although it is less than what is reported in [7]. This points out that the DL-DRAM requires further improvement in BTBT mode of operation, perhaps using architectural modifications or material engineering.

VI. CONCLUSION

In this paper, using simulations, we have demonstrated that a dopingless DRAM can be realized using charge plasma concept. The proposed device simplifies the fabrication process and can avoid high thermal budgets required to create source and drain openings. The proposed device is immune to RDF due to the absence of dopant atoms. Since RDF is known to decrease the RT in a DRAM and its impact worsens with scaling, the proposed device can be employed in future as 1T DRAMs. Furthermore, we have shown that the proposed architecture is flexible enough to change the read mechanism from drift-diffusion to BTBT by varying the source workfunction.

The results presented in this paper demonstrate that the electrical characteristics such as the SM and the RT obtained for the proposed dopingless device are comparable to the emerging DRAMs realized using conventional doping. However, considering future applications, more investigation is required in improving the density, compatibility with the existing fabrication technology, high temperature operation including impact of temperature variations and immunity against process-induced variations.

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