Open access • Proceedings Article • DOI:10.1145/1118299.1118374

# Double edge triggered Feedback Flip-Flop in sub 100NM technology



Seid Hadi Rasouli, Amir Amirabadi, Azam Seyedi, Ali Afzali-Kusha

**Institutions:** University of Tehran

**Published on:** 24 Jan 2006 - Asia and South Pacific Design Automation Conference

**Topics:** Subthreshold conduction and Dynamic demand

# DOUBLE EDGE TRIGGERED FEEDBACK FLIP-FLOP IN SUB 100NM TECHNOLOGY

S. H. Rasouli
Nanoelectronics Center of Excellence
ECE Dept.
University of Tehran
Tehran , Iran
Tel: 9821-8209-4359
Email: s_hrasouli@yahoo.com

A. Amirabadi
Nanoelectronics Center of Excellence
ECE Dept.
University of Tehran
Tehran , Iran
Tel: 9821-8209-4359
Email: A.amirabadi@ece.ut.ac.ir

A. Seyedi
Nanoelectronics Center of Excellence
ECE Dept.
University of Tehran
Tehran , Iran
Tel: 9821-8209-4359
Email: A.Seyedi@ece.ut.ac.ir

A. Afzali-Kusha
Nanoelectronics Center of Excellence
ECE Dept.
University of Tehran
Tehran , Iran
Tel: 9821-8209-4359
Fax: 9821-8877-8690
Email: afzali@ut.ac.ir

**ABSTRACT**

**In this paper, a new flip-flop called Double-edge triggered Feedback Flip-Flop (DFFF) is proposed. The dynamic power consumption of DFFF is reduced by avoiding unnecessary internal node transition. The subthreshold current in the flip-flops is very low compared to other structures. Reducing the number of transistor in the stack and increasing the number of charge path leads to higher operational speed compared to others flip-flops. The simulation results show an improvement of 44% in the speed and 45% in the static leakage power.**

## 1. INTRODUCTION

The power consumption of the systems is a critically important parameter in modern VLSI circuits especially for low power applications and, hence, the power optimization techniques should be applied at different levels of the digital design. One of these techniques is to use low power logic styles which should be used in design of latches and flip-flops (FF's) which are among the components widely used in digital systems [1][2]. There are other concerns in the design of DFF's such as $T_{clk\text{-}q}$ (delay from *clk* to output of FF) and $C_{clk}$ (the load capacitance of the clock) which are also should be minimized to maximize the FF performance. Among these parameters, reducing the $C_{clk}$ or the frequency of clock has a great impact on the power consumptions of clock tree and the logic [3].

In addition to the dynamic power consumption, the high leakage current in deep sub-micron regimes is a significant contributor to the power dissipation of CMOS circuits as the CMOS technology scales down [4]. The subthreshold leakage power is expected to become a significant fraction of the total power in the sub-100 nm CMOS technology where reducing the subthreshold leakage power of the circuit is crucial.

Several flip-flops have been proposed in the literature for improving the speed and/or reducing the power consumption (see, e.g. [3], [5], [7], [9]). A static single edge-triggered flip-flop called Hybrid Latch Flip-Flop (HLFF) has been proposed in [5]. It is based on generating an explicit transparency window for the time that the transition is allowed. Its idea is similar to a latch because it can provide a soft clock edge which allows for slack passing and minimizes the effect of clock skew on the cycle time [6]. However, the existence of redundant transitions in the internal nodes of HLFF leads to more power consumption. Semi-Dynamic Flip-Flop (SDFF) which is a single edge-triggered FF and faster than HLFF has been proposed in [7]. The existence of 1-1 glitch leads to an

0-7803-9451-8/06/$20.00 ©2006 IEEE.

undesired power dissipation. The number of transistors in this logic is greater than that of HLFF. Conditional Capture Flip-flop (CCFF) has been proposed to reduce redundant transitions at internal nodes [3]. The conditional capture technique needs many additional transitions for certain flip-flops which themselves cause an extra power consumption.

The dynamic power consumption in the clock tree depends on the frequency, the voltage swing, and the load of clock tree [8]. If the sampling of the input is performed in both rising and falling edge of clock (double-edge triggered), then for same applications and operational speeds, the frequency of the clock can be half of the clock frequency of the single edge triggered FF. This has been the motivation for proposing double-edge triggered flip-flops. In [9], Low-Swing clock Double-edge triggered Flip-Flop (LSDFF) has been described. In their work, the power consumption in the clock tree is reduced using a low swing clock and low-$V_{th}$ transistors in the FF. The subthreshold current of low-$V_{th}$ transistors in the main logic is controlled by high-$V_{th}$ transistors. However, the subthreshold current of low-$V_{th}$ transistors in the inverters used in the clock tree incur more power consumption especially in very deep submicron technology. Furthermore, the number of transistors in this logic is much greater than previous works.

In this paper, a Double-edge triggered Feedback Flip-Flop (DFFF) is proposed which has less dynamic power consumption, static power, and delay compared to the previous flip-flops. This paper is organized as follows. In Section 2, the structures of single-edge and double-edge triggered FF's are described and compared. The subthreshold leakage currents of the flip-flops are discussed in Section 3 while section 4 contains the simulation results. The paper ends with summary and conclusions in Section 5.

## 2. FLIP-FLOP STRUCTURES

### *A. Single-edge triggered Flip-Flops*

The structure of Hybrid Latch Flip-flop (HLFF) is shown in Figure 1 [6]. While HLFF has a very simple circuit, its unnecessary internal transitions increase the total power consumption of the flip-flop. In each clock cycle, when the input is high, regardless of previous state of the output a glitch is generated [3]. Furthermore, the transistors in the stack degrade the performance of the logic. These disadvantages make HLFF not suitable for low power applications.

In Figure 2, the circuit diagram of Semi-Dynamic Flip-Flop (SDFF) is illustrated [7]. This logic is faster than HLFF due to its lower number of transistor in the stack. However, the total number of transistors is greater than HLFF and, similar to HLFF, unnecessary internal node transitions exist in SDFF.

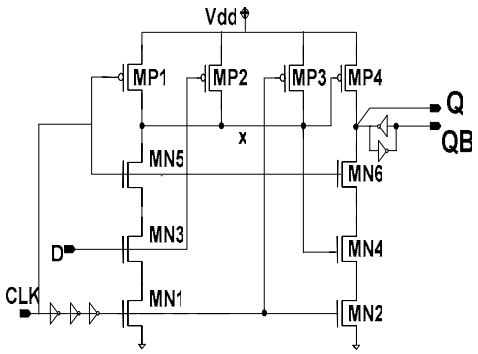



Figure 1. Circuit diagram of HLFF [6].

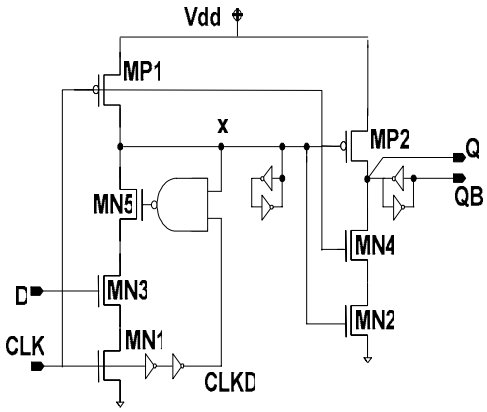



Figure 2. Circuit diagram of SDFF [7].

To see the first drawback of this FF more clearly, suppose that input is high in two successive clock cycles. Before the rising edge of the second clock, the node $Q$ is high while the node $X$ is pre-charged to $V_{dd}$. At rising edge of the second clock cycle, there is a short circuit path from $Q$ to ground until the node $X$ is discharged. This leads to a 1-1 glitch which consumes unnecessary power.

***B. Double-edge triggered flip-flops***

The circuit diagram of Low Swing clock Double edge Flip-Flop (LSDFF) is depicted in Figure 3 [9]. The input of the flip-flop is transferred to the output at the rising and falling edges of the clock. To reduce the power consumption of the clock tree, a low swing clock is used in this logic. To have a proper functioning, some of high-$V_{th}$ transistors are replaced with low-$V_{th}$ transistors whose subthreshold currents are controlled by high-$V_{th}$ transistors. For the same throughput, the frequency of the clock in LSDFF could be half of the frequency of the clock in HLFF or SDFF.

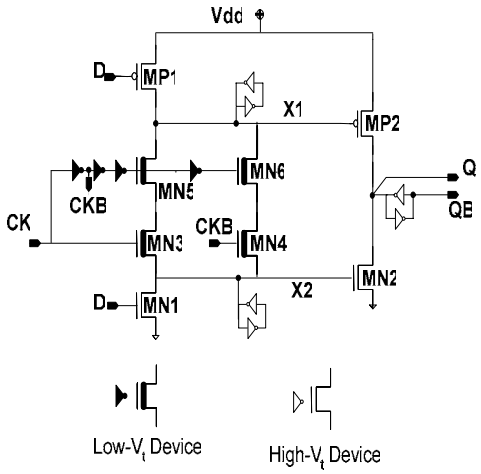
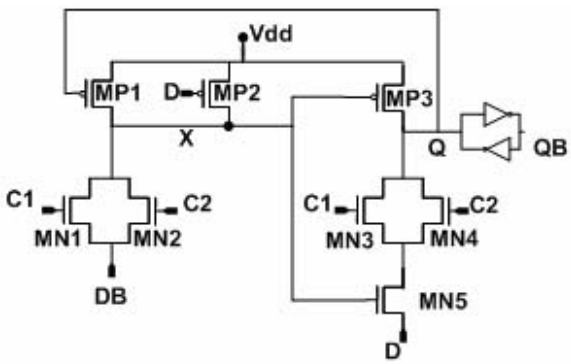



Figure 3. Circuit diagram of LSDFF [9].

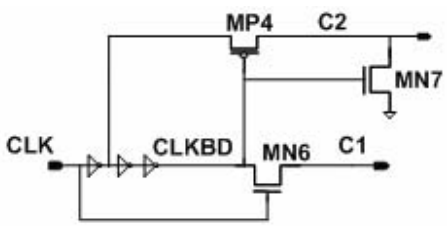
The power consumption of the clock tree is proportional to the clock load, frequency and the swing of clock. Since compared to the previous FF's, the swing and the frequency of the clock is lower, the power consumption of LSDFF clock tree could be lower than those of others. However, uncontrolled subthreshold current low-$V_{th}$ transistors in the clock tree leads to a more power consumption. In addition, since the charging (discharging) the internal node X2 (X1) is done through three transistors, the speed of the circuit is reduced.

To avoid unnecessary transitions in the previous flip-flops, we propose a Double edge-triggered feedback flip-flop (DFFF) whose circuit is shown in Fig. 4. In this flip-flop, the node transitions occur only when the inputs are different in two successive clocks. The operational principle of this work is explained here. When the clock (CLK) makes a transition from low to high, CLKBD remains high for a period equal to the delay of the three inverters creating a transparency window. In this period, C1 is high turning on MN1 and MN3. In this window, if D is low and Q is high (D was high in the previous clock), MP2 becomes on turning on MN2 which forces the output to low. If both D and Q are low, MP1 and MN2 are on before the beginning of the transparency window making the delay zero (similar to previous flip-flops). If D is high and Q is low, node X becomes low turning on MP3 which forces the output to high.

Note that, as MP1 is a weak transistor, the fighting problem during the output change is alleviated. If D is high and Q is high, node X will not change and, therefore, contrary to the other flip-flops discussed here, redundant transitions are avoided. As another advantage of this logic compared to the other flip-flops, note that there is no delay whenever D is high in two successive clock cycles. Additionally, the charging of the node X is done through two paths where one path consists of MP1 and MP2 (similar to others) and the other consists of MN1 at rising edge of the clock and MN2 at the falling edge. This increases the speed of the FF compared to the previous ones.




(a)




(b)

Figure 4: Structure of (a) DFFF, (b) clock-tree.

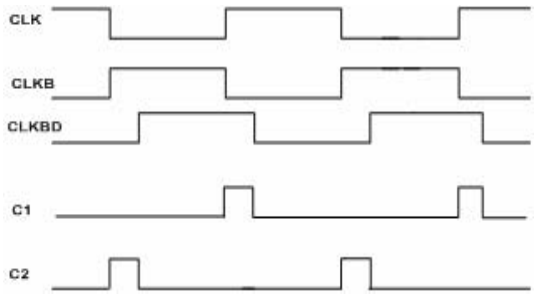



Figure 5: The timing diagrams of C1 and C2 in DFFF.

Also, it should be noted that the charging of node X is needed when DB is high and discharging of node X occurs when it is low. As another advantage of this logic is that the node X is discharged through only one transistor (MN1 or MN2) that again leads to the reduction of the DFFF delay. Finally, we should mention that the node Q also can be charged through MN3 and MN5 at the rising edge of clock and MN4 and MN5 at the falling edge of the clock whenever needed (*i.e.*, when D is high). Contrary to previous logic, there is no unnecessary transition in X and, hence, no extra power consumption occurs. Choosing MP1 as a small pull-up device, a weak fighting might exist during an input state change in two successive clock cycles.

The operation of the logic at the falling edge of the clock is similar to its operation at the rising edge except that C2 is high rather than C1 (Fig. 5) and MN2 and MN4 play the role of MN1 and MN3, respectively. The waveform of C1, C2, and the output using HSPICE is depicted in Figure 6.

**3. SUBTHRESHOLD CURRENT**

Subthreshold or weak inversion conduction current between the source and drain in an MOS transistor occurs when the gate voltage is below $V_{th}$ [4]. Weak inversion typically dominates modern device off-state leakage due to the low-$V_{th}$ [4]. The weak inversion current can be expressed as [10]

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times \exp[\frac{(V_g - V_{th})}{m v_T}]$$

$$\times (1 - \exp[\frac{-V_{DS}}{v_T}]) \qquad (1)$$

where

$$m = 1 + \frac{3t_{ox}}{W_{dm}} \qquad (2)$$

where $V_{th}$ is the threshold voltage, and $v_T = KT/q$ is the thermal voltage, $C_{ox}$ is the gate oxide capacitance, $\mu_0$ is the zero bias mobility; and $m$ is the subthreshold swing coefficient (also called body effect coefficient). $W_{dm}$ is the maximum depletion layer width, and $t_{ox}$ is the gate oxide thickness [4]. As it is obvious from (1), if $V_{DS} = 0$, then subthreshold current will be zero.

Based on the above discussion, here we present a brief description of the previous flip-flop structures. In HLFF (Fig. 1) and SDFF (Fig. 2), when the node X is high, a voltage equal to $V_{dd}$ is applied across the first branch in the pull down network (consisting of MN1, MN3 and MN5). On the other hand, when the node $X$ is low then $Q$ (output) will be high and output pull down tree sustains a voltage equal to $V_{dd}$. This high $V_{DS}$ voltage drop causes large leakage currents and hence high leakage powers. The situation is even worse in the case of SDFF where this voltage exists across two transistors compared to the case of HLFF where three transistors exist in the output pull down network. Let's explain the situation in LSDFF (Fig. 3). Suppose that D is low, and then the voltage of node X2 as well as $V_{DS}$ of MN1 is equal to $V_{dd}$. In the case that D is high, the $V_{DS}$ of MN2 will be equal to $V_{dd}$ and, hence, only one transistor has a high $V_{DS}$ drop. As a result of this, the leakage current will be higher than the previous flip-flops. With the same argument, it can be observed that LSDFF would have more leakage current due to low-$V_{th}$ transistors in its clock tree.

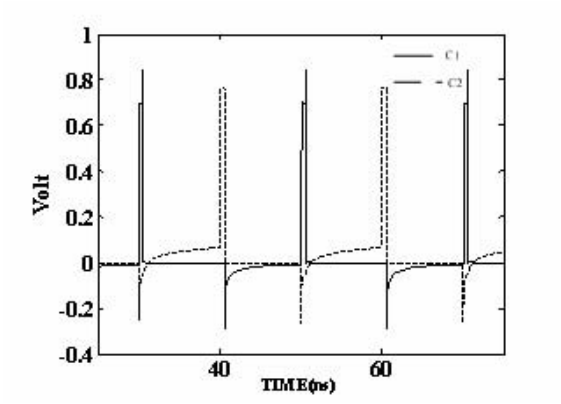
The subthreshold current in DFFF is very low which is due to the fact that the $V_{DS}$ of each transistor in the pull-down network will be zero. Assuming D is high (DB is low), node X will be high, and, hence, both the drain and the source of MN1 and MN2 have high logic values leading to an approximately zero $V_{DS}$ for these transistors. When D as well as Q is high, the voltage drop across the output pull-down tree will be approximately zero too. Compared to other flip flops, subthreshold current in DMHLFF is very low. These very low $V_{DS}$ minimize the subthreshold leakage current of the flip-flop.

## 4. SIMULATION RESULTS

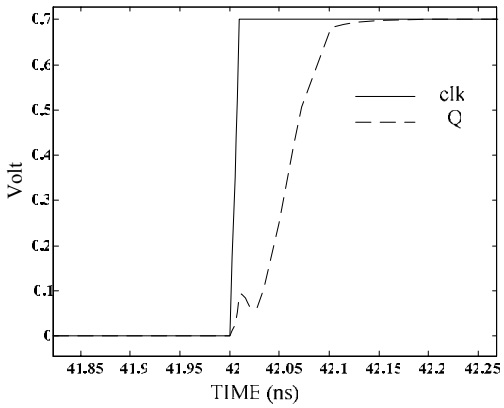
To evaluate the performance of the proposed flip-flop compared to other flip-flop circuits, all the discussed flip-flops have been simulated in a 70 *nm* CMOS process [Ref]. The HSPICE simulation results for $V_{dd}$ = 0.7V are given in Table 1. The clock frequencies were 100 and 50 MHz for single-edge and double-edge triggered FF's, respectively. The load capacitance for flip-flops was assumed to be 10 fF. As is observed from the table, DFFF has lower power consumption, delay, and area (transistor count) compared to other flip-flop structures. The simulation result shows that the power-delay product of DFFF is 73% better than LSDFF. These improvements are 82% and 83% compared to SDFF and HLFF, respectively. The leakage powers of different flip-flops are given in Table 2 which shows the smallest leakage for DFFF as was expected.

## 5. SUMMARY AND CONCLUSION

In this work, we proposed a new Double edge triggered Feedback Flip-flop (DFFF) which had a better performance compared to previous logic. By a proper circuit design, unnecessary internal node transitions were avoided in this logic. Since the flip-flop is double-edge triggered, this logic may work with a lower clock frequency compared to single edge triggered flip-flops. These two reduced the power consumption of the flip-flop compared to other flip-flops. Furthermore reducing the number of transistor in the stack for both the internal and the output nodes and increasing the number of charging and discharging paths decreased the delay of the logic. The simulation results indicate that the improvement in the performance of DFFF is approximately between 70% and 84% compared to previous works.




(a)




(b)

Figure 6: The waveform of (a) the controlling signal (*i.e.*, C1 and C2) (b) the output of DFFF.

## REFERENCES

[1] M. Hamada, T. Terazawa, T. Higashi, S. Kitabayashi, S. Mita, Y. Watanabe, M. Ashino, and H. Hara, T. Kuroda, "Flip-Flop Selection Technique for Power-Delay Trade-off," in IEEE Int. Solid-State Circuits Conf., pp. 270–271, Feb. 1999.

[2] B. Nicolick, V. Stojanovic, V. G. Oklobdzija, W. Jia, J. chiu, M. Leung . "Sense Amplifier-Based Flip-Flop" in IEEE Int. Solid-State Circuits Conf. , pp. 282-283, Feb. 1999.

[3] B. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-Capture Flip-Flop Technique for Statistical Power Reduction," in IEEE Int. Solid-State Circuits Conf., pp. 290–291, Feb. 2000.

[4] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," in

*Proceedings of IEEE*, vol. 91, issue 2, pp. 305 – 327, Feb. 2003.

[5] N. Nedovic, V.G. Oklobdzija, "Hybrid latch flip-flop with improved power efficiency," in *Proceedings of IEEE Symp. on Integrated Circuits and Systems Design*, pp. 211-215, Sep. 2000.

[6] E. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements," in *Proceedings of IEEE Int. Solid-State Circuits Conf.*, Feb. 1996.

[7] F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 108–109, June 1998.

[8] H. Kojima, S. Tanaka, and K. Sasaki, "Half-Swing Clocking Scheme for 75% Power Saving in Clocking Circuitry," *IEEE J. Solid-State Circuits*, vol. 30, pp. 432–435, Apr. 1995.

[9] C. Kim, S.-M. (Steve) Kang, "A Low-Swing Clock Double-Edge Triggered Flip-Flop" *IEEE J. of Solid-State Circuits*, vol. 37, no. 5, May 2002.

[10] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, New York, Cambridge Univ. Press, 1998, ch. 3, pp. 120–128.

[11] V. Stojanovic and V.G. Oklobdzija, "Comparative Analysis of Master–Slave Latches and Flip-Flops for High-Performance and Low-Power Systems," *IEEE J. Solid-State Circuits*, vol. 34, pp. 536–548, Apr. 1999.

Table 1: Comparing various structures of DFF

| Style | No. of Tr. | No. of Clked Tr. | Clk-Q (ps) | Power (μW) | P.D. (fj) | Improvement |
|---|---|---|---|---|---|---|
| SDFF | 23 | 5 | 132 | 2.12 | 0.280 | 82% |
| HLFF | 20 | 4 | 145 | 2.06 | 0.299 | 83% |
| LSDFF | 28 | 3 | 106 | 1.8 | 0.191 | 73% |
| DFFF | 21 | 3 | 59 | 0.88 | 0.051 | - |

Table 2: Comparison between the leakage powers of different flip-flops.

| Leakage Power (nW) | SDFF | HLFF | LSDFF | DFFF |
|---|---|---|---|---|
| | 86 | 49 | 82 | 27 |