Double Flying Capacitor Multicell Converter Based on Modified Phase-Shifted Pulsewidth Modulation

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***Abstract*—Multilevel converters are very interesting alternatives for medium and high-power applications. The main reason is the increase in the number of output voltage levels and its apparent frequency. This paper presents a new configuration of flying capacitor multicell (FCM) converter. The main advantages of the proposed converter, in comparison with FCM and stacked multicell converters, are doubling the rms and the number of output voltage levels, improving the output voltage frequency spectrum, and canceling the midpoint of dc source. This progress is achieved by adding only two low-frequency switches to the conventional configuration of FCM converter while the number of high-frequency switches and capacitors, voltage ratings of capacitors and switches, and the number of high-frequency switchings during a full cycle are kept constant. This converter is controlled by a modified phase-shifted pulsewidth modulation, therefore, the self-balancing property of the flying capacitor converter is maintained in the proposed converter. The circuit is simulated using power systems computer-aided design/electromagnetic transients in DC systems (EMTDC) software and simulation results are presented to validate the effectiveness and advantages of the proposed configuration as well as its control strategy. Additionally, measurements taken from an experimental setup are presented in order to study the practical configuration.**

***Index Terms*—Cascaded multicell (CM) converter, flying capacitor multicell (FCM) converter, natural balance, phase-shifted pulsewidth modulation (PSPWM), stacked multicell (SM) converter.**

I. Introduction

MULTILEVEL converters have been continuously developed in recent years due to the necessity of increase in power level of industrial applications, especially high-power applications, such as high-power ac motor drives, active power filters, reactive power compensation, and FACTS devices [1]–[5]. The main reason is the capability of these topologies to handle voltage/power in the range of kilovolts/megawatts due to recent developments in the area of high-power semiconductors [6]–[9].

Multilevel converters include an array of power semiconductors and capacitor voltage sources, which generate output voltage with stepped waveforms. The commutation of the switches permits the addition of the capacitors voltages and generates high voltage at the output, while the power semiconductors must withstand only reduced voltages [8], [10], [11].

The term multilevel starts with the three-level converter introduced by Nabae *et al.* [12]. By increasing the number of levels in the converter, the output voltage has more steps generating a staircase waveform, which has a reduced harmonic distortion [13]. However, a high number of levels increases the control complexity and introduces voltage imbalance problems [10].

The neutral point clamped (NPC) converter, presented in the early 1980s [12], is now a standard topology in industry on its three-level version. However, for a high number of levels, this topology presents some problems, mainly with the clamping diodes and the balance of the dc-link capacitors. An alternative for the NPC converter are the multicell topologies. Different cells and ways to interconnect them generate many topologies, which the most important ones, described in Section II, are the cascaded multicell (CM) and the flying capacitor multicell (FCM) with its subtopology stacked multicell (SM) converters [11], [14].

The FCM converter [15] and [16], and its derivative, the SM converter [17]–[19], have many attractive properties for medium voltage applications, including, in particular, the advantage of transformerless operation and the ability to naturally maintain the flying capacitors voltages at their target operating levels [15], [20]. This important property is called natural balancing and allows the construction of such converters with a large number of voltage levels [21]. Natural self-balancing of the flying capacitors voltages occurs without any feedback control. A necessary self-balancing condition is that the average flying capacitors currents must be zero. As a result, each cell must be controlled with the same duty cycle and a regular phase-shifted progression along the cells. Generally, an output *RLC* filter (balance booster circuit), tuned to the switching frequency or multiple of that, is suggested to be connected across the load in order to accelerate this self-balancing process in the transient states and to reduce the effect of control signal faults [9], [22].

The FCM converter uses a series connection of "cells" comprising a flying capacitor and its associated complimentary switch pair and produces a switched voltage that is the sum of the individual cell states. The SM converter stacks two FCM converters together with the upper stack switching only when a positive output is required and the lower stack switching only when a negative output is required [21].

The remainder of this paper is organized as follows. Section II provides a brief summary of multicell converter

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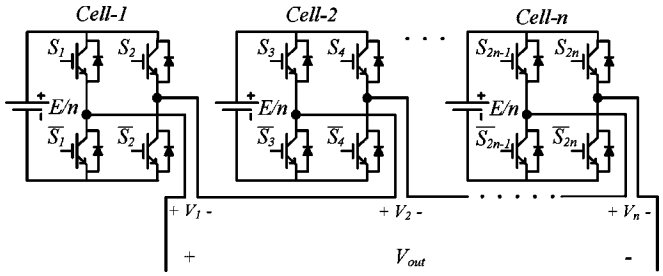

Fig. 1. $2n + 1$ level CM converter with maximum output voltage value of *E*.

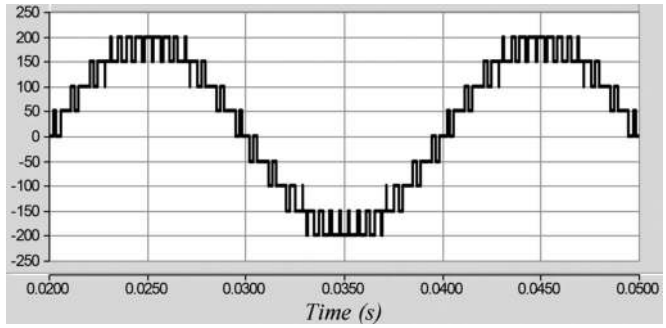

Fig. 2. Output voltage of a four-cell-nine-level CM converter (in volt).

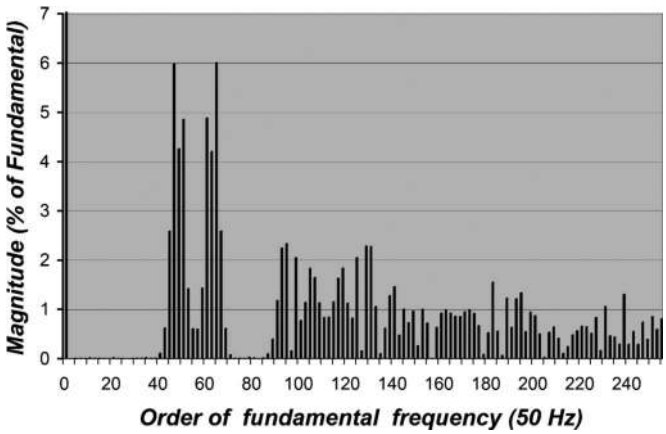

Fig. 3. Output voltage frequency spectrum of a four-cell-nine-level CM converter.

circuit topologies, their properties, and output voltages. In Section III, the new configuration based on the FCM converter and its control strategy based on the modified phase-shifted pulsewidth modulation (PSPWM) technique are proposed. The proposed configuration, called double FCM (DFCM) converter, doubles output voltage levels and rms of output voltage in comparison with FCM and SM converters; this progress is achieved by applying only two additional low-frequency switches, which work with low-switching frequency, and generally, are switched twice during a full cycle of the fundamental output voltage.

Simulation and experimental results are presented in Sections IV and V, respectively, for single-phase four-cell-nine-level proposed DFCM converter to validate the effectiveness and advantages of the proposed configuration and its control strategy.

II. Multicell Converters

A. CM Converter

The CM converter, as shown in Fig. 1, was introduced in the early 1990s [23], [24]. This topology is based on the series connection of units known as cells with three-level output voltage. Each cell is a structure based on an isolated voltage source, therefore, a bulky and complex multisecondary input transformer is required when only one dc voltage source is available. Therefore, it causes increase in the cost and size of the converter. As the cells are connected in series, a maximum of $2n + 1$ output voltage levels is obtained and the total output voltage, corresponding to the sum of each cell output voltage, is as follows:

$$v_{\text{out}} = \sum_{i=1}^{n} v_i \tag{1}$$

where *n* is the number of cells connected in series.

An additional advantage of this topology is that when an internal fault is detected and the faulty cell is identified, it can be easily isolated through an external switch and replaced by a new operative cell without turning OFF the converter. However, while the replacement is done, the maximum output voltage in the faulty leg is reduced to

$$v_f = v_{\text{out}} \left(1 - \frac{f}{n}\right) \tag{2}$$

where *f* is the number of faulty cells.

As the four-cell-nine-level CM converter is controlled by PSPWM ($f_{\text{switching}} = 700$ Hz) and operated with a modulation index equal to 0.8 ($M = 0.8$), the output voltage with total harmonic distortion (THD) of 15% as well as its frequency spectrum are illustrated in Figs. 2 and 3, respectively.

The PSPWM, which is used in CM, FCM, SM, and proposed DFCM converters is a regular PSPWM, where the phase shift between the carriers of each cell is as follows:

$$\varphi = \frac{2\pi}{n} \tag{3}$$

where *n* is number of cells.

B. FCM Converter

A 2*n*-cell FCM converter, as shown in Fig. 4, is composed of 4*n* switches forming 2*n*-commutation cells controlled with equal duty cycles and phase shifted of π/n and $2n - 1$ flying capacitors with the same capacitance. As a result, the electrical stresses on each switch are reduced and more equally distributed as each switch must withstand E/n volts [25]–[27].

The output voltage of 2*n*-cell FCM converter has $2n + 1$ level and its frequency spectrum has the harmonics around the $(2nkf_{\text{switching}})$th harmonic, where *k* and $f_{\text{switching}}$ are the integer number and the switching frequency, respectively. All capacitors see similar current waveforms and have the same capacitance to obtain the same voltage ripple, but their dc voltage ratings are different and equal to $E/n, 2E/n, \ldots, (2n-1)E/n$,

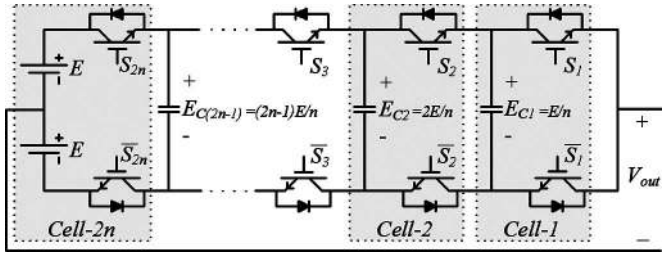

Fig. 4. $2n + 1$ level FCM converter with maximum output voltage value of *E*.

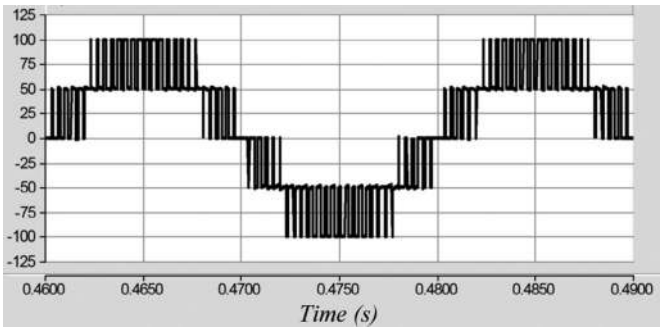

Fig. 5. Output voltage of a four-cell-five-level FCM converter (in volt).

therefore, the energy stored in the capacitor *k* is as follows [26]:

$$U_K = \frac{1}{2}C\left(\frac{KE}{n}\right)^2. \tag{4}$$

Main advantages of a FCM converter over a CM converter are that the FCM converter does not require a complex input transformer and in the case of internal fault of one cell, the maximum output voltage remains constant, but the number of levels decreases to as follows:

$$L_f = L - f \tag{5}$$

where *f* is the number of faulty cells.

The output voltage of a four-cell-five-level FCM converter with THD of 36%, its frequency spectrum and its internal flying capacitors voltages are shown in Figs. 5–7, respectively, while the converter is controlled by PSPWM ($f_{\text{switching}} = 700$ Hz) and operated with a modulation index equal to 0.8 ($M = 0.8$). Fig. 7(a) depicts the internal flying capacitors voltages for the case in which the converter load is resistive and no output *RLC* filter is applied. Fig. 7(b) is for the case in which the output load is resistive–inductive, therefore, an output *RLC* filter is needed and applied. This filter, which consists of a resistance, inductance, and a capacitance in series connection, accelerates the self-balancing process and is connected in parallel with the load. The output *RLC* filter is tuned to the switching frequency as follows:

$$\sqrt{LC} = \frac{1}{2\pi f_{\text{SW}}} \tag{6}$$

where f_{SW} is the switching frequency, *L* and *C* are inductance and capacitance of the output *RLC* filter, respectively.

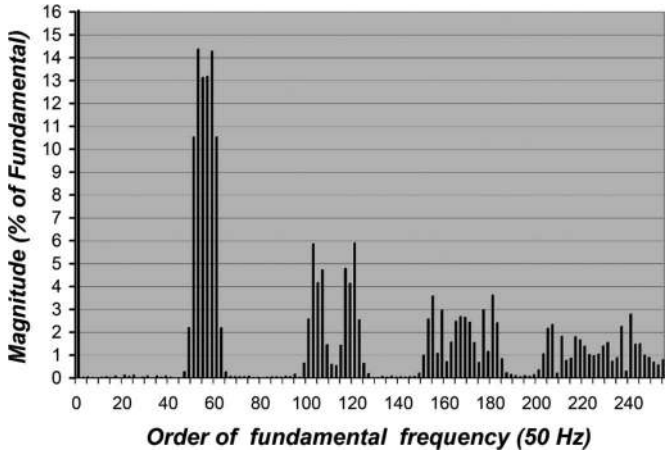

Fig. 6. Output voltage frequency spectrum of a four-cell-five-level FCM converter.

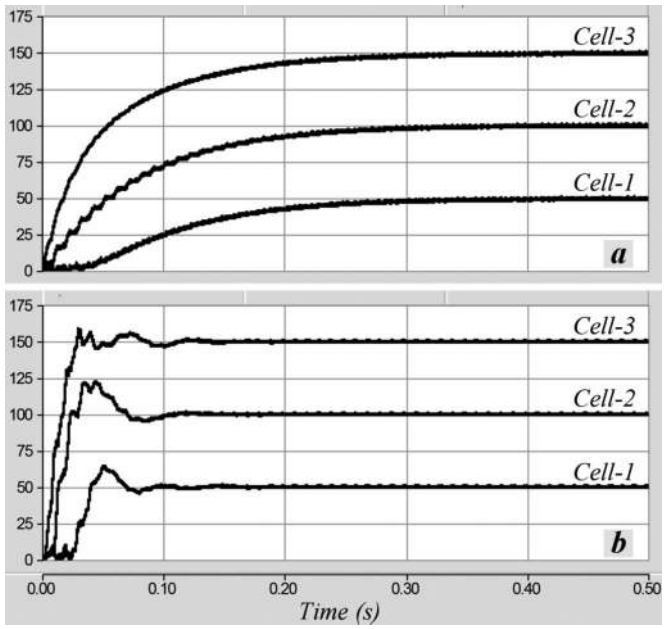

Fig. 7. Internal flying capacitors voltages of a four-cell-five-level FCM converter (in volt). (a) Resistive load without output *RLC* filter. (b) Resistive–inductive load with output *RLC* filter.

C. SM Converter

An alternative topology based on the FCM converter is the SM converter; this structure uses a $m \times n$ cells array to increase the number of output voltage levels. A $2 \times n$ SM converter is shown in Fig. 8. The main advantages of this configuration are that the number of combinations to obtain a desired voltage level is increased (redundancy), and the voltage ratings of capacitors and stored energy in the flying capacitors as well as the semiconductor losses are reduced. However, it requires the same number of capacitors and semiconductors in comparison with the equivalent FCM converter for the same number of output voltage levels [28].

The output voltage of a four-cell-five-level SM converter with THD of 37% and its frequency spectrum as well as its

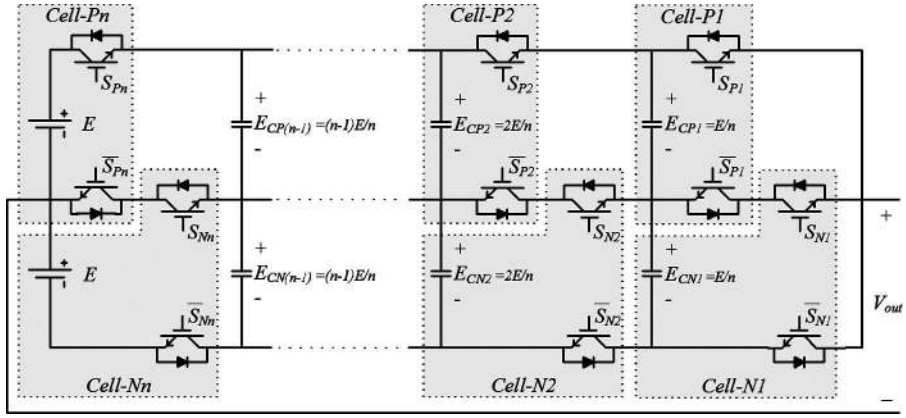

Fig. 8. $2n + 1$ level SM converter with maximum output voltage value of E.

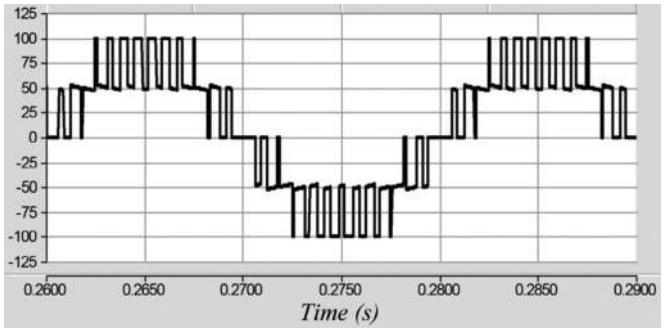

Fig. 9. Output voltage of a four-cell-five-level SM converter (in volt).

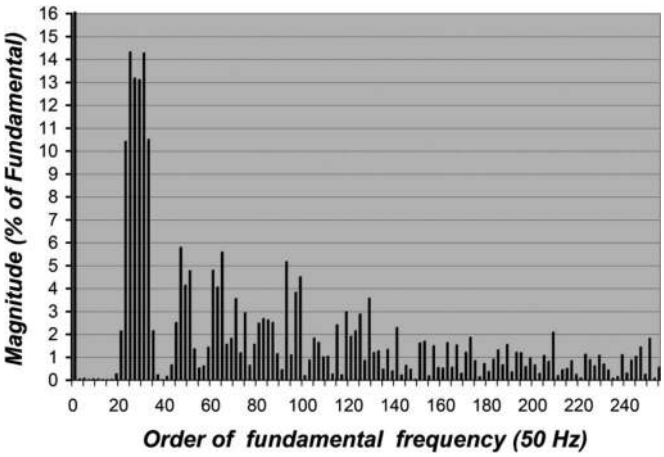

Fig. 10. Output voltage frequency spectrum of a four-cell-five-level SM converter.

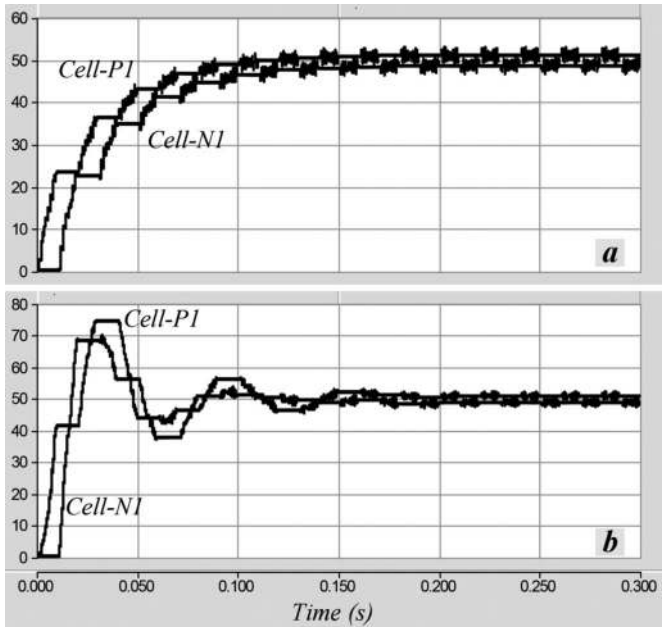

Fig. 11. Internal flying capacitors voltages of a four-cell-five-level SM converter (in volt). (a) Resistive load without output *RLC* filter. (b) Resistive–inductive load with output *RLC* filter.

internal flying capacitors voltages are shown in Figs. 9–11, respectively, while the converter is controlled by PSPWM ($f_{\text{switching}} = 700$ Hz) and operated with a modulation index equal to 0.8 ($M = 0.8$). Fig. 11(a) depicts the internal flying capacitors voltages for the case in which the converter load is resistive and no output *RLC* filter is applied. Fig. 11(b) is for the case in which the output load is resistive–inductive, therefore, an output *RLC* filter is needed and applied.

III. Proposed DFCM Converter

A. Converter Description

The conventional four-cell-five-level FCM converter, its control strategy based on the PSPWM and the output voltage is shown in Fig. 12. As shown in Fig. 13, two low-frequency switches $(J, \overline{J})$ are added to the conventional configuration of FCM converter and the new four-cell-nine-level converter, called DFCM converter, is proposed. Two additional switches work with low-switching frequency, and generally, are switched twice during a full cycle of the fundamental output voltage, while the switch J is ON for negative output voltage and the switch $\overline{J}$ is ON for positive output voltage. The proposed configuration, its control strategy based on the modified PSPWM and its output voltage is shown in Fig. 13 (see Table I for the

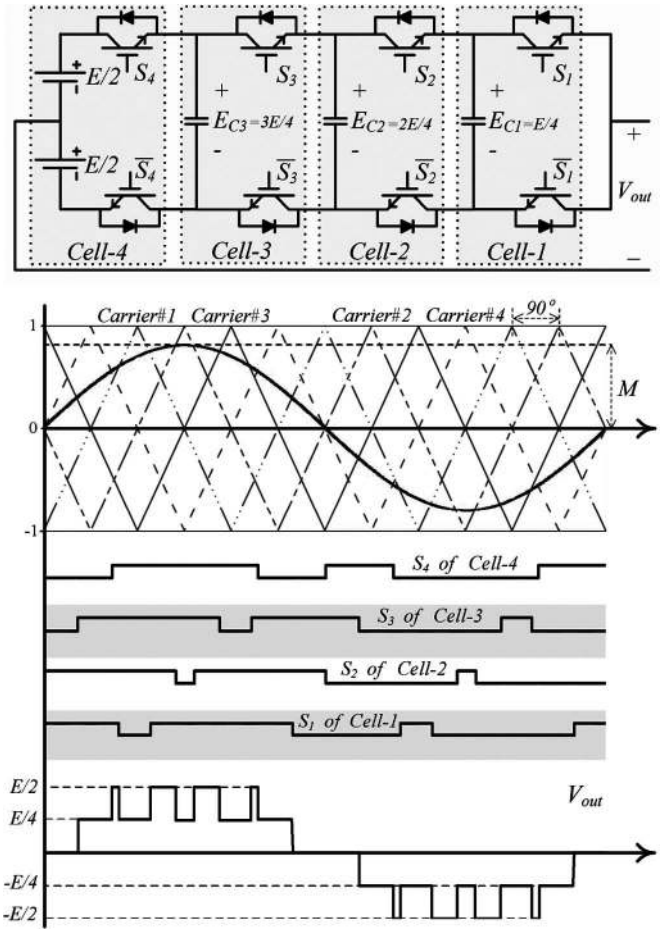

Fig. 12. Four-cell-five-level FCM converter's configuration, control strategy, and output voltage.

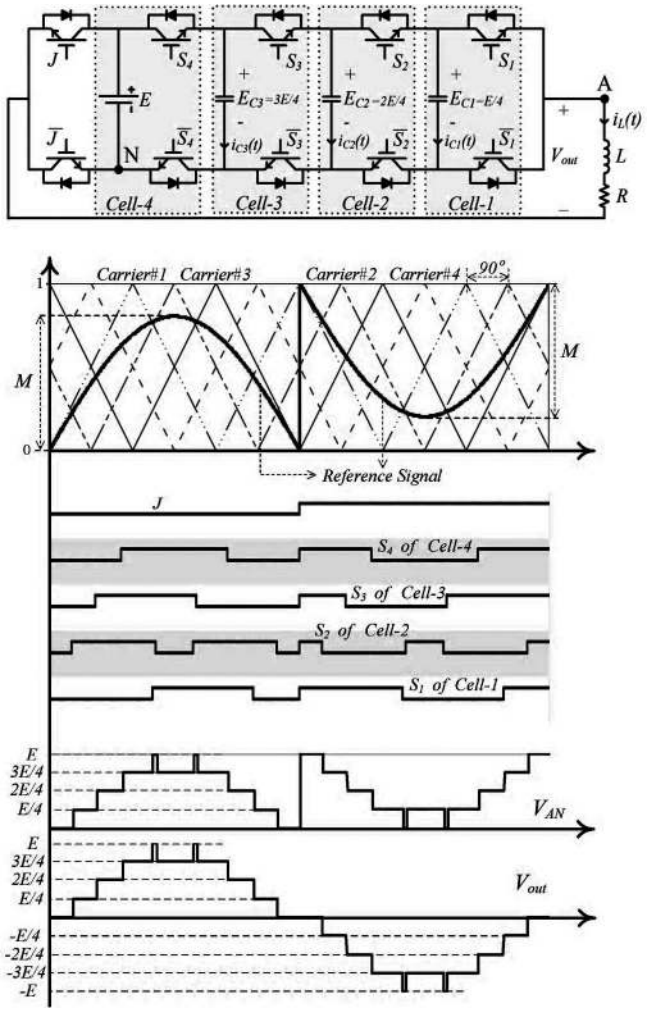

Fig. 13. Four-cell-nine-level proposed DFCM converter's configuration, control strategy, and output voltage.

output voltage levels and switching states of four-cell-nine-level DFCM converter).

In the conventional configuration of FCM converter, as shown in Fig. 12, maximum values of positive and negative peaks of output voltage are only half of the dc source voltage, i.e., $\pm E/2$, while in the proposed DFCM converter, applying the switches J and $\overline{J}$, makes it possible to obtain full value of the dc source voltage, i.e., $\pm E$ for positive and negative peaks of output voltage. As shown in Fig. 13, this achievement causes to double the rms value of output voltage and the number of output voltage levels. The effect of switch J is a negative shift of the voltage V_{AN}, equal to $-E$, in the second half cycle to form the output voltage $V_{\rm out}$. As a result, the reference signal must be shifted one positive unit in the second half cycle to offset negative shift of the voltage V_{AN} made by switch J, as shown in Fig. 13.

The main advantages of the proposed converter, in comparison with FCM and SM converters, are doubling the rms of output voltage and the number of output voltage levels and canceling the midpoint of dc source. This progress is achieved by adding only two low-frequency switches to the conventional configuration of FCM converter, while the number of high-frequency switches and capacitors, voltage ratings of capacitors and switches and the number of high-frequency switchings during a full cycle are kept constant. Also, the frequency spectrum of output voltage is improved and its THD is reduced significantly because of doubling the number of output voltage levels.

Different types of conventional multicell converters, i.e., CM, FCM, and SM converter, as well as the proposed DFCM converter for producing the identical output voltage with equal number of levels ($2n+1$ level) and equal maximum value of output voltage (E) are displayed in Figs. 1, 4, 8, and 14, respectively. Also, comparison between the conventional multicell converters and the proposed converter is displayed in Table II for the identical output voltage with equal number of levels ($2n+1$ level) and equal maximum value of output voltage (E).

As shown in Figs. 1, 4, 8, and 14 and Table II, the progress of doubling the rms of output voltage and the number of output voltage levels in the proposed DFCM converter makes it possible to decrease the number of flying capacitors, high-frequency switches and input dc voltage sources by 50% in comparison with FCM and SM converters. Although the number of high-frequency switches is decreased by 50% in the proposed DFCM converter in comparison with CM, FCM, and SM converters,

TABLE I
SWITCHING STATES OF FOUR-CELL-NINE-LEVEL PROPOSED DFCM CONVERTER

Output Voltage Level	State: J	State: (S_4, S_3, S_2, S_1)	No. of states
$+E$	0	(1,1,1,1)	1
$+\frac{3}{4}E$	0	(1,1,1,0) , (1,1,0,1) , (1,0,1,1) , (0,1,1,1)	4
$+\frac{2}{4}E$	0	(1,1,0,0) , (1,0,0,1) , (0,0,1,1) , (0,1,1,0)	4
$+\frac{1}{4}E$	0	(1,0,0,0) , (0,1,0,0) , (0,0,1,0) , (0,0,0,1)	4
0	0	(0 , 0 , 0 , 0)	2
	1	(1 , 1 , 1 , 1)	
$-\frac{1}{4}E$	1	(0,1,1,1) , (1,0,1,1) , (1,1,0,1) , (1,1,1,0)	4
$-\frac{2}{4}E$	1	(1,1,0,0) , (1,0,0,1) , (0,0,1,1) , (0,1,1,0)	4
$-\frac{3}{4}E$	1	(0,0,0,1) , (0,0,1,0) , (0,1,0,0) , (1,0,0,0)	4
$-E$	1	(0,0,0,0)	1

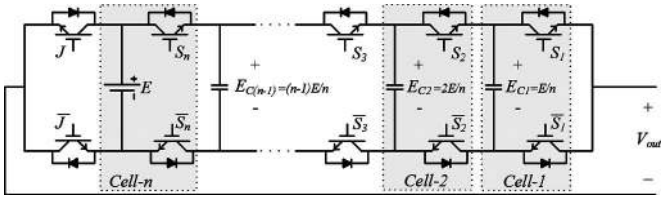

Fig. 14. $2n+1$ level proposed DFCM converter with maximum output voltage value of E.

the voltage rating of switches is not changed for producing the identical output voltage, as shown in Figs. 1, 4, 8, and 14 and Table II. Also, because of producing the identical output voltage, the load current of equal load is same for all type of mentioned converters. As a result, the power rating of all high-frequency switches is equal in all type of mentioned converters. However, the power rating of two added low-frequency switches is not equal to high-frequency switches.

As shown in Fig. 14, only one dc source (or one dc-link capacitor) is needed for the dc link of the proposed converter in the single-phase applications, such as single-phase active power filter, single-phase motor drive, and/or in three-phase applications in which the each single-phase converter must be controlled separately, such as dynamic voltage restorer or unified power quality conditioner. But, two dc sources (or two dc-link capacitors) are required for the conventional configuration of FCM and SM converters in the mentioned applications, as shown in Figs. 4 and 8.

Because of adding two low-frequency switches (J and $\overline{J}$) to conventional FCM converter, the proposed DFCM converter is combination of H-bridge converter and FCM converter, as shown in Fig. 13. Therefore, the application of the proposed multilevel DFCM converter for three-phase load is like multilevel H-bridge converter while it is mandatory to use three multilevel DFCM converters. As a result, the connection of three separate multilevel DFCM converters must be in one of the following methods.

1) Using one dc voltage source (or dc link) jointly for three single-phase proposed DFCM converters and three isolation transformers for each single-phase converter
2) Using three isolated dc voltage sources (or three isolated dc links) for each single-phase proposed DFCM converter without isolation transformer.

Moreover, three-phase application of proposed DFCM converter, such as motor drives, FACTS controller, and other must be in one of the aforementioned methods for connection of three separate multilevel DFCM converters.

B. Instantaneous Model of the Converter in the State-Space Representation

As studied in [3], [7], [25], and [28], the instantaneous model of converter is necessary for estimation of the flying capacitors voltages and active control of the FCM and SM converters. Following, the instantaneous model of the four-cell-nine-level DFCM converter, as shown in Fig. 13, in the state-space representation is obtained

$$\begin{cases} \underline{X}'(t) = A(\underline{S}(t))\underline{X}(t) + B(\underline{S}(t))E \\ Y(t) = C\underline{X}(t) \end{cases} \tag{7}$$

$$\underline{X}(t) = [\, V_{C1}(t) \quad V_{C2}(t) \quad V_{C3}(t) \quad i_L(t) \,]^T \tag{8}$$

$$A(\underline{S}(t)) = \begin{bmatrix} 0 & 0 & 0 & \frac{S_2 - S_1}{C_1} \\ 0 & 0 & 0 & \frac{S_3 - S_2}{C_2} \\ 0 & 0 & 0 & \frac{S_4 - S_3}{C_3} \\ \frac{S_1 - S_2}{L} & \frac{S_2 - S_3}{L} & \frac{S_3 - S_4}{L} & \frac{-R}{L} \end{bmatrix} \tag{9}$$

$$B(\underline{S}(t)) = \begin{bmatrix} 0 & 0 & 0 & \frac{S_4 - J}{L} \end{bmatrix}^T \tag{10}$$

$$C = [\, 0 \quad 0 \quad 0 \quad 1 \,] \tag{11}$$

where E is the input voltage source, $\underline{S} = [\, S_1 \quad S_2 \quad S_3 \quad S_4 \,]$ is the states of switches, $Y(t) = i_L(t)$ is the measured state and corresponds to the load current, and R and L are the resistance and inductance of load, respectively. In the aforementioned instantaneous model, the output *RLC* filter is not existent at the output.

IV. SIMULATION RESULTS

Computer simulation is performed to verify the effectiveness and performance of the proposed converter. The

TABLE II
COMPARISON BETWEEN THE CONVENTIONAL MULTICELL CONVERTERS AND THE PROPOSED CONVERTER FOR THE SAME OUTPUT VOLTAGE

Type of multicell converter	No. of High Frequency Switches	No. of Low Frequency Switches	No. of Cells	No. of Capacitors	No. of DC Sources	Voltage Rating of DC Sources (per unit)	Voltage Rating of High Frequency Switches (per unit)	Power Rating of High Frequency Switches (per unit)	Voltage Rating of Capacitors (per unit)
Cascade Multicell	*4n*	*0*	*n*	*0*	*n*	*1*	*1*	*1*	---
Flying Capacitor Multicell	*4n*	*0*	*2n*	*2n-1*	*2*	*n*	*1*	*1*	From *1* to *2n-1*
Stacked Multicell	*4n*	*0*	*2n*	*2n-2*	*2*	*n*	*1*	*1*	From *1* to *n-1*
Proposed Double Flying Capacitor Multicell	*2n*	*2*	*n*	*n-1*	*1*	*n*	*1*	*1*	From *1* to *n-1*

TABLE III
MAIN PARAMETERS OF SIMULATED CONVENTIONAL AND PROPOSED CONVERTERS

System Parameters	Values
DC voltage (E)	200 V
Internal flying capacitors (C)	1mF
PSPWM carrier frequency ($f_{switching}$) used for CM, FCM, SM and DFCM converters	700 Hz
Fundamental output voltage frequency	50 Hz
Resistive load (R_L)	9 Ω
Resistive-Inductive load (R_L ; L_L)	20Ω ; 50mH
Output RLC filter tuned to f_{SW} (R, L, C)	1Ω ; 9mH ; 5.74μF
Output RLC filter tuned to $2f_{SW}$ (R, L, C)	1Ω ; 2.25mH ; 5.74μF
Number of harmonics for THD calculation	255

four-cell-nine-level DFCM converter, as shown in Fig. 13, is simulated using the power systems computer aided design /EMTDC software. The main parameters used in the simulations are given in Table III.

As the four-cell-nine-level DFCM converter is controlled by PSPWM ($f_{\text{switching}} = 700$ Hz) and operated with a modulation index equal to 0.8 ($M = 0.8$), the output voltage with THD of 15% and load current, as well as the flying capacitors voltages are illustrated in Figs. 15 and 16, respectively. Fig. 16(a) depicts the internal flying capacitors voltages for the case in which the converter load is resistive and no output *RLC* filter is applied. Fig. 16(b) is for the case in which the output load is resistive-inductive, therefore, an output *RLC* filter is needed and applied. In comparison with Figs. 5 and 9, Fig. 15 illustrate that in the proposed DFCM converter both the rms of output voltage and the number of output voltage levels are doubled. As shown in Fig. 16, the flying capacitors can reach to their desired voltages, meaning that the self-balancing property of the FCM converter is maintained in the DFCM converter.

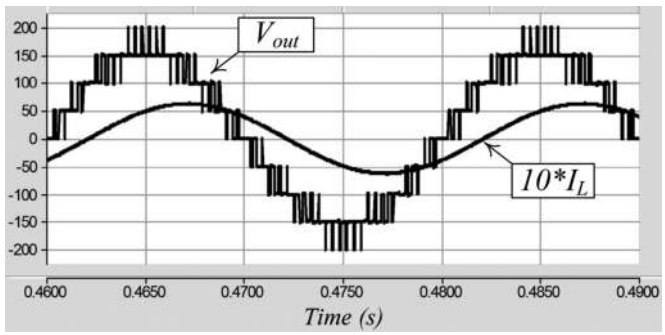

Fig. 15. Four-cell-nine-level DFCM converter output voltage (in volt) and load current (in ampere) with resistive–inductive load.

Fig. 17 shows the output voltage frequency spectrum of the four-cell-nine-level DFCM converter. As shown, the output voltage frequency spectrum of the proposed converter is improved in comparison with Figs. 6 and 10.

V. EXPERIMENTAL RESULTS

To test both the validity and the practicality of the proposed configuration, a prototype four-cell-nine-level proposed DFCM converter was built with ten *IRFP460* 500 V 20 A MOSFETs, as shown in Fig. 18. The flying capacitors values are 1 mF, dc voltage is 100 V, switching frequency is 2.1 kHz, modulation index (*M*) is 0.8 and resistive–inductive (*RL*) load is

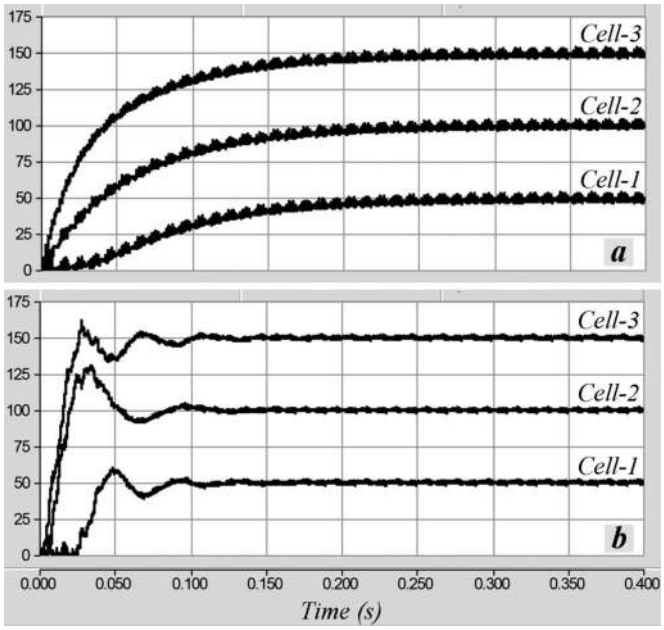

Fig. 16. Internal flying capacitors voltages of a four-cell-nine-level DFCM converter (in volt). (a) Resistive load without output *RLC* filter. (b) Resistive–inductive load with output *RLC* filter.

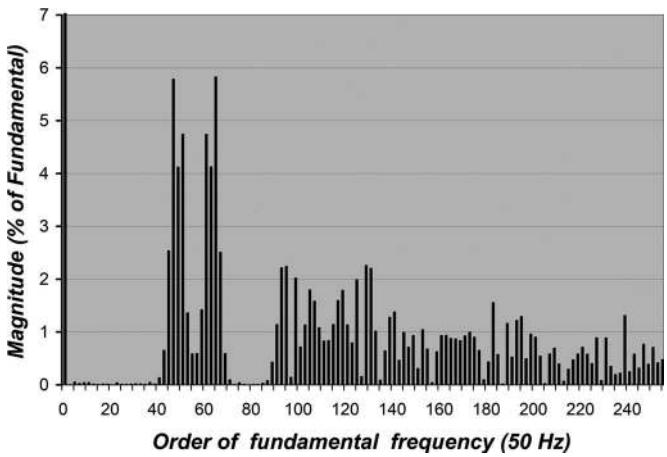

Fig. 17. Output voltage frequency spectrum of a four-cell-nine-level proposed DFCM converter.

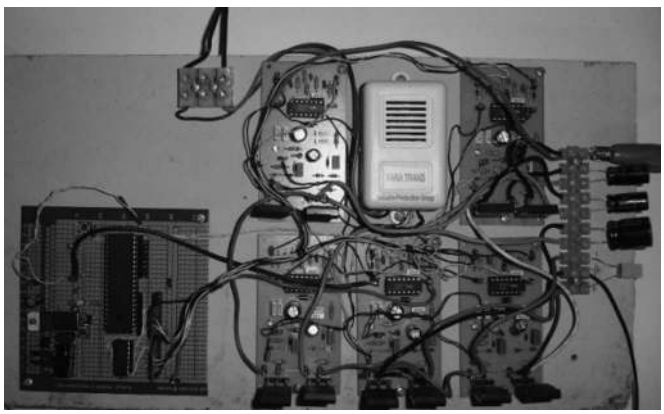

Fig. 18. Hardware implementation of four-cell-nine-level DFCM converter.

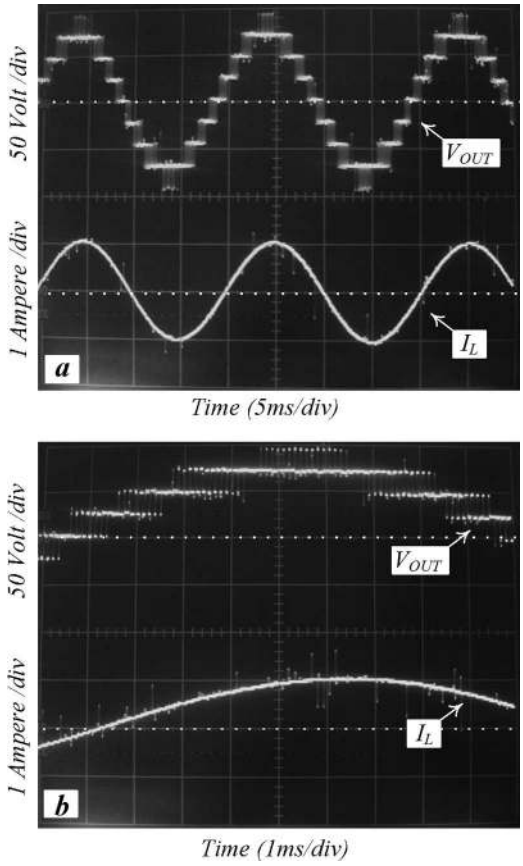

Fig. 19. Experimental results. (a) Four-cell-nine-level DFCM converter output voltage and load current. (b) More detailed of output voltage and load current.

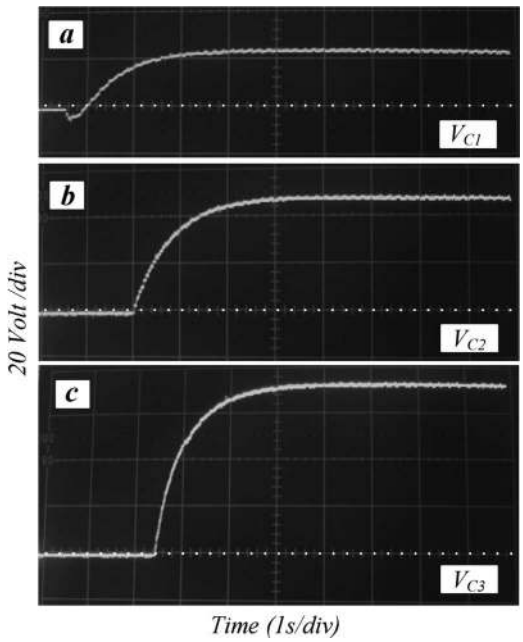

Fig. 20. Experimental results. (a) Voltage of cell-1's flying capacitor (V_{C1}). (b) Voltage of cell-2's flying capacitor (V_{C2}). (c) Voltage of cell-3's flying capacitor (V_{C3}).

75 Ω–90 mH. As the prototype converter was built for the laboratory test, its maximum output power is 500 W.

The measured output voltage and load current as well as the flying capacitors voltages taken from the prototype system without applying output *RLC* filter (balance booster circuit) are illustrated in Figs. 19 and 20, respectively.

The match between simulation and experimental results confirms the advantages and practicality of the proposed DFCM converter and its modified PSPWM control strategy.

VI. Conclusion

Multicell converters are very interesting for high-power/high-voltage applications and considerably improve the output voltage frequency spectrum. This paper has proposed a new configuration of the FCM converter called DFCM converter. In comparison with FCM and SM converters, the main advantages of the proposed converter are doubling the rms of output voltage and the number of output voltage levels and canceling the midpoint of dc source. This progress is achieved by adding only two low-frequency switches to the conventional configuration of the FCM converter, while the number of the high-frequency switches and capacitors, voltage ratings of capacitors and switches, and the number of high-frequency switchings during a full cycle are kept constant. Two additional switches work with low-switching frequency and are generally switched twice during a full cycle of the fundamental output voltage. Also, the frequency spectrum of the output voltage is improved and its THD is reduced significantly because of doubling the number of output voltage levels. As a result, the progress of doubling the rms of output voltage and the number of output voltage levels in the proposed DFCM converter makes it possible to decrease the number of flying capacitors, high-frequency switches, and input dc voltage sources by 50% in comparison with CM, FCM, and SM converters. Moreover, the self-balancing property of the FCM and SM converters, and transformerless operation are maintained in the proposed DFCM converter, which its control strategy is based on the modified PSPWM.

Provided a comparison between the conventional configurations of multicell converters and the proposed DFCM converter, and both simulation and experimental results demonstrate the good performance and feasibility of the proposed converter.

The authors believe that the proposed configuration has a good potential for high-power/high-voltage applications, such as high-power ac motor drives, active power filters, reactive power compensation, dynamic voltage restorer, FACTS devices, and power electronic transformers, while the connection of three separate single-phase DFCM converters must be in one of the mentioned methods.

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