Double-Sided IPEM Cooling Using Miniature Heat Pipes

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***Abstract*—Integrated power electronic module (IPEM) planar interconnect technologies offer opportunities for improved thermal management by allowing thermal access to the upper side of the power devices. In this paper, the feasibility of using miniature heat pipes to achieve effective double-sided cooling is investigated by analyzing the complete thermal circuit associated with the power device. A nominal case was modeled using the ANSYS(tm) finite element software in a single-sided and double-sided configuration. The numerical model predicted that the double-sided configuration would result in a 13 °C reduction in the maximum temperature compared to the single-sided case, for the same 100 W/cm^2 power dissipation in the semiconductor die. This corresponds to a 15% decrease in the maximum temperature rise relative to ambient or a similar increase in allowable power dissipation. Twenty-eight percent of the heat was removed from the upper side of the IPEM in the double-sided case. An additional benefit associated with double-sided cooling was a significant reduction in the spatial temperature gradients along the surface of the IPEM which would translate to lower thermally induced stress and higher reliability. The sensitivity of the numerical predictions to important parameters; including the dielectric conductivity, contact conductance, and heat sink characteristics are numerically investigated. An experimental fixture was fabricated and used to measure a miniature rectangular heat pipe's performance characteristics and the solder joint resistance at its evaporator and condenser interfaces in order to validate the numerical model inputs and demonstrate the required heat pipe capacity. The tested heat pipe was limited to approximately 80 W/cm^2 heat flux in a vertical, evaporator-over-condenser orientation. This limit was not observed in a vertical, gravity-assisted orientation for applied heat flux up to 125 W/cm^2. Equivalent heat pipe resistances of approximately 0.12 and 0.08 K/W were measured in these orientations, respectively. The contact resistance of the indium solder joint was measured and found to be approximately 0.1 cm^2 · K/W.**

***Index Terms*—Heat pipe, integrated power electronic module (IPEM), power electronics, thermal management.**

I. Introduction

A TYPICAL power electronics converter consists of one or more power semiconductor modules mounted on a heat sink. The top-side of the module is devoted to electrical interconnections while the bottom side is dedicated to thermal management. Wire bonds are the most typical technique used to interconnect electrical components within the module. Research and development is presently under way to develop the next generation of power modules known as integrated power electronics modules (IPEMs) [1] that seeks to eliminate these wire bonds in favor of planar interconnections.

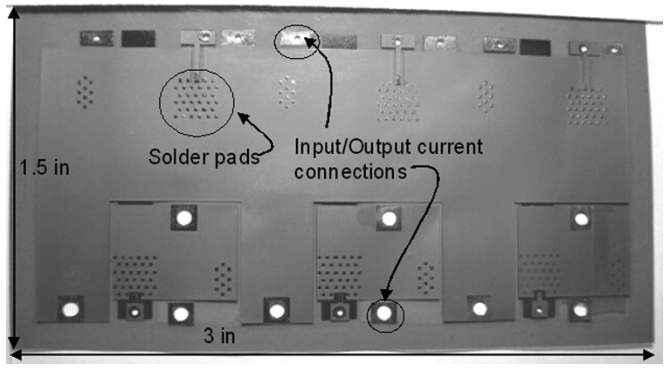

Fig. 1. Flex substrate with solder pads and input/output current connections.

One of the appealing planar interconnect technologies that is presently under investigation uses metallized polyimide films to provide a planar upper surface [2]–[4]. The planar interconnect is achieved using metallized layers deposited on both sides of a flexible polyimide substrate (henceforth referred to as flex). The flex sample shown in Fig. 1 has been fabricated with solder pads to facilitate die attachment and through-holes for the input and output pins. Current or signal carrying paths are laid out in a planar geometry by etching the metallized layers on the polyimide.

This flex technology may allow thermal access to the upper side of the module and therefore enable double-sided cooling of IPEMs. Double-sided cooling of IPEMs has the potential to allow increased chip power dissipation and/or to improve IPEM reliability by lowering the junction operating temperature. Heat pipes have been used in the past to provide double-sided cooling of discrete power semiconductor devices [5], [6] but not in integrated power modules. Despite their cooling potential, heat pipes have not been widely utilized in the electronics industry until the 1990s when they were incorporated into laptop computers [7], [8].

An earlier analysis projected that heat pipes are capable of removing heat fluxes greater than 100 W/cm^2 from a chip surface, making them compatible with expected future IPEM requirements [9]. A numerical optimization of the heat pipe design variables: effective pore radius, wick permeability, porosity, and thickness was performed using the Los Alamos HTPIPE code [10] on a 5-cm-long copper/water heat pipe with an external, axial cross section of 0.785 cm^2. According to this study, the maximum axial heat flux at an operating temperature of 77 °C was predicted to be 419 W/cm^2. This decreased to 330 W/cm^2

Manuscript received August 22, 2003; revised June 8, 2004. This work was supported primarily by the ERC Program of the National Science Foundation under Award EEC-9731677. This work was recommended for publication by Associate Editor D. N. Donahoe upon evaluation of the reviewers' comments.

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Digital Object Identifier 10.1109/TCAPT.2005.848591

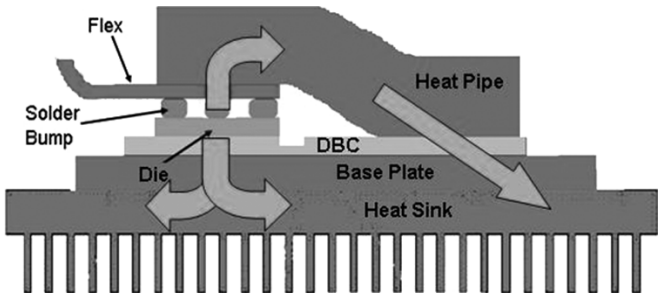


Fig. 2. Double-sided cooling concept using polyimide flex for electrical connections and heat removal from the upper surface of the power device using a heat pipe.

at 97 °C. The numerical analysis was performed with the evaporator and condenser at the same elevation. The code predicted only minor performance degradation in going from a vertical evaporator-over-condenser orientation to a vertical condenser-over-evaporator orientation. An equivalent thermal resistance of 0.0524 K/W was calculated for the heat pipe, assuming an axial heat flux of 100 W/cm^2.

It is of interest to quantify the steady-state thermal improvement that can be achieved with double-sided cooling using an optimized heat pipe mounted on the top surface of a flex substrate above a power die. According to the adopted configuration, the heat pipe transfers the thermal energy to the same heat sink on which the power die is mounted, as shown in Fig. 2. The direct-bond copper (DBC) substrate in this figure provides galvanic insulation between the power semiconductors and the metal heat sink, while the base plate serves as a structural mounting surface for the power devices and a means for spreading the heat. It is assumed that a flex substrate is used for power and signal distribution, and flip-chip solder techniques [11] are used to connect the power die to the flex.

One of the limitations of current air-cooled designs is high temperature—the result of significant thermal impedances associated with the DBC substrate, conductive spreading resistances in the base plate and heat sink, interface resistances, and the convection resistance to the external cooling medium (air is assumed in this paper). In particular, the ceramic alumina (Al_2O_3) layer within the DBC that is required for electrical isolation has an extremely low thermal conductivity. Furthermore, the upper copper layer on the DBC substrate is extremely thin so that very little heat spreading occurs between the chip base and the ceramic layer. A key advantage of double-sided cooling with a heat pipe is that a larger area of DBC can be activated, significantly reducing this very large internal thermal resistance. Furthermore, the activation of a larger DBC area results in better utilization of the base plate and heat sink, reducing the spreading resistance within these components and resulting in a lower chip-to-air thermal impedance.

These system-level effects are subtle and can only be examined by considering the complete thermal network between the heat generation zone and the cooling air. Therefore, this paper investigates the use of a heat pipe within a double-sided cooling configuration for an IPEM and considers the complete thermal impedance path at a nominal set of operating conditions. A comparable single-sided case is also considered in order to quantify the benefits of this thermal management approach.

This paper is divided into four sections. In the first section, a numerical model is described. In the second section, the numerical model is used to quantify the thermal performance improvement that can be achieved using double-sided cooling. A parametric analysis of the effect of the critical package parameters is also reported. The third section describes experimental measurements of the heat pipe thermal performance and the contact resistance values. The final section summarizes the major conclusions and observations in this paper.

II. Numerical Model

The double-sided cooled IPEM concept investigated in this paper is shown in Fig. 2. It features a single power semiconductor die that is electrically connected with a metallized polyimide film (flex) using solder bumps instead of wirebonds. An insulated gate bipolar transistor (IGBT) was selected as the power semiconductor in this example. A heat pipe is used to extract some heat from the top side of the device and transfer it to the DBC substrate. The DBC consists of a core of thermally conductive dielectric material such as alumina or aluminum nitride that is metallized on both sides with copper. The base plate, typically copper, provides a rugged mounting structure and heat spreader. Heat is ultimately dissipated to the environment using the same air-cooled heat sink that is affixed to the bottom side of the base plate. The top side of the die, the emitter for an IGBT, can operate at voltage potentials several hundred volts above the bottom side, the transistor collector. Electrical isolation between the top and bottom side is therefore required and can be achieved with the use of a dielectric either at the evaporator or the condenser end of the heat pipe. In Fig. 2, electrical isolation is achieved at the condenser end by etching the upper metallization layer of the DBC down to the dielectric layer in order to isolate the DBC region that accepts the condenser.

The numerical models described here capture the steady-state, maximum temperatures and spatial temperature gradients within a single die. The main components included in these models are the heat pipe, flip-chip-on-flex interconnections, die, DBC substrate, base plate, heat sink, and the solder joints between the die and DBC and the DBC and base plate. Contact resistances are also included at the base plate/heat sink interface and the heat pipe evaporator and condenser interfaces.

Given the complexity of the heat transfer mechanisms inside the heat pipe and at the heat sink-air interface and the dramatic differences in the physical scale of the materials within the IPEM package, various modeling simplifications were utilized to achieve reasonable solutions given the available computational resources. These simplifications include: 1) an effective convection coefficient applied to the bottom side of the heat sink in order to represent the actual convection coefficient and conduction through the fins; 2) pseudomaterials with anisotropic properties chosen to represent composites of multiple, thin materials; 3) the complex internal structure and fluid flow within the heat pipe modeled using an equivalent solid with a representative, effective thermal conductivity; and 4) the IPEM model split into two separate models based on the geometric scale of

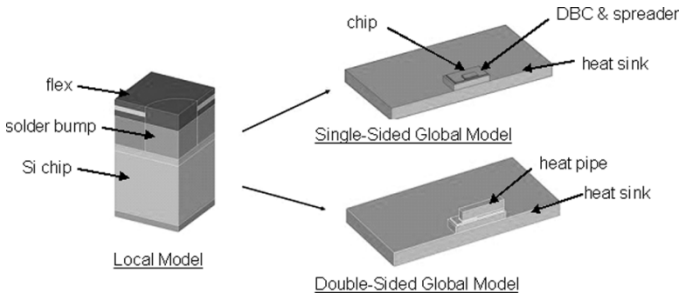


Fig. 3. Multiscale modeling methodology illustrating local model and global models for single- and double-sided cooling configurations.

the features being considered. This last simplification addresses the fact that the die and interconnect geometry has a dramatically different length scale (100 μm) from the balance of the IPEM package (1-cm scale).

When geometric features with widely disparate length scales are modeled together, the smallest features require correspondingly fine meshes. System resources are rapidly strained and computational run times become onerous. In order to avoid this situation, two separate models are generated. The first model, referred to as the local model, captures the small-scale features adjacent to the chip. The local model is used to calculate equivalent thermal resistances for the composite, multidimensional, small-scale geometries between the heat generation zone and the DBC substrate, as well as between the heat generation zone and the evaporator of the heat pipe. These equivalent resistances guided the selection of appropriate equivalent material properties in the global model that capture the larger-scale phenomena associated with conductive spreading within the DBC layer, base plate, and heat sink in the single- and double-sided cooled devices, respectively. Two separate global models were developed in order to evaluate single- and double-sided cooling configurations, respectively. Fig. 3 illustrates these models which are discussed in the subsequent subsections.

A. Local Model

The local model is illustrated in Fig. 4. The model consists (from top to bottom) of a copper-polyimide-copper flex layer with solid, copper vias (i.e., holes in the polyimide flex layer filled with copper), a solder bump with an adjacent air-filled zone, the power device itself, and a solid, solder layer. A quarter-symmetry model of a unit cell of the IPEM core structure is modeled, assuming that a square grid of solder bumps and copper vias (aligned) encompasses the entire top surface of the power device.

Volumetric heat generation was applied to the top 10% of the chip thickness in order to model the expected concentration of power dissipation in the upper layer of the power device [12]. Isothermal boundary conditions were applied to the top and bottom surfaces of the local model. These boundary conditions are arbitrary; both surfaces are assumed to be cooled to the same temperature for the purposes of this local model. The heat transferred through the upper and lower surfaces in conjunction with the maximum junction temperature were determined and used to calculate the effective thermal resistance through the upper IPEM core (between the heat generation zone of the chip and the heat pipe evaporator), and the lower IPEM core (between the heat generation zone of the chip and the DBC surface). These thermal resistance values (rather than the amount of heat passed through the surfaces) are eventually used in the Global Model; the thermal resistance values are not sensitive to the assumed temperature boundary condition. Dimensions and properties used in the local model are listed in Table I.

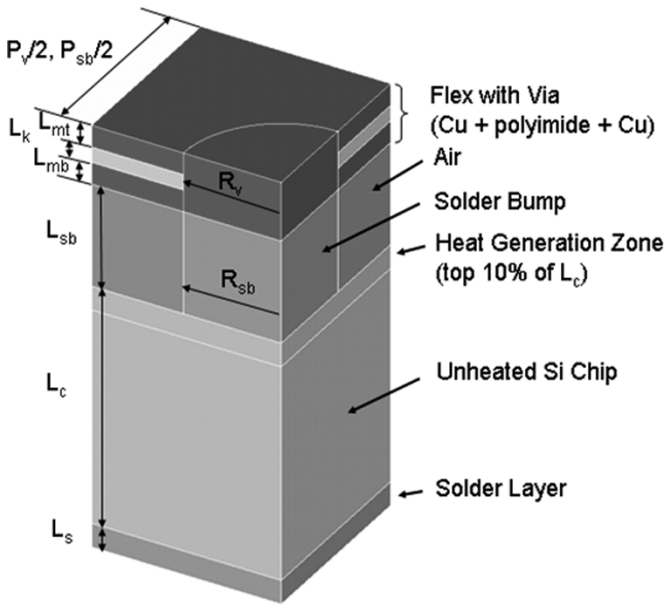


Fig. 4. Local model schematic with key dimensions indicated.

The solid via passing through the flex layer is critical to the double-sided cooling concept. The polyimide has a very low thermal conductivity which forces the heat to spread laterally to the via. Decreasing the pitch, increasing the via cross-sectional area, or increasing the metallization thickness all tend to decrease the upper path resistance and reduce the localized hot spots produced by the solder ball pattern. The via modeled here covers 21% of the unit cell and is laid out on a square pattern with a pitch four times the via radius. The solder balls used to attach the die to the flex are assumed to be aligned with the solid vias.

Underfill, the filling of the gap between the chip and substrate with an appropriate polymer, is often used instead of air around the solder balls to improve device reliability by reducing fatigue wear-out. However, the use of an underfill epoxy will not significantly alter the thermal model results since both air and epoxy have very low thermal conductivity relative to the metallization. Therefore, no underfill was considered in this analysis.

The small-scale thermal behavior predicted by the local model is transferred to the larger-scale global models by selecting appropriate material properties for solids that represent the actual composite structure of the IPEM core, as described in the subsequent section.

B. Global Model

Two global models have been developed, corresponding to single- and double-sided cooling configurations, shown in Fig. 5(a) and (b), respectively. These models are composed of

TABLE I
MODEL INPUTS FOR LOCAL MODEL

Parameter	Nominal Value	Parameter	Nominal Value
copper thermal conductivity	386 W/m-K	flex via radius, R_v	0.323 mm
silicon thermal conductivity	100 W/m-K	flex via pitch, P_v	1.25 mm
solder thermal conductivity	36 W/m-K	flex metalization (top), $L_{m,t}$	0.068 mm
polyimide thermal conductivity	0.16 W/m-K	flex metalization (bottom), L_{mb}	0.068 mm
air thermal conductivity	0.02 W/m-K	polyimide thickness, L_k	0.050 mm
solder ball radius, R_{sb}	0.323 mm	solder layer thickness, L_s	0.075 mm
solder ball height, L_{sb}	0.323 mm	solder ball pitch, P_{sb}	1.25 mm

several volumes that represent different elements in the 3-dimensional thermal circuit, including: the heat sink, base plate and contact resistance, lower DBC copper layer and solder layer, DBC alumina layer, upper DBC copper layer, lower IPEM core, heat generation zone, upper IPEM core, heat pipe, and heat pipe pad (resistance between the heat pipe condenser and the DBC). The last three elements are not present in the single-sided global model. Table II summarizes the inputs to the global models.

The conductivities of the upper and lower IPEM core elements are chosen so that they match the thermal resistances predicted by the local model and therefore approximate the composite structure of the IPEM core. The heat sink fins are not modeled explicitly but the heat sink base material is included. This is necessary since a large part of the internal thermal resistance is related to lateral heat spreading. The fins attached to the base then become essentially one-dimensional thermal elements due to conduction through the fins and convection into the air. An effective heat transfer coefficient that characterizes the thermal resistance from the fin base to the cooling air temperature can be determined from heat sink specifications. A typical value for an aluminum extrusion subjected to a 5 m/s air flow, consistent with a small cooling fan placed very near to the IPEM, is 275 W/m$^2 \cdot$ K. This value was chosen for the nominal condition. The subsequent section describes a comparison between the single- and double-sided cooling configurations; therefore, the details of the cooling system, such as the assumed ambient temperature, are less important than the eventual calculated change in the maximum junction temperature. Also, a parametric analysis of the effective heat transfer coefficient is presented in the subsequent section.

The upper copper and alumina layers of the DBC substrate are extremely important elements in the thermal network and are therefore modeled explicitly in the large-scale models. However, the lower DBC copper layer and solder layer were combined to circumvent meshing difficulties. Orthotropic material properties were chosen to represent the effective thermal resistance of these two materials along each axis. The base plate material, assumed to be copper, and the contact resistance between it and the heat sink were also combined in this fashion. Since no thermal spreading occurs within the contact resistance, its resistance only affects the conductivity along the vertical z-axis.

In the global models, the heat pipe is represented by a solid element with a high thermal conductivity. The mechanisms inside the heat pipe are immaterial as long as the heat pipe is working in its design heat flux and temperature range; that is, its equivalent thermal conductivity is essentially constant when operated under design conditions. The heat pipe dimensions and thermal resistance are consistent with the geometry optimized by Shi *et al.* [9]. The selection of a water filled heat pipe is consistent with standard design practice for this type of application and precludes operation below 0 °C due to freezing limitations. The material properties of the heat pipe pad are chosen so that it represents the thermal resistance of the evaporator-to-flex and condenser-to-DBC contact resistances as well as the heat pipe resistance which is small relative to these other components. Contact resistance is present at the interface between two surfaces due to surface irregularities that decrease the actual surface area available for heat transfer. The nominal contact resistance used in this analysis corresponds to a greased joint under 1–50 psi [13].

III. RESULTS

The steady-state, conduction analysis assumes that the chip dissipates 100 W with 25 °C cooling air flowing through the heat sink. This test condition represents a relatively high but achievable power dissipation value for modern power semiconductor devices. The first subsection presents the results for the nominal operating conditions and geometry listed in Tables I and II. The second subsection presents a parametric analysis of the key model inputs.

A. Results at Nominal Conditions

The temperature distribution in Fig. 6 shows an 82 °C temperature rise in the single-sided configuration with the maximum temperature occurring at the center of the top surface of the die due to symmetry. Although the heat generation is modeled as being evenly distributed across the die, temperature gradients develop in the die and flip-chip-on-flex interconnects due to lateral spreading in the upper copper layer of the DBC. A top view of the die is shown in Fig. 7(a) and shows that this temperature gradient across the die surface can be as much as 18 °C. Underneath the die, at the DBC surface, the temperature gradient is even more pronounced, approximately 24 °C as shown in Fig. 7(b). Spatial gradients can induce stresses that reduce the reliability of the packaged device and therefore should be avoided.

The maximum junction temperature in the double-sided configuration is reduced by 13 °C when compared to the single-sided case given the same ambient temperature and chip dissipation, as shown in Fig. 8. The numerical model predicts that 28% of the heat is removed from the top side of the die through the heat pipe. The presence of the heat pipe near the heat generation zone reduces the spatial temperature gradients along the top surface of the die from 18 °C to 10 °C, as shown

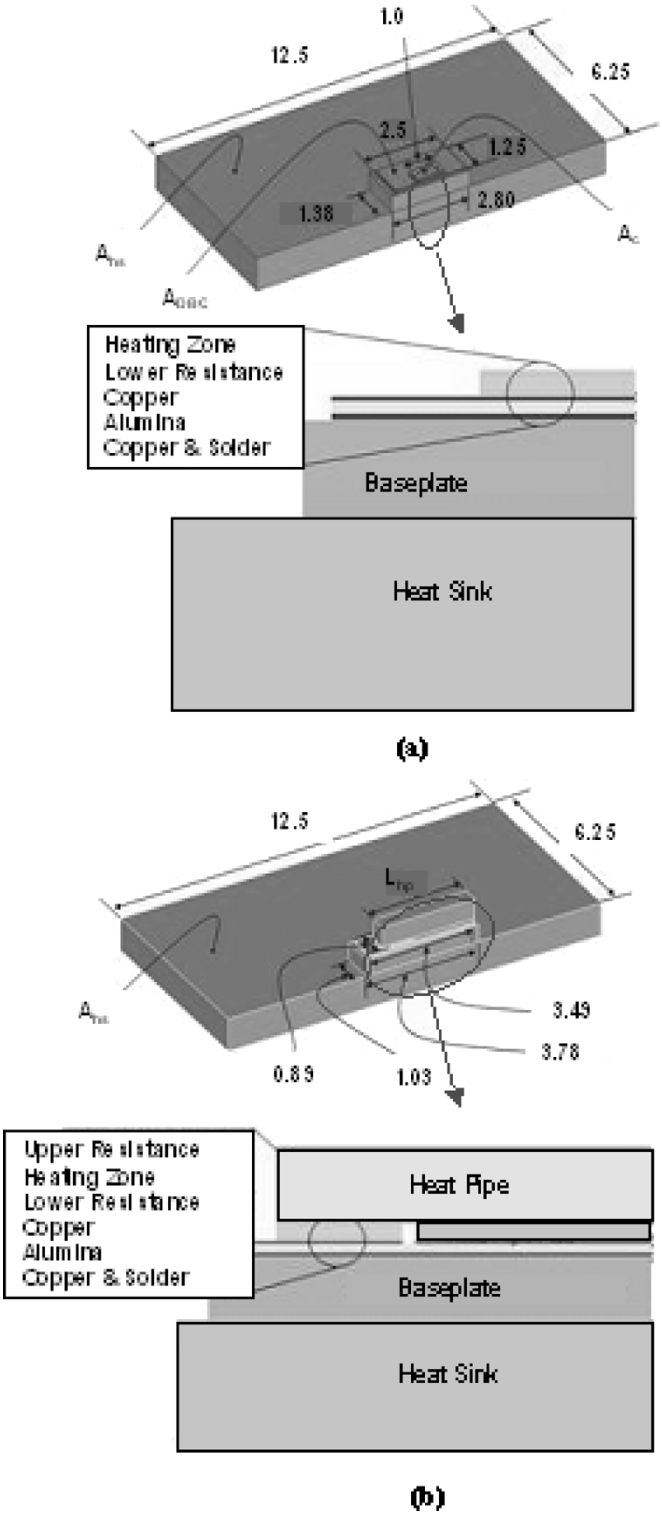


Fig. 5. Global (a) single-sided and (b) double-sided models showing thermal elements and key dimensions (in millimeters).

in Fig. 9(a). Underneath the die, the temperature gradient is reduced from 24 °C to 16 °C, as shown in Fig. 9(b).

Fig. 10 illustrates the maximum temperature predicted on the die surface for the single-and double-sided configurations as a function of the chip power. The use of a miniature heat pipe on the top side of the die translates into a 15% reduction in junction

TABLE II
MODEL INPUTS FOR GLOBAL MODELS

Parameter	Nominal Value, Single-Sided	Nominal Value, Double-Sided
copper thermal conductivity	386 W/m-K	386 W/m-K
silicon thermal conductivity	100 W/m-K	100 W/m-K
solder thermal conductivity	36 W/m-K	36 W/m-K
aluminum thermal conductivity	200 W/m-K	200 W/m-K
Al_2O_3 thermal conductivity	20 W/m-K	20 W/m-K
heat pipe length, L_{hp}	-	3.1 cm
heat pipe condenser area		1x2 cm^2
heat pipe resistance	-	0.052 K/W
contact resistances	-	0.000025 m^2K/W
chip area, A_c	1 cm^2	1 cm^2
chip height, L_c	0.75 mm	0.75 mm
DBC copper layer thickness	0.25 mm	0.25 mm
DBC Al_2O_3 thickness	0.64 mm	0.64 mm
DBC area, A_{DBC}	6.25 cm^2	6.25 cm^2
base plate thickness	5 mm	5 mm
ratio of base plate area to DBC area	1.25:1	1.25:1
heat sink thickness	10 mm	10 mm
heat sink area, A_{hs}	12.5x12.5 cm^2	12.5x12.5 cm^2
effective heat transfer coefficient	275 W/m^2-K	275 W/m^2-K
ambient temperature	25ºC	25ºC
chip power dissipation	100 W	100 W

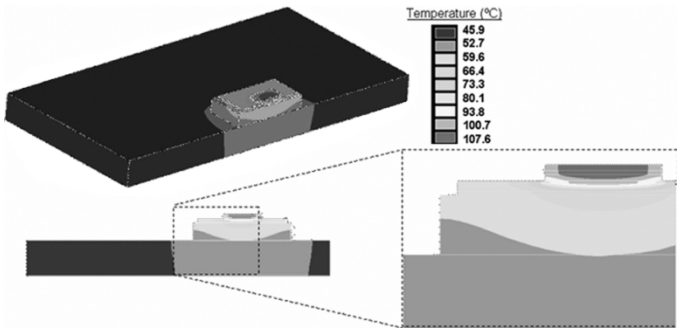


Fig. 6. Temperature distribution predicted by the single-sided global model under nominal conditions.

temperature for a given chip power or an 18% increase in allowable dissipated power for a given maximum allowable junction temperature. Also, the reliability of the IPEM device will be enhanced by the use of a heat pipe due to reduced spatial temperature gradients and therefore lower thermal stresses across solder joints and metallization layers.

B. Parametric Analysis

A parametric analysis was carried out to investigate the effect of the dielectric thermal conductivity, the effective heat transfer coefficient, and the contact resistance on the thermal performance of the system.

Dielectric properties consistent with alumina (Al_2O_3) were used in the nominal conditions because of its widespread use in power electronics modules today. Its low thermal conductivity represents a major thermal impedance, accounting for approximately 20 °C of the 82 °C temperature rise in the single-sided device. Alternative dielectric materials such as aluminum nitride (AlN) or beryllium oxide have higher thermal conductivity; up to 170–230 W/m·K or nearly an order of magnitude greater than alumina. These materials tend to have higher thermal expansion coefficients and/or toxicity concerns that have deterred widespread use [14]. Fig. 11 illustrates the maximum junction temperature as a function of the dielectric thermal conductivity for

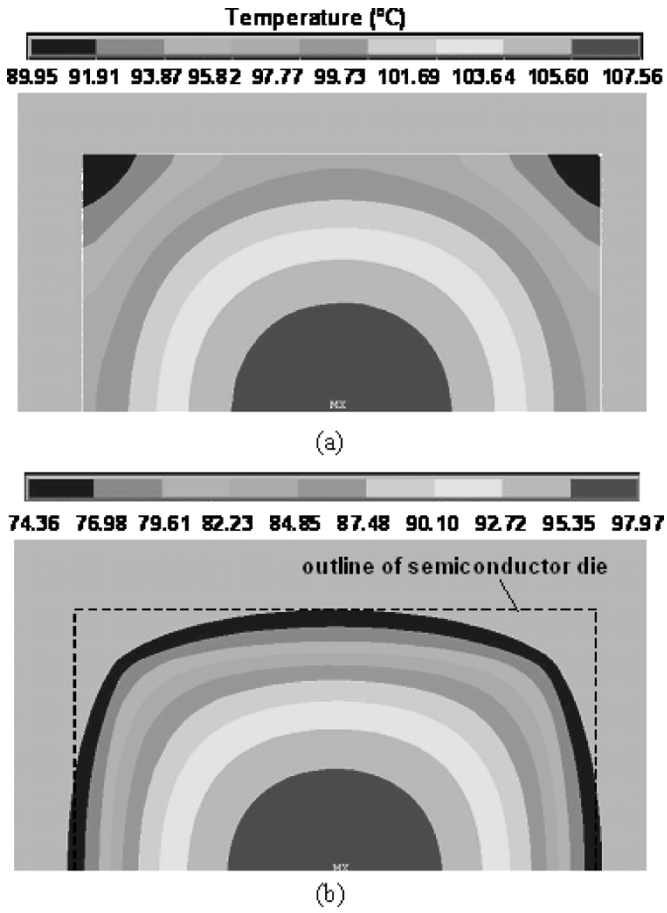


Fig. 7. Temperature (a) across the die surface and (b) on the DBC surface underneath the die predicted by the single-sided global model.

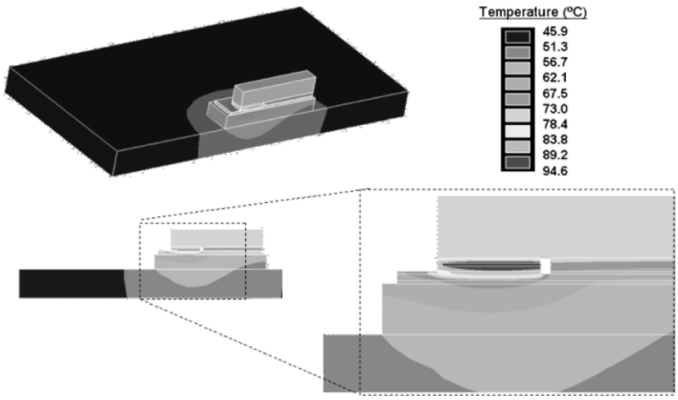


Fig. 8. Temperature distribution predicted by the double-sided global model under nominal conditions.

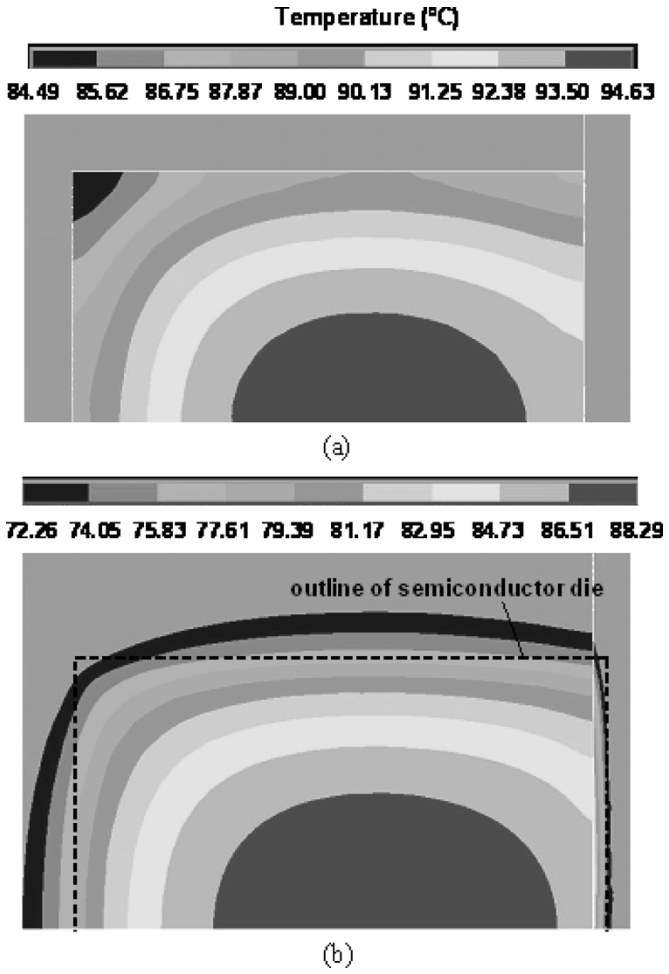


Fig. 9. Temperature (a) across the die surface and (b) on the DBC surface underneath the die predicted by the double-sided global model.

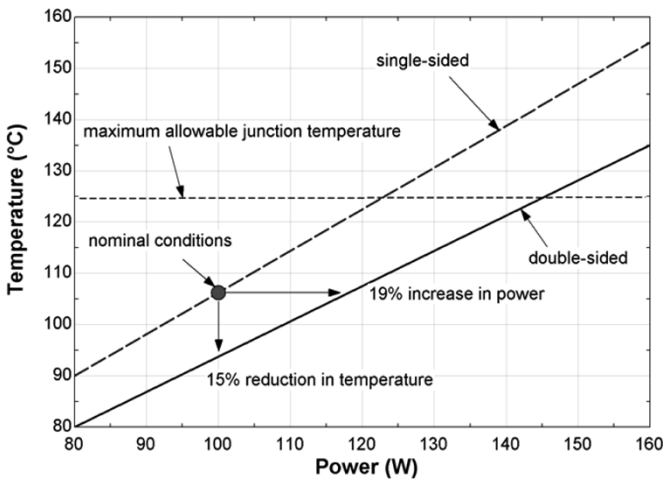


Fig. 10. Maximum die temperature as a function of chip power for single-sided and double-sided configuration.

the single- and double-sided configurations. Notice that a dielectric thermal conductivity of 60 W/m·K produces the same operating temperature reduction in a single-sided configuration as can be expected by the addition of a heat pipe. The addition of the heat pipe provides improved thermal performance compared to single-sided cooling over the entire range of dielectric conductive values; however the improvement becomes less as the conductivity of the dielectric layer increases.

Contact resistance was modeled both at the baseplate-to-heat sink interface and at the surfaces of the heat pipe evaporator and condenser. However, the objective of the contact resistance sensitivity analysis was to evaluate the impact of the technique used to mount the heat pipe and the relative importance of creating a high conductivity joint. Therefore, the parametric analysis was performed by holding the base plate-to-heat sink contact resistance constant at the nominal value and varying only

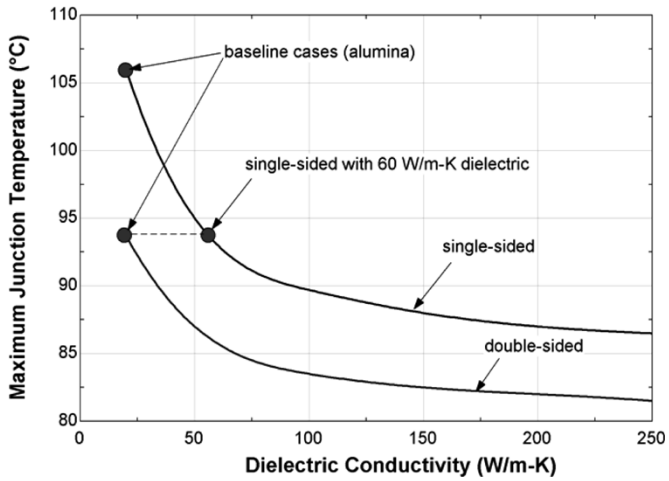


Fig. 11. Maximum die temperature as a function of dielectric thermal conductivity for single-sided and double-sided configuration.

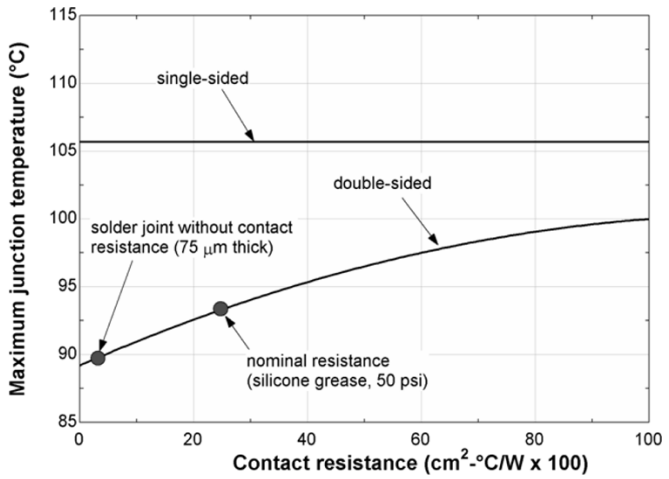


Fig. 12. Maximum die temperature as a function of the contact resistance at the heat pipe surface for single-sided and double-sided configuration.

the contact resistance at the heat pipe surfaces. Fig. 12 illustrates the maximum junction temperature as a function of the contact resistance at the heat pipe surfaces. Since the single-sided configuration does not contain a heat pipe, the parametric study does not affect the single-sided results. The nominal condition corresponds approximately to a silicon grease joint with a 50-psi clamping pressure. The use of a solder joint can be expected to lower the contact resistance. Note that the reduction in the maximum die temperature between the single-sided and double-sided cases increases from 13 °C to 17 °C if a solder joint is used for the heat pipe.

The thermal impedance of the heat sink accounts for 25 °C of the 82 °C temperature rise in the single-sided case. Fig. 13 illustrates the maximum die temperature as a function of the effective heat transfer coefficient, described earlier, for the single-sided and double-sided configurations. Varying the effective heat transfer coefficient corresponds to changing the base plate heat removal mechanism; very small values would correspond to natural convection whereas very large values might be associated with a water-cooled base plate.

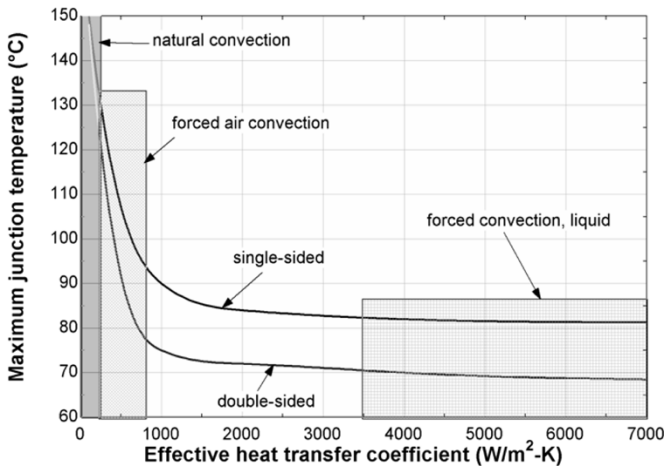


Fig. 13. Maximum die temperature as a function of the effective heat transfer coefficient at the baseplate surface for single-sided and double-sided configuration.

IV. Experimental Results

The numerical analysis described above showed that the double-sided cooling concept may be an attractive technique for reducing the maximum die temperature as well as spatial gradients in the IPEM. The success of double-sided cooling depends on the ability of the heat pipe to handle an appropriate level of heat flux and the parametric analysis showed that contact resistance at the heat pipe evaporator and condenser surfaces have a significant effect on the thermal performance. Therefore, an experiment was designed to measure the performance characteristics of a heat pipe and the contact resistance between it and mating surfaces in order to confirm the values used in a numerical model. The experiment did not include a complete, double-sided cooling configuration; rather, the experiment was designed to measure the resistance of the heat pipe and the contact resistance associated with mounting the heat pipe in isolation.

A rectangular copper/water heat pipe with a sintered copper wick was obtained from Thermacore Inc. The heat pipe dimensions are $13.5 \times 1.2 \times 0.6$ cm^3. The experimental configuration simulates a heat pipe mounted on a power electronics die. The thermal heat load is applied by an electrical heater embedded in a cylindrical copper heater block and evenly introduced over a 1 cm^2 area on one side of the heat pipe evaporator. The heat is removed by a cylindrical, water-cooled heat sink from one side of the 2 cm^2 condenser. The heat pipe is soldered to the heater and the heat sink.

The temperature difference across the heat pipe is measured using type J thermocouples wired in a thermopile arrangement. Thermocouple junctions are also embedded in the heater and heat sink flanges in order to capture the contact resistance. The mass flow rate of the cooling water is measured using a digital scale and stop watch. The inlet and outlet cooling water temperature are computed using redundant penetration thermistors. The voltage and current applied to the heater are measured using voltage taps at the heater and a shunt resistor. Fig. 14 illustrates the key features of the experiment.

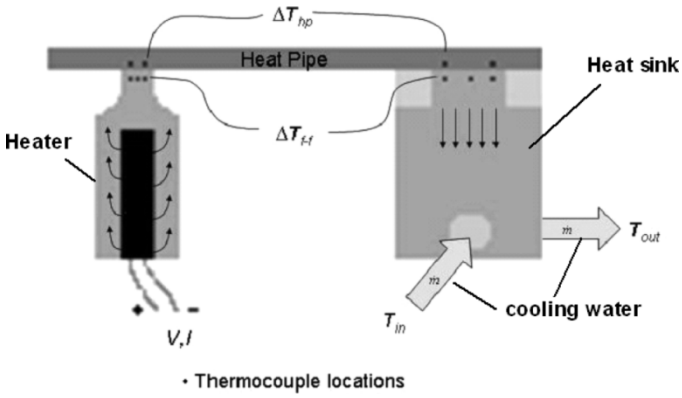


Fig. 14. Experimental configuration showing heater, heat pipe, and heat sink with thermocouple locations indicated.

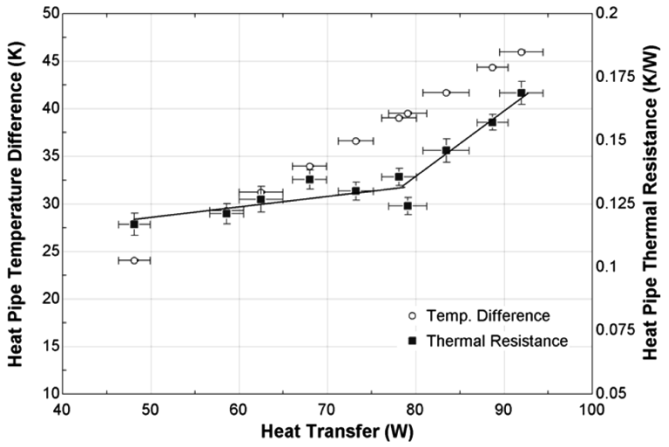


Fig. 15. Measured heat pipe temperature difference and thermal resistance for the evaporator-over-condenser configuration.

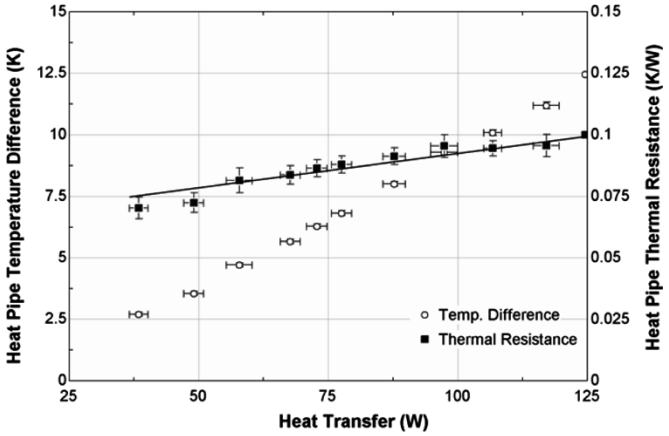


Fig. 16. Measured heat pipe temperature difference and thermal resistance for the condenser-over-evaporator configuration.

The experimental setup is installed in a vacuum chamber. Radiation shielding with fiberglass mesh spacers is applied to the heater block and the inside surfaces of the vacuum can in order to reduce the largest parasitic radiation losses. The separate measurement of the energy absorbed by the water and the power applied to the heater allows the experimental setup to be evaluated using a heat balance; a comparison of these two energy flows. For the data reported here, the energy balance for the apparatus ranged between 93% and 97%.

The heat pipe thermal resistance is defined as the ratio of the temperature difference between the evaporator and condenser over the heat transferred through the system. The heat transferred is taken to be the average of the heater power and cooling water measurements.

The evaporator contact resistance is defined as the ratio of the temperature difference between the heater flange and the evaporator to the heat transferred across this interface (taken to be the heater power), normalized by the evaporator area. The condenser contact resistance is defined as the ratio of the temperature difference between the condenser and the heat sink flange to the heat transferred across this interface (taken to be the cooling water energy), normalized by the condenser area.

With the water lines hooked up and the vacuum can disassembled, the peristaltic pump is started and the fixture rotated to remove any trapped air in the fittings. Then with the water lines full, the vacuum can is assembled and the turbopump activated. Data acquisition begins when the facility is evacuated to a pressure less than 2e-4 torr. The heater power supply is activated and set to some intermediate level to bring the fixture up to operating temperature. The water flow rate is set to achieve a temperature difference between the inlet and exit cooling water of 10 °C. The power supply is operated in current control mode with the maximum voltage set to prevent thermal runaway. Data points are recorded every 5.5 s and steady-state is defined qualitatively by examining the temperature data over at least a 1/2 hour interval. The orientation of the heat pipe relative to gravity can be adjusted by altering the position of the vacuum can.

The temperature difference across the heat pipe and the associated heat pipe thermal resistance as a function of applied heater power is shown in Figs. 15 and 16 for the evaporator-over-condenser and condenser-over-evaporator configurations, respectively. Note that in the evaporator-over-condenser configuration gravity opposes the flow of the vapor. The result is an operating limit of nominally 80 W, as evidenced by the sharp increase in the thermal resistance; this exceeds the predicted requirements for double-sided cooling by a factor of 2 and corresponds to a heat flux of 110 W/cm^2. Note that the boiling limit predicted using the technique described by Faghri [15] is 183 W/cm^2. No such operational limit was observed over the range of applied power investigated here for the condenser-over-evaporator configuration and therefore the heat flux limitation is at least 175 W/cm^2. The thermal resistance of the heat pipe is somewhat larger in the evaporator-over-condenser configuration; although this thermal resistance is never significant relative to other impedances anticipated in a double-sided cooling configuration. The maximum temperature adjacent to either interface of the heat pipe for any of the experimental runs was less than 100 °C, the performance of the heat pipe is likely to decrease if the operating temperature increases.

Fig. 17 illustrates the measured contact resistance (the average of the evaporator and condenser surfaces) as a function

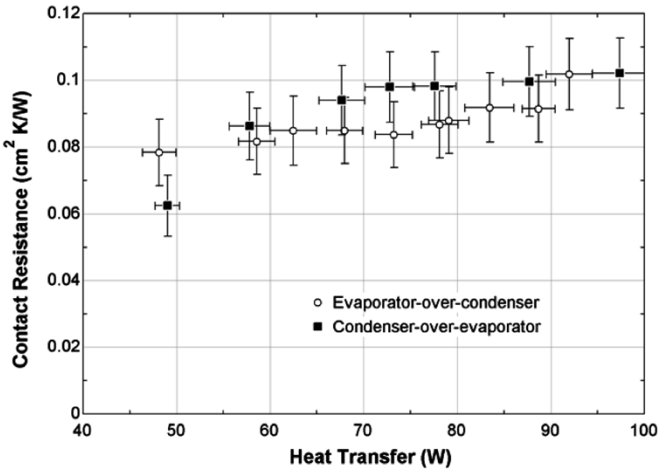


Fig. 17. Measured interface resistance (average of evaporator and condenser surfaces) for both evaporator-over-condenser and condenser-over-evaporator configurations.

of the applied heater power for both the evaporator-over-condenser and condenser-over-evaporator tests. As expected, neither heater power or heat pipe orientation has a strong effect on the interface resistance.

The error bars reported in Figs. 15–17 were estimated based on a detailed uncertainty analysis that includes errors related to data acquisition resolution, temperature sensor accuracy and mounting errors, uncertainty in the mass flow rate, heater voltage, and heater current, calibration precision, parasitic heat loss to the ambient (estimated based on the energy balance), and uncertainty in the active evaporator and condenser areas [16].

V. Conclusion

This investigation has shown that miniature heat pipes may provide an effective means for improving the thermal management of IPEMs fabricated with flip-chip-on-flex planar interconnect designs. More specifically, the numerical results indicate that the use of a miniature heat pipe on the top-side of a flex-based IPEM can reduce the temperature rise in the device by 15% for the same power dissipation or increase the power dissipation by 18% for the same junction operating temperature. Furthermore, the heat pipe reduces the spatial temperature gradients and therefore decreases thermally induced stresses; contributing to increased IPEM reliability. Finally, the heat pipe represents a large thermal mass due to the vaporization of the working fluid. This thermal mass will act to mitigate temperature variations in time related to variations in the operating conditions that might also contribute to failure.

The baseline numerical analysis was performed assuming alumina DBC material. Replacing the alumina with a more thermally conductive dielectric such as aluminum nitride or beryllium oxide would provide larger thermal benefits for single-sided cooling configurations compared to the benefit of adding heat pipes while retaining alumina DBC. However, the heat pipes provide a net improvement in thermal performance regardless of the DBC dielectric material.

The experimental tests verified that a miniature heat pipe is capable of removing the required heat flux, as predicted by the numerical model, regardless of physical orientation in a gravitational field. Finally, the contact resistance measurements for a soldered joint indicated impedance values of nominally $0.1\text{cm}^2 \cdot^\circ$ C/W, significantly higher than what is expected for an indium solder joint. This could increase the resistance associated with the upper path by as much as 10% and reduce the benefit of the double-sided approach by a similar amount.

References

[1] F. C. Lee, J. D. van Wyk, D. Boroyevich, T. M. Jahns, T. P. Chow, and P. Barbosa, "Modularization and integration as a future approach to power electronics systems," presented at the Int. Conf. Integrated Power Systems (CIPS), Bremen, Germany, Jun. 2002.

[2] X. Liu, S. Haque, J. Wang, and G-Q. Lu, "Packaging of integrated power electronics modules using flip-chip technology," in *Proc. 15th Annu. IEEE Applied Power Electronics Conf.*, vol. 1, 2000, p. 290.

[3] C. S. Korman, W. Bicknell, W. Hennessy, W. Daum, W. Roshen, and R. L. Steigerwald, "High density integrated power—a new concept in power integration," *Proc. SPIE*, vol. 2105, pp. 662–672, 1993.

[4] X. Liu, X. Jing, and G-Q. Lu, "Chip-scale packaging of power devices and its application in integrated power electronics modules," *IEEE Trans. Adv. Packag.*, vol. 24, no. 2, pp. 206–215, May 2001.

[5] S. W. Kessler and R. M. McKechnie, "Transcalent silicon power rectifier," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-7, no. 6, pp. 1151–1156, Nov. 1971.

[6] T. D. Sheppard Jr., "Heat pipes and their application to thermal control in electronic equipment," in *Proc. Nat. Electronic Packaging and Production Conf.*, Anaheim, CA, Feb. 1969, pp. 11–13.

[7] S. Kalahasti and Y. K. Joshi, "Performance characterization of a novel flat plate micro heat pipe spreader," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 4, pp. 554–560, Dec. 2002.

[8] T. Nguyen, M. Mochizuki, K. Mashiko, Y. Saito, I. Sauciuc, and R. Boggs, "Advanced cooling system using miniature heat pipes in mobile PC," in *Proc. 1998 IEEE Intersoc. Conf. Thermal Phenomenon*, 1998, pp. 507–511.

[9] B. Shi, T. M. Jahns, and J. M. Pfotenhauer, "Feasibility of heat pipes for double-sided cooling of integrated power electronic modules," presented at the CPES Seminar, Blacksburg, VA, Apr. 2001.

[10] K. A. Woloshun *et al.*, *HTPIPE: A Steady-State Heat Pipe Analysis Program, A User's Manual*: Los Alamos Nat. Lab., 1988.

[11] X. Liu, S. Haque, and G-Q. Lu, "Three-dimensional flip-chip on flex packaging for power electronics applications," *IEEE Trans. Adv. Packag.*, vol. 24, no. 1, pp. 1–9, Feb. 2001.

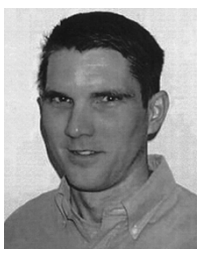
[12] T. P. Chow and Z. Shen, "An analytical IGBT model for power circuit simulation," in *Proc. 3rd Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, Apr. 1991, pp. 79–82.

[13] M. M. Yovanovich, J. R. Culham, and P. Teertstra, "Calculating interface resistance," *Electron. Cooling*, vol. 3, no. 2, pp. 24–27, May 1997.

[14] W. Werdecker and F. Aldinger, "Aluminum nitride—an alternative ceramic substrate for high power applications in microcircuits," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. CHMT-7, no. 4, pp. 399–405, Apr. 1984.

[15] A. Faghri, *Heat Pipe Science and Technology*. Washington D.C.: Taylor and Francis, 1995.

[16] T. J. Martens, "Double-Sided IPEM Cooling Using Miniature Heat Pipes," M.S. thesis, Mech. Eng. Dept., Univ. Wisconsin, , Madison, 2003.



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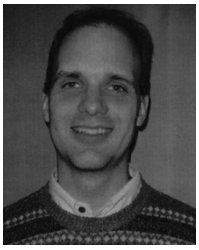

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