Double Snapback Characteristics in High-Voltage nMOSFETs and the Impact to On-Chip ESD Protection Design

Ming-Dou Ker, *Senior Member, IEEE,* and Kun-Hsien Lin, *Student Member, IEEE*

***Abstract*—The double snapback characteristic in the high-voltage nMOSFET under transmission line pulsing stress is found. The physical mechanism of double snapback phenomenon in the high-voltage nMOSFET is investigated by device simulation. With double snapback characteristic in high-voltage nMOSFET, the holding voltage of the high-voltage nMOSFET in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristic will cause the high-voltage CMOS ICs susceptible to the latchup-like danger in the real system applications, especially while the high-voltage nMOSFET is used in the power-rail electrostatic discharge clamp circuit.**

***Index Terms*—Double-diffused drain (DDD), electrostatic discharge (ESD), high-voltage nMOSFET, lateral diffused MOS (LDMOS), latchup.**

I. Introduction

HIGH-VOLTAGE transistors in smart-power technology are extensively used for display driver ICs, power supplies, power management, and automotive electronics. The electrostatic discharge (ESD) reliability is an important issue for high-voltage MOSFET with applications in these products. In smart-power technology, most of the publications related to ESD protection devices concern the lateral or vertical bipolar transistors [1], [2]. However, process complexity and fabrication cost are increased by adding bipolar modules into the CMOS process. The high-voltage MOSFET has been widely used as the common ESD protection device in the high-voltage CMOS ICs, because it can work as both of output driver and ESD protection device simultaneously without additional process modification. The earlier publications focused on analyzing and improving ESD robustness of the high-voltage MOSFET [3]–[6]. Although the double snapback characteristic in the n-p-n bipolar device for smart-power technology has been reported [1], however, the latchup-like failure from the high-voltage MOSFET as ESD protection device under normal circuit operating condition was not considered in the earlier reports.

In this letter, the double snapback characteristic in high-voltage nMOSFET under transmission line pulsing (TLP) stress is found to have a very low holding voltage, which could suffer the transient-induced latchup failure [7] during normal circuit operating condition, especially when such high-voltage nMOSFETs are used in on-chip ESD protection circuits. The physical mechanism of double snapback characteristic in high-voltage nMOSFET is clearly investigated by two-dimensional device simulation.

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The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: mdker@ieee.org).

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II. Experimental Results and Analysis

A. The Double-Snapback Characteristic

The double-diffused drain (DDD) MOS structure fabricated in a 0.35-μm 18-V CMOS process and lateral diffused MOS (LDMOS) structure fabricated in a 0.25-μm 40-V CMOS process are studied in this work. The TLP system with a pulse width of 100 ns and a rise time of $\sim$10 ns is used to measure the snapback current–voltage (*I–V*) curves of the fabricated 18-V and 40-V nMOSFET devices. The TLP-measured *I–V* characteristics of 18-V and 40-V gate-grounded nMOS (GGNMOS) devices are shown in Fig. 1(a) and (b), respectively. The corresponding cross-sectional view of the device structure is also shown in the inset of the figure. From the measured results, the double-snapback characteristics are found both in 18-V nMOSFET and 40-V nMOSFET. For the 18-V nMOSFET shown in Fig. 1(a), after the first snapback voltage at 22.2 V, the device snaps back to 8.5 V. Then, the device quickly goes into the second snapback, and the voltage drops to only $\sim$5 V. The slope of the snapback curves is almost the same at first and second snapback states. For the 40-V nMOSFET shown in Fig. 1(b), after the first snapback voltage at 27.2 V (52 V in dc), the device snaps back to 23 V, from where the voltage strongly increases again. Then, the device goes into the second snapback, and the voltage drops to only $\sim$7 V. In 40-V nMOSFET, the turn-on resistance of the first snapback state is much larger than that of the second snapback state. The difference between the TLP breakdown point and the dc breakdown point in the 40-V nMOSFET is due to the large displacement currents caused by the dv/dt transition during TLP pulse.

B. Simulations and Analysis

The first snapback mechanism involves both avalanche breakdown and turn on of the parasitic bipolar transistor [8]. For 40-V nMOSFET, the avalanche generation is initiated by the n^+ buried layer (NBL)/p-well junction. Fig. 2(a) shows the current distribution in the 40-V nMOSFET under first snapback state, where the current path flows vertically into the NBL region. Due

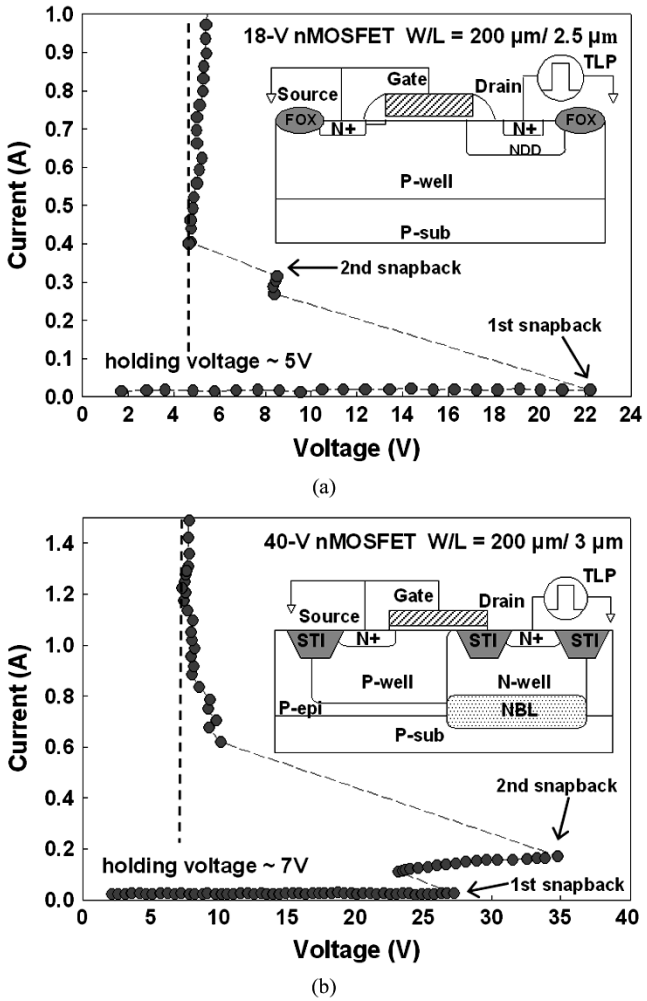


Fig. 1. TLP-measured *I–V* characteristics of (a) DDD MOS structure fabricated in a 0.35-μm 18-V CMOS process and (b) LDMOS structure fabricated in a 0.25-μm 40-V CMOS process.

to the longer current path through lightly doped well region, the turn-on resistance is large at the first snapback state, as that shown in Fig. 1(b). When the current further increases, the device enters into high-injection condition and the Kirk effect [9] occurs. The base push-out effect causes the maximum electric field to change from the NBL/p-well junction to the n^+/n-well junction. Due to higher multiplication rate at this higher doped region, a strong snapback occurs to cause a low holding voltage. Fig. 2(b) shows the current distribution in the 40-V nMOSFET under the second snapback state. The current path changes from the vertical direction to the lateral direction, when the device switches from the first to the second snapback state. The turn-on resistance becomes much smaller when the current path flows in the lateral direction. For 18-V nMOSFET, the avalanche generation is initiated by the n-diffused-drain (NDD)/p-well junction. With shallower NDD diffusion in the device structure, the current path basically flows in the lateral direction at the first and second snapback states. Therefore, the turn-on resistance is almost the same at these two states. In addition, with shallower NDD diffusion, the first snapback state could be not obvious, because the maximum electric field changes from the NDD/p-well junction to the n^+/NDD junction quickly.

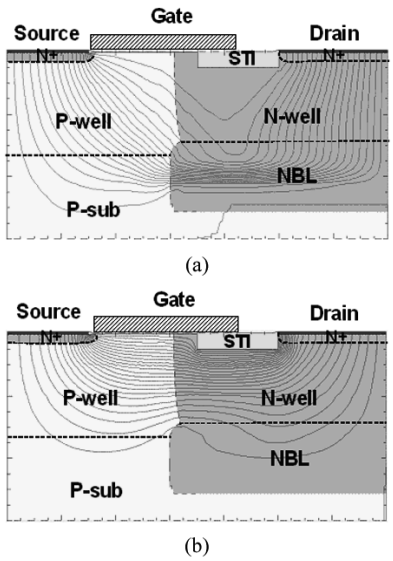


Fig. 2. Simulated current distributions in the 40-V nMOSFET under (a) the first snapback state and (b) the second snapback state.

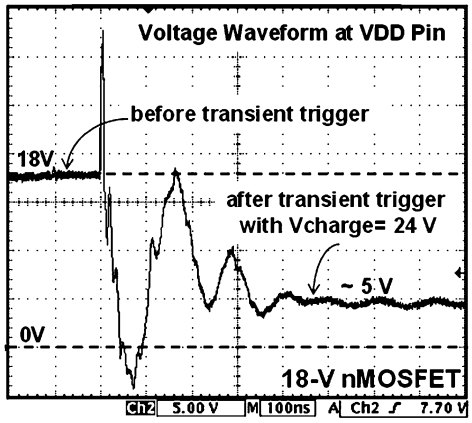
The doping concentration and junction depth of lightly doped drain region (NDD for 18-V nMOSFET and n-well for 40-V nMOSFET) are the major factors to influence double snapback characteristics. Because these factors directly affect the process of base push-out effect, which changes the maximum electric field from initial avalanche breakdown region to the n+/n- region. The increase of doping concentration and junction depth of lightly doped drain region will delay space-charge region edge moving toward n+/n- region, and therefore delay the device into the second snapback state.

C. Transient Latchup Test

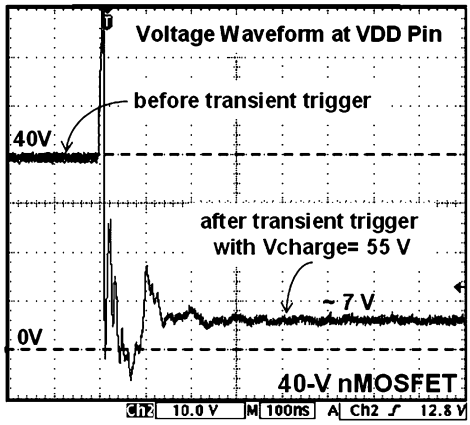
Transient latchup (TLU) test [7] is used to investigate the susceptibility of high-voltage nMOSFET to the noise transient or glitch on the power lines during normal circuit operating condition. The charging voltage (Vcharge) on the energy storage capacitor generating the transient is used to trigger the device into the latch state [7]. A power supply voltage of 18 V (40 V) is applied to 18-V (40-V) nMOSFET used as power-rail clamp device during TLU test. The clamped voltage waveforms across the 18-V nMOSFET and 40-V nMOSFET under TLU test are shown in Fig. 3(a) and (b), respectively. From the measured results, the clamped voltage level of 18-V (40-V) nMOSFET in snapback breakdown condition is $\sim$5 V ($\sim$7 V) due to the transient triggering with the capacitor charging voltage of 24 V (55 V). The clamped voltage level of the device is consistent with the holding voltage measured by TLP stress. The experimental results have confirmed that the latchup-like issue between the power rails will occur, when the high-voltage nMOSFET is triggered by the noise transient on power lines.

III. Impact to On-Chip ESD Protection

In the whole-chip ESD protection scheme, the ESD clamp circuit between the VDD and VSS power rails has been often added into the chip to avoid ESD damages located in the internal circuits [10]. When the high-voltage nMOSFET is used as the



(a)



(b)

Fig. 3. Measured voltage waveforms on (a) 18-V nMOSFET, and (b) 40-V nMOSFET, before and after transient trigger.

power-rail ESD clamp device, the device is expected to be kept off in normal circuit operation condition. In the ESD stress condition, the parasitic bipolar transistor in the nMOSFET can be triggered on to discharge the ESD current. During the system-level electromagnetic compatibility (EMC)/ESD test [11], the power lines of ICs in the system board can be coupled with an overstress voltage even up to several hundred volts [12]. Such a system-level EMC/ESD event easily causes the transient-induced latchup failure in CMOS ICs [13], [14]. Because the holding voltage of high-voltage nMOSFET in snapback breakdown condition is much smaller than the power supply voltage, the latchup-like issue between the power rails will occur. This phenomenon often leads to IC function failure or even destruction by burning out. Therefore, the low holding voltage characteristic of the high-voltage nMOSFET will cause the high-voltage CMOS IC susceptible to the latchup-like danger during normal circuit operating condition.

IV. Conclusion

The double snapback characteristic in the high-voltage nMOSFET has been investigated in this work. With both measured and simulation results, the double snapback characteristics in the 18-V and 40-V nMOSFETs have been fully analyzed. The latchup-like issue between the power rails in the high-voltage CMOS ICs has been confirmed by TLU test. How to avoid the latchup-like failure of high-voltage nMOSFET under normal circuit operating condition will be an important challenge to on-chip ESD protection design for high-voltage CMOS IC products.

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