Drain Induced Barrier Lowering (DIBL) Effect on the Intrinsic Capacitances of Nano-Scale MOSFETs

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ABSTRACT

This paper presents a physical explanation of MOSFET intrinsic gate to drain capacitance (C_{GD}) going negative due to Drain Induced Barrier Lowering (DIBL) effect. For the sub-90nm MOS devices, DIBL effect may be dominant enough to guide C_{GD} to negative if de-embedded from parallel extrinsic overlap, outer and inner fringing capacitances. The possibility of this phenomenon is evident from the results of our 2-D TCAD simulations of conventional bulk MOS structure. However negative capacitances lead to non-convergence issue in circuit simulators and need to be bounded in MOS devices compact models.

Keywords: MOSFET, Negative Intrinsic Capacitance, DIBL.

1 INTRODUCTION

MOSFET intrinsic capacitances' going negative is a major concern in the compact model community. Negative Intrinsic Capacitances (NIC) can raise non-convergence issues in circuit simulators, e. g. if placed in series with positive resistors, it can make the system unstable. NICs may also cause problem in various category of simulations such as Electro Static Discharge (ESD) events, where the voltages and currents are somewhat unusual. Consequently, compact models resulting in NICs are criticized by the member companies of Compact Model Council (CMC) and also in the literature [1]-[3]. To negotiate with NICs in the leading industry standard compact models such as BSIM3 and BSIM4, fixes based on bounding variable values have been proposed in the course of time (e.g. [4]).

On the other hand, as MOS devices are scaling down aggressively [4], DIBL effect is increasing. However, investigation of the effect of increasing DIBL is lacking in the literature. Though Filho et al. pointed out the DIBL effect on C_{GD}, they did not explain the underlying physics [5].

MOSFET negative intrinsic capacitances are usually considered as non-physical. But in some cases these NICs can be explained using physical phenomena. In this work we particularly focus on physics behind the possibility of gate to drain intrinsic capacitance (C_{GD}) going negative.

2 THEORY

Four terminal MOS device have sixteen capacitances, including four self capacitances corresponding to its four terminals namely, Gate (G), Drain (D), Source (B), Body (B). The sixteen capacitances form the Indefinite Admittance Matrix (IAM). Each element C_{ij} of this capacitance matrix describes the dependence of the charge at the terminal i with respect to the voltage applied at the terminal j with all other voltages held constant.

$$C_{ij} = \begin{cases} -\dfrac{\partial Q_i}{\partial V_j}, & i \neq j, \;\; i,j = G,D,S,B \\ \dfrac{\partial Q_i}{\partial V_j}, & i = j \end{cases} . \qquad (1)$$

In matrix form,

$$C_{ij} = \begin{bmatrix} C_{GG} & -C_{GD} & -C_{GS} & -C_{GB} \\ -C_{DG} & C_{DD} & -C_{DS} & -C_{DB} \\ -C_{SG} & -C_{SD} & C_{SS} & -C_{SB} \\ -C_{BG} & -C_{BD} & -C_{BS} & C_{BB} \end{bmatrix}. \qquad (2)$$

Each row must sum to zero for the matrix to be reference-independent, and each column must sum to zero for the device description to be charge-conservative.

From Eq. (1),

$$C_{GD} = -\frac{\partial Q_g}{\partial V_D} . \qquad (3)$$

Inversion charge can be explained as

$$Q_{inv} = -C_{OX}\left(V_G - V_{FB} - \varphi_s - \gamma\sqrt{\varphi_s}\right). \quad (4)$$

Here, C_{OX} is the oxide capacitance, V_{FB} is the flatband voltage, φ_s is the surface potential and γ is the body factor.

When V_D increases, surface potential at the drain side also increases. So, from Eq. (4), Q_{inv} decreases which results in a decrease in C_{GD}. Eventually C_{GD} vs V_{DS} should go to zero at high V_{DS} in ideal long channel devices.

For long channel devices, gate/channel charge keep decreasing with increasing V_D and eventually become insensitive to changes in V_D. On the other hand, for short channel devices, initially gate/channel charge decreases with increasing V_D until a considerable amount of DIBL effect kicks in. Due to barrier lowering at the source side, it is very much likely to have more channel charge with increasing V_D and consequently may lead to negative C_{GD}.

3 RESULTS AND DISCUSSIONS

To manifest the theory presented here, we run TCAD simulations on a simple bulk NMOSFET structure. To comprehend the impact of inversion layer charges (Q_{inv}) on the C_{GD} vs V_{DS} characteristics, 2-D TCAD simulation is done for two different values of gate bias, $V_G = V_{th}$ and $V_G = V_L$. Here, V_{th} is the threshold voltage and we define V_L as the gate voltage at which drain current (I_D) is 0.1% of its value at $V_G = V_{th}$. At $V_G = V_{th}$, there is sufficient Q_{inv} and at $V_G = V_L$, there is negligible amount of Q_{inv}.

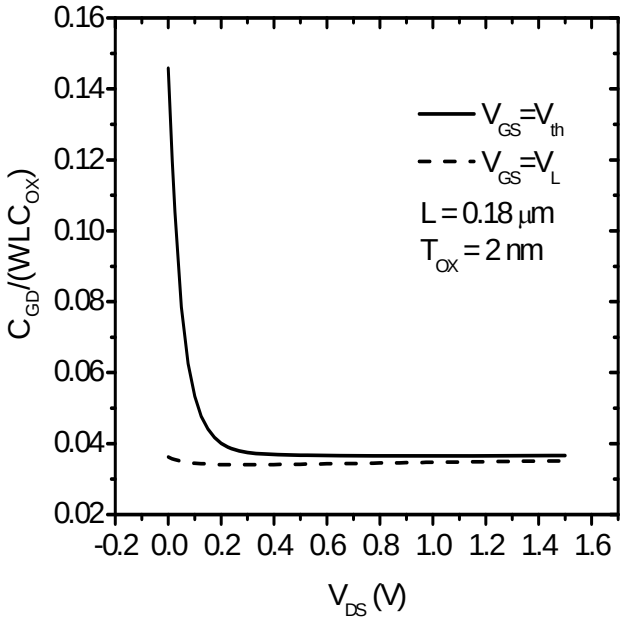

Figure 1: Normalized C_{GD} vs V_{DS} for channel length L=0.18 μm.

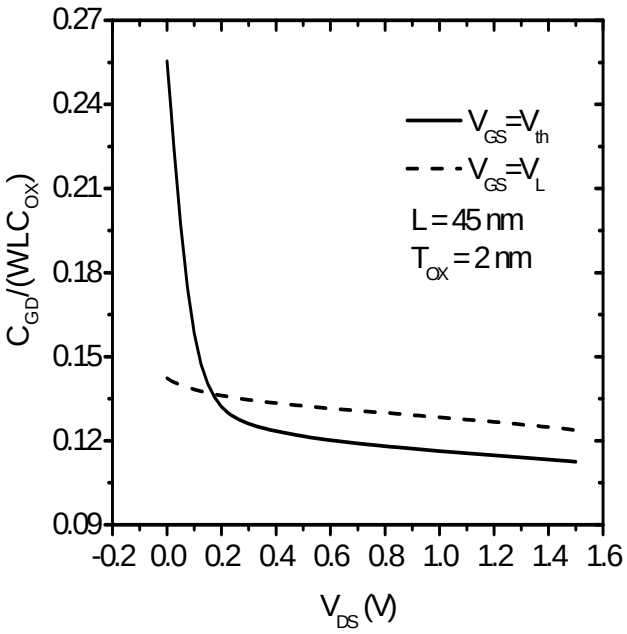

Figure 2: Normalized C_{GD} vs V_{DS} for channel length L=45 nm.

Figs. 1 and 2 show normalized C_{GD} (with WLC_{OX}) vs V_{DS} for channel lengths (L) of 0.18μm and 45nm respectively keeping all other parameter unchanged. C_{GD} presented here is not only due to gate/channel charges (intrinsic) but also from other parasitic extrinsic sources such as overlap, inner, and outer fringe capacitances etc. Fig. 3 show graphically all the intrinsic and extrinsic capacitances related to gate and drain terminal.

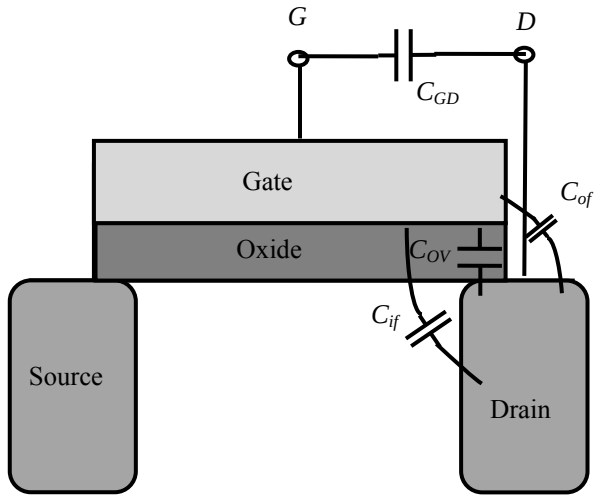

Figure 3: MOSFET intrinsic and extrinsic capacitances related to gate and drain terminal.

Though some work has been reported on de-embedding the parasitic capacitances [6], [7], unfortunately there is no way to completely de-embed all the extrinsic capacitances from C_{GD} in the bias region of our interest. Unlike Fig. 1, Fig. 2 shows a crossover between the two curves. The possible reason is for shorter channel length, DIBL effect is more dominant. But only this cross over cannot indicate the possible negative intrinsic C_{GD} since the contribution of extrinsic capacitances are different in the two curves.

To observe the effect of DIBL on C_{GD} vs V_{DS} gate oxide thickness T_{OX} and junction depth (X_j) are varied. The threshold voltage shift for DIBL may be expressed as [8]

$$\Delta V_{th} \propto V_{DS} e^{\frac{-L}{l}}. \quad (5)$$

Here, l is the characteristic length which may be expressed as

$$l \approx \sqrt{3\, T_{OX} X_j}. \quad (6)$$

From Eq. (5), DIBL is increased with decreasing L/l ratio. Figs. 4 and 5 show I_{DS} vs V_{GS} curves for high and low V_{DS} for the same structure of Figs. 1 and 2. Fig. 2 shows much more V_{th} shift than Fig. 1 due to smaller L/l ratio which results in more DIBL.

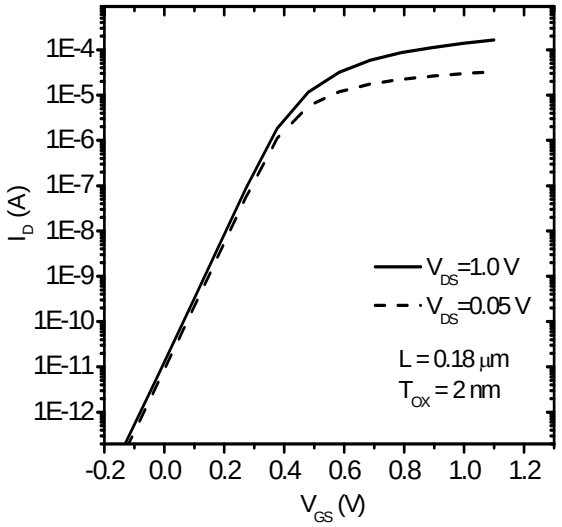

Figure 4: I_D vs V_{GS} for channel length L=0.18 μm

Fig. 6 shows normalized C_{GD} vs V_{DS} for different gate oxide thickness T_{OX}. With increasing T_{OX} (therefore increasing DIBL), the separation between $V_G = V_{th}$ and $V_G = V_L$ curves keep increasing with increasing V_{DS} after the crossover point. This strongly infers the possibility of intrinsic C_{GD} going negative for an appreciable amount of

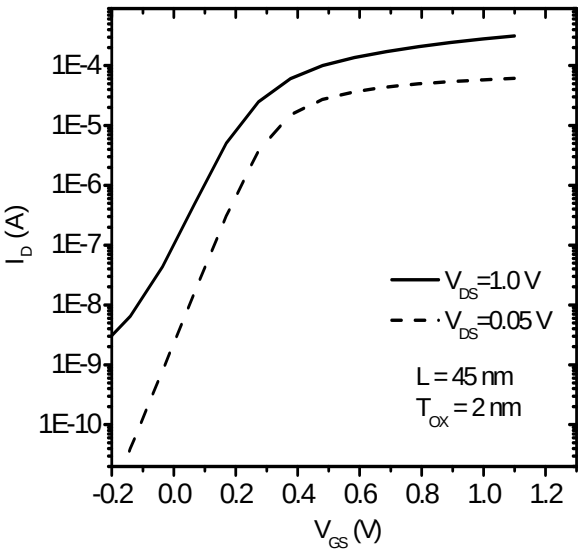

Figure 4: I_D vs V_{GS} for channel length L=45 nm

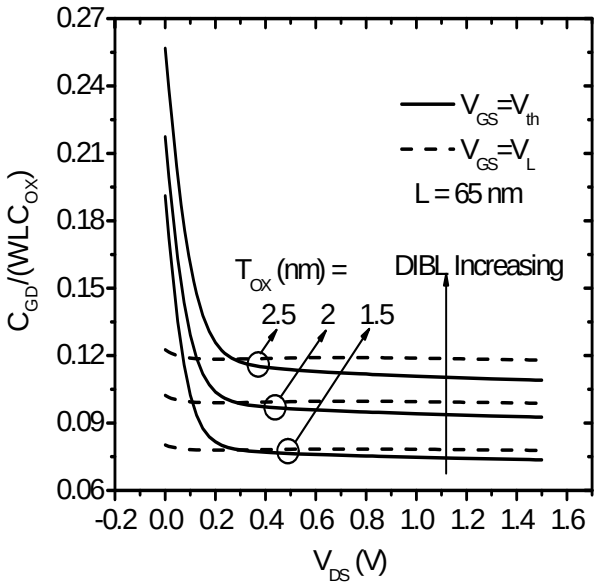

Figure 6: Normalized C_{GD} vs V_{DS} for different T_{OX} values.

DIBL. Fig. 7 shows another way of representing DIBL effect on C_{GD}. Normalized C_{GD} vs V_{DS} is plotted for different source/drain junction depth X_j. With increasing DIBL, shifting of crossover point towards left and increasing the separation of the $V_G = V_{th}$ and $V_G = V_L$ curves a bit after crossover point as well restate the probability of intrinsic C_{GD} going negative. If C_{GD} goes

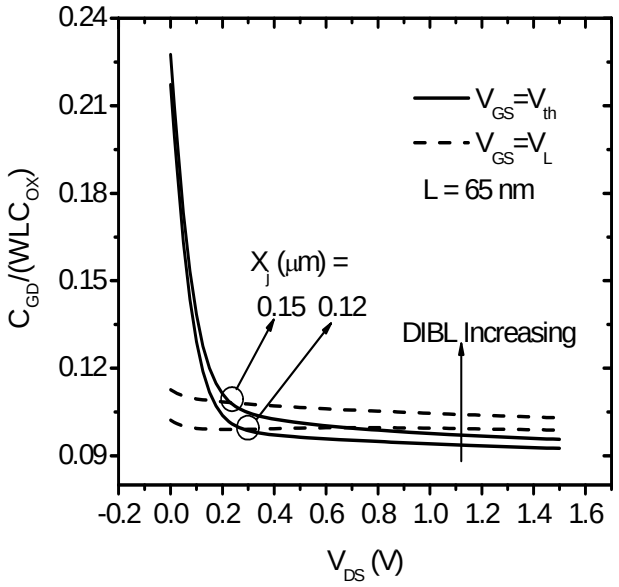

Figure 7: Normalized C_{GD} vs V_{DS} for different X_j values.

negative then other drain bias dependent intrinsic capacitances (C_{DD}, C_{SD}, and C_{BD}) will change accordingly for charge conservation according to Eq. (2).

4 CONCLUSION

We presented a physical elucidation behind the possibility of MOSFET intrinsic gate to drain capacitance going negative for high drain bias. A comprehensive inner fringing capacitance model for entire gate and drain bias range of typical MOSFET operation modes is required to make this phenomenon more transparent. But from compact model uses point of view, negative capacitance values are completely unwanted to avoid non-convergence in the circuit simulator. Since these negative capacitances are coming from physical effects, from model developer perspective, bounding these capacitances in positive is difficult.

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