Driving Toward Higher I_{DDQ} Test Quality for Sequential Circuits: A Generalized Fault Model and Its ATPG

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Abstract

We propose a generalized stuck-at fault model for sequential circuits under the selective I_{DDQ} test strategy. The proposed fault model makes a pessimistic assumption on the Boolean fault effects when the fault is activated. We show that by using the proposed fault model, test sequences of higher quality can be generated and/or selected. We further propose a test vector generation and selection method for this fault model. We present results to illustrate that a high fault coverage for the proposed fault model can be achieved by a small test set under the selective I_{DDQ} test environment.

1 Introduction

I_{DDQ} testing has been proposed as an effective method for detecting actual defects in the CMOS circuits [2]–[4]. In I_{DDQ} testing, the fault effects are directly observed as the extra current at the power lines spread over the entire chip. This provides much better circuit observability, and thus the cost of test vector generation and the hardware overhead for improving testability are greatly reduced. One major cost of I_{DDQ} testing is its long test application time. A popular test application scheme is the selective I_{DDQ} test scheme [4] [5], where even though a large vector set is applied, only a small fraction of the vectors is selected for the current measurement. Under this test application scheme, the test application time is strongly related to the number of the vectors for which the current is measured and only weakly related to the total length of the test set. Therefore, the objective of the vector compaction is to reduce the number of the vectors for I_{DDQ} measurement.

Extensive studies have been made for ATPG for sequential circuits in the voltage testing environment. ATPG algorithms for combinational circuit have been extended successfully for sequential circuit by using the time frame expansion technique [1]. For I_{DDQ} testing, the same algorithms can be used by treating every gate output as a primary output [2]. In the time frame expansion technique, the target fault is present in every time frame. Under the selective I_{DDQ} test scheme, it is possible that the fault be activated at time frames which are not selected for I_{DDQ} measurement. A question to be answered is : what Boolean logic value should the faulty signal be assigned to for the fault effect propagation (to the next state lines)? The value assigned for further fault effect propagation will affect the faulty circuit values in the flip-flops which will in turn affect the fault detection in the future time frames.

Several fault models have been proposed for I_{DDQ} testing. Under the selective I_{DDQ} test scheme, different models assume different faulty logic values when a fault is activated. For example, in the leakage fault model (LF) [5], the faulty logic value is assumed to be the same as the fault-free logic value. On the other hand, in the pseudo stuck-at fault model (PSAF) [2], the fault is assumed to be permanently stuck at a binary value. Different assumptions make fault simulators and ATPG tools generate different test sets and report different fault coverages for sequential circuits. Moreover, it is likely that some vectors which activate a defect are not selected for measurement. The defect which is activated but is not detected may produce a logic value inconsistent with the assumption of a specific fault model. Then, the states of the faulty sequential circuit will become different from the simulated ones and the fault coverage computed will be different from the actual coverage.

In this paper, we focus on fault modeling and vector generation for sequential circuits in the selective I_{DDQ} test environment. We propose a generalized stuck-at fault model for intra gate defects. In this model, the faulty logic level at the fault site is assumed to be an unknown (X) whenever a fault is activated. Tests targeting these generalized faults will then cover a broader class of defects compared with tests targeting PSAFs or LFs. The described fault model only covers intra gate defects but its concept can be ex-

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tended to the other fault models, such as bridging faults. Based on this fault model, we discuss issues on fault simulation, vector generation, and vector selection. We show that by using this generalized fault model, test sequences of higher quality can be selected or generated.

The paper is organized as follows. In Section 2, we briefly summarize the fault models previously proposed and then discuss the generalized model. In Section 3, we show the effectiveness of the proposed model under the selective I_{DDQ} test environment. In Section 4, a test vector generation and selection method is described. Experimental results are presented in Section 5. Section 6 concludes the paper.

2 Fault Model

Several fault models have been proposed for I_{DDQ} testing [5] [2]. In this paper, we focus on fault models for intra gate defects.

2.1 Fault Models for intra gate defects

The leakage faults [5] have been shown to be a good fault model for intra gate defects. In this model, 6 transistor shorts are modeled for each transistor in a gate. It is assumed the LFs only draw extra I_{DDQ} current and do not cause any logic value change in the presence of the fault. This assumption can also be used for stuck-at faults. In the rest of the paper, such stuck-at faults are referred to as *leakage stuck-at faults* (LSAFs). The pseudo stuck-at fault model is also used successfully for I_{DDQ} testing [2]. It has been shown that a PSAF test set for combinational circuits consisting of primitive gates AND, NAND, OR, NOR and NOT detects all the LFs in these primitives. In the PSAF model, the logic value at the fault site is assumed to be stuck at "0" or "1" permanently.

In a real device, when a fault is activated, the voltage level at the fault site depends on many factors, such as the defect class, DC characteristics of the gates driven by the faulty gate or net, the vector applied to the gates, wire resistance, *etc*. Therefore, it may happen that the actual faulty value is inconsistent with the one assumed by the fault model. If the vectors which activate some of the defects are not selected for the current measurement, the inconsistency will be propagated into future time frames. Therefore, the faulty circuit states and fault detectability for the rest of the test sequence will be different from the simulated ones.

Example 1: Consider the circuit in Fig. 1 which contains the resistive short defect *D1*. Assume a test sequence T1 of length 3 is applied : (i,j) = { (1,0), (0,1), (0,1) }. The faulty logic level at *m* and in turn at gate B depend on the resistance of *D1*. If the resistance is high enough, *D1* will not affect the logic level when the defect is activated. On the other hand, a low resistance will make *D1* defect a *hard* stuck-at 0 fault. For a resistance in between, the faulty value is not predictable.

Table 1 shows the faulty values at internal nodes *m* and *n* under different assumptions. The columns under PSAF (LSAF) shows the signal vales using the PSAF (LSAF) model. In this table, *Av* denotes that the defect is activated by the vector and its faulty value is *v*. *Uv* denotes that the defect is *NOT* activated by the vector and its faulty value is *v*. If the row with an entry of *Av* is selected for I_{DDQ} measurement, the I_{DDQ} should be elevated and the defect is considered detected. The defect *D1* is first activated regardless of the faulty value of *D1*. Under the LSAF model, the faulty value at node *m* is "1" and the next state value at node *n* is "0" after the application of vector 2. Under the PSAF model, the faulty value at node *m* is always considered as "0" and the next state value at node *n* becomes "1". As a result, different faulty values are stored in the flip-flop C for these two different assumptions. This makes *D1* undetected by vector 3 under the LSAF model though it is detected by vector 3 under the PSAF model.

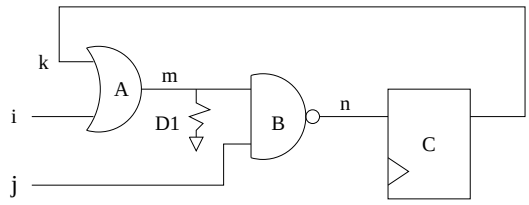

Figure 1: Example 1

Table 1: Signal values under the PSAF & LSAF models

Vec	i	j	PSAF		LSAF	
			m	n	m	n
1	1	0	A0	1	A1	1
2	0	1	A0	1	A1	0
3	0	1	A0	1	U0	1

Example 2: The faulty value propagated to different branches of faulty signal stem may be different due to the different DC characteristics of the gates at branches and the wire resistance of each branch. For example, the resistive short defect *D2* shown in Fig. 2 is activated when h = j = 1. The four possible faulty values at nodes *p* and *q* are listed in Table 2 depending on the factors mentioned above. One of the four cases occurs in the faulty circuit. Note that it is possible that the voltage levels at *p* and *q* be somewhere between logic "0" and logic "1". The four cases listed could be considered as values perceived by gates A and B. Case 1 and Case 4 follows the assumptions of PSAF and LSAF respectively. On the other hand, Case 2 and 3 are not covered by these fault models. Table 3 shows the logic values at internal nodes *p*, *q* and *r* for the input sequence T2 : (i, j, k) = { (0,0,1), (1,1,0), (0,1,1) }. As shown in Table 3, *D2* is not detected by vector 3 under Case 2 while it is detected by vector 3 for all other cases.

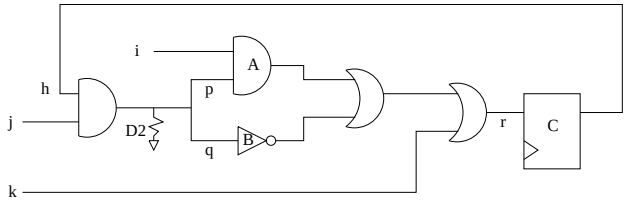

Figure 2: Example 2

Table 2: Possible values at p & q due to activation of D2

Case	p	q
1	0	0
2	0	1
3	1	0
4	1	1

Table 3: Signal values under different value propagation

Vec	i j k	Case 1	Case 2	Case 3	Case 4
		p q r	p q r	p q r	p q r
1	0 0 1	U0 U0 1	U0 U0 1	U0 U0 1	U0 U0 1
2	1 1 0	A0 A0 1	A0 A1 0	A1 A0 1	A1 A1 1
3	0 1 1	A0 A0 1	U0 U0 1	A1 A0 1	A1 A1 1

2.2 Generalized Stuck-at Fault Model

We generalize the pseudo stuck-at faults for I_{DDQ} testing for sequential circuits. The generalized model is called the *Generalized Stuck-at Fault (GSAF)* model. In this model, the logic value at the fault site is assumed to be an unknown (X) whenever it is activated. Because of this assumption, only the vectors which activate the fault without using the effect from the fault site will be selected.

Table 4 shows the internal signal values of defect *D1* in Example 1 under the GSAF model. The values at node *m* are X's in vector 1 and 2 because defect *D1* is activated. After the application of vector 2, the next state line *n* becomes an X which is propagated from the fault site. In this model, *D1* is not activated by vector 3. Therefore, vector 3 is excluded from consideration for selecting the vectors to detect *D1* in the selective I_{DDQ} test scheme. Similarly, vector 2 is the only vector that guarantees to detect the defect *D2* as shown in Table 5. These are consistent with the discussion in the previous subsection.

Because of the more pessimistic assumption on faulty value made in the GSAF model, the selected vectors will cover a broader class of defects as compared with those selected based on the PSAF or LSAF models and therefore, achieve a better defect coverage.

Note if every vector is selected for I_{DDQ} measurement, known as the every-vector I_{DDQ} test scheme [4], there will be no difference among LSAFs, PSAFs and GSAFs. Under the every-vector I_{DDQ} test scheme, when a fault is activated, it is detected and the detectability of the fault in future cycles becomes irrelevant.

Table 4: Signal values of Ex. 1 under the GSAF model

Vec	i	j	m	n
1	1	0	Ax	1
2	0	1	Ax	x
3	0	1	Ux	x

Table 5: Signal values of Ex. 2 under the GSAF model

Vec	i	j	k	p	q	r
1	0	0	1	U0	U0	1
2	1	1	0	Ax	Ax	x
3	0	1	1	Ux	Ux	1

3 Effectiveness of the GSAF model

We conducted an experiment to evaluate the effectiveness of the GSAF model. For a given test set, we use a known vector selection algorithm to select I_{DDQ} measurement vectors for three different fault models: the LSAF, PSAF and GSAF models. The selected vector set based on each fault model is then evaluated for its coverages for other fault models. Our intention is to show that : (1) The vectors selected based on the LSAF or PSAF models usually fail to detect many GSAFs that can be detected if specifically targeted in the vector selection process. (2) The LSAFs and PSAFs that are detectable can usually be detected by the vectors selected based on the GSAF model. In other words, if the quality of a test set is measured in terms of its coverages for LSAFs or PSAFs, the selection based on the GSAF model will not cause loss of quality. On the other hand, if the quality is measured by its GSAF coverage, test quality will be significantly raised by specifically targeting GSAFs.

The vector selection algorithm we used is based on the one suggested in [6]. Table 6 shows the comparison of the fault coverages of the selected test vectors under different fault models. The maximum number of vectors (*VMAX*) is set to 20. The given test vector set for selection used in the experiment is generated by an ATPG procedure to be described in Section 4.

Three major columns labeled as *LSAF, PSAF* and *GSAF* show the vector selection results based on these three different fault models. For each vector set, the fault coverages are measured with respect to these three fault models. The fault coverages are labeled as *LFC, PFC and GFC* for LSAFs, PSAFs and GSAFs respectively.

For vectors selected based on LSAFs or PSAFs, their GFC tends to be lower than the LFC and PFC. Especially for circuits such as s382 and s400, the GFC is 40% lower than its LFC and PFC. On the other hand, the fault coverages of vectors selected based on GSAFs have consistently higher GFCs while maintaining high LFCs and PFCs.

Each fault coverage in Table 6 is calculated as *Det* / (*NF* - *UT*) where *Det*, *NF* and *UT* are the number of detected faults, total faults and untestable faults respectively. For

Table 6: Fault Coverages for different models

Cir.	LSAF		PSAF		GSAF		
	LFC	GFC	PFC	GFC	GFC	LFC	PFC
s298	98.9	71.5	98.9	87.9	98.9	98.9	98.9
s344	95.8	91.3	95.8	95.5	95.8	95.8	95.8
s349	98.8	94.7	98.8	98.8	98.8	98.8	98.8
s382	96.8	54.1	96.0	57.3	88.7	90.5	91.0
s386	95.2	94.9	95.7	95.5	95.5	95.5	95.5
s400	96.8	51.5	96.5	55.5	88.8	92.0	92.0
s420	98.8	95.0	97.9	95.0	97.9	98.3	97.9
s444	97.5	51.1	96.6	55.0	89.1	92.3	91.6
s526	92.8	61.2	93.8	62.7	82.5	88.0	88.6
s641	92.1	91.9	92.8	92.8	92.6	92.6	92.6
s713	94.3	93.3	93.9	93.9	93.7	93.7	93.7
s820	85.7	85.4	86.9	85.5	84.9	85.4	85.3
s832	86.6	85.7	86.8	85.4	84.7	84.8	84.9
s838	98.0	96.2	98.0	95.9	98.0	98.0	98.0
s953	95.5	95.5	95.5	95.5	95.5	95.5	95.5
s1196	91.4	91.4	91.4	91.4	91.4	91.4	91.4
s1238	90.5	90.5	90.5	90.5	90.5	90.5	90.5
s1423	88.8	83.3	85.8	83.9	84.5	88.0	84.9
s1488	93.4	91.7	93.0	92.1	92.6	93.4	92.8
s1494	92.9	92.0	93.3	92.5	91.9	92.3	92.1
s5378	80.5	76.0	79.4	76.7	80.1	80.7	80.5
Ave.	93.4	82.8	93.2	84.7	91.3	92.2	92.0

the untestable faults, we claim the following lemma.

Lemma 1 *If a PSAF-0 (1) or LSAF-0 (1) at signal s is untestable, the GSAF-0 (1) at signal s is also untestable.*

The untestable PSAFs are identified by STG3 running in the I_{DDQ} test mode [2] and its number is used for *UT* in these experiments.

Lemma 2 *If a PSAF-0 (1) or LSAF-0 (1) at signal s is not detected by a test set T, the GSAF-0 (1) at signal s is not detected by T. On the other hand, if a GSAF-0 (1) at s is not detected by T, T may detect the PSAF-0 (1) or LSAF-0 (1) at s.*

The above lemma implies a better strategy for I_{DDQ} vector selection. We can target GSAFs to achieve the highest possible coverage for GSAFs. The test set is then simulated for LSAFs or PSAFs and the undetected LSAFs or PSAFs are identified. A second run of vector selection can be conducted to target the remaining undetected LSAFs or PSAFs.

4 Test Generation/Selection for GSAFs

In this section, we describe the ATPG and fault simulation issues for GSAFs. We modified a conventional sequential ATPG tool for the GSAF model.

A sequential ATPG program STG3 has been modified to generate I_{DDQ} vectors for PSAFs in sequential circuits under the every-vector I_{DDQ} test scheme [2]. Note that if a PSAF is untestable under the every-vector I_{DDQ} test scheme, the corresponding GSAF is untestable under the selective I_{DDQ} test scheme. Therefore, we can use the I_{DDQ} mode of STG3 to identify the untestable GSAFs. We further modify STG3 for test generation for GSAFs. In the the I_{DDQ} mode, STG3 assumes every gate output as a primary output and one fault is selected randomly and targeted. The generated test sequence is then simulated to identify the faults which are accidentally detected by the test sequence. This process continues until all faults are detected or a CPU time limit is reached. For GSAFs, we modify the flow as follows.

Fault Simulation: The generated test sequence is evaluated by the fault simulator with two modifications : (1) Based on the GSAF model instead of the PSAF model. (2) For those time frames where I_{DDQ} is not measured, internal gate outputs are not assumed as primary outputs. The parallel fault simulation technique [1] is used for fault simulation. Moreover, we use a screening technique to eliminate unnecessary simulation for many faults. Fault-free simulation is first performed for the test sequence. Note that based on the logic simulation results, the fault detection for LSAFs can be determined. Furthermore, by Lemma 2, if a LSAF is not detected, the corresponding GSAF is not detected either. Therefore, based on the logic simulation results, a large number of GSAFs not detected by the given test sequence can be identified and removed from actual fault simulation.

Test Vector Generation and Selection: For a target fault, we use STG3 in the I_{DDQ} mode without modification to generate a test sequence. We then attempt to identify the most effective vectors from the generated test sequence for current measurement. Based on the GSAF-based fault simulation of the sequence, We identify the number of the faults detected by each vector in the sequence and select the vector which detects the largest number of GSAFs. Only the faults detected by the selected vector are considered as *detected* and are removed from the fault list. The additional vector is selected from the current test sequence if the number of the detected faults by the vector exceeds a threshold. The threshold used is similar to the one used in QUIETEST : $F/VMAX$ where F is the number of remaining undetected faults [5]. This additional vector selection process continues until no more test vectors can detect more than $F/VMAX$ undetected faults. After the selection process, a new target fault is selected and the next test sequence is generated for vector selection.

The following steps summarize our test vector generation and selection process.

Step 1: Identify the untestable GSAFs using STG3 based on the PSAF model. Remove the identified untestable faults from the fault list.

Step 2: Select a target fault and run STG3 in the I_{DDQ}

mode to generate a test sequence for it.

Step 3: Logic simulate the generated test sequence to identify a subset of undetected GSAFs.

Step 4: Fault simulate the sequence for the remaining GSAFs. Select the vector which detects the largest number of remaining faults.

Step 5: Update the fault list by removing the faults detected by the selected vector. Also update the number of detected faults of the remaining vectors and re-sort the remaining vectors with respect to the number of detected faults. If the vector in the top of the re-sorted vector list detects more than $F/VMAX$ faults, select the vector and repeat step 5. If not, a new target fault is selected and a new set of the vectors is generated.

Step 6: Repeat Steps 2 - 5 until all faults are detected, the target fault coverage is achieved or the number of selected vectors exceeds *VMAX*.

5 Experimental results

The test generation algorithms have been implemented in C. The ISCAS89 sequential benchmark circuits [8] were used to evaluate the performance of the proposed method.

Table 7 presents the results of test generation. The target fault coverage is set to 95%. Column NV_{NC} is the length of the vectors generated by STG3 under I_{DDQ} option where I_{DDQ} is assumed to be measured at every vector. We further selected the effective vectors from them using the QUIETEST vector selection strategy [5]. In this selection strategy, a vector is selected for I_{DDQ} measurement if it detects at least one undetected fault. This method gives some vector compaction without losing GSAF coverage. Column NV_C shows the number of the vectors selected for I_{DDQ} measurement. We use this number as *VMAX* for ATPG. Since *VMAX* affects the final result of our ATPG program, it is important to set *VMAX* properly when there is no clear limitation on the number of selected vectors. As shown in this table, our program selects fewer test vectors for most of the benchmark circuits.

Table 7: Results of test generation for GSAFs

Cir.	NF	UT	STG3			Proposed	
			FC	NV_{NC}	NV_C	FC	NV
s298	308	27	95.7	48	23	95.7	19
s344	342	7	95.2	29	20	95.8	17
s349	350	9	96.5	31	20	96.5	17
s382	399	20	95.5	306	44	95.5	35
s386	384	32	95.7	57	35	96.0	30
s400	424	24	95.3	665	49	95.3	36
s420	430	190	97.1	35	18	97.1	16
s444	474	32	95.5	298	47	95.5	35
s526	555	57	95.4	1256	70	95.4	46
s641	467	49	95.2	50	38	95.2	40
s713	581	73	95.3	51	40	95.3	36
s820	850	2	95.1	166	79	95.1	63
s832	870	2	95.5	147	78	95.5	56
s838	857	466	95.9	34	17	96.7	10
s953	1079	748	95.2	15	15	95.5	12
s1196	1242	0	95.0	73	69	95.0	58
s1238	1355	12	95.2	74	67	95.2	62
s1423	1515	10	87.3	82	56	86.7	42
s1488	1486	4	95.1	77	45	95.3	34
s1494	1506	4	95.1	65	44	95.3	37
s5378	4117	303	92.2	492	224	92.2	171
Ave.	-	-	95.0	192.9	52.3	95.0	41.5

6 Conclusion

We propose a generalized stuck-at fault model for sequential circuits under the selective I_{DDQ} test scheme. The assumption on the logic value at the faulty signal will affect the faulty states and fault detection in future cycles. This phenomenon is thoroughly discussed and examples are given. The GSAF model makes pessimistic assumption on this effect and therefore tests targeting this fault model will cover a wider class of defects. The GSAF model presented in this paper only covers the defects within a gate, but the concept can be easily extented to other types of defects such as bridging faults.

We also presented a test vector generation and selection method for the GSAF model. We modify a conventional test vector generator and a fault simulator for sequential circuits for the GSAF model. We demonstrate that a high fault coverage for the GSAFs can be achieved using only a small number of selected I_{DDQ} vectors.

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