Dual Active Bridge based Battery Charger for Plug-in Hybrid Electric Vehicle with Charging Current Containing Low Frequency Ripple

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I. INTRODUCTION

Plug-in Hybrid Electric Vehicles (PHEVs) have gained high popularity recently due to the environmental friendliness and the growing price of the fossil fuel. The batteries of PHEVs can be restored to full charge by easily connecting a plug to the electric wall socket if the battery charger is on-board. As such, achieving high efficiency and small size for the on-board battery charger is very important because it will help to improve overall performance of the PHEV. In the ADEPT program of ARPA-E[1], HRL Laboratories are using gallium nitride (GaN) semiconductors to create battery chargers for hybrid electric vehicles (HEVs) that are more compact and efficient than traditional EV chargers. Wide band-gap material, such as Gallium Nitride (GaN), theoretically outperforms Si in such aspects including switching speed and efficiency [1, 2]. Since GaN devices enable higher switching frequency (up to MHz) in the battery charger design, smaller passives can be expected and thus an increase in the power density.

On the other hand, the battery charger topology will inevitably be a single phase AC/DC converter since the battery need to be charged with household electrical outlet. As Power Factor Correction (PFC) is usually required at the AC side, the AC input voltage and current will be sinusoidal, so that input power will pulsate at two times line frequency. This pulsating power usually is stored in a capacitor which has high capacitance, high volume, and also low life time if electrolytic capacitor is used. It can be proved that the size of the DC link capacitor is mainly determined by the current ripple at two times line frequency instead of the switching ripple [3], thereby the DC link capacitors may become the major power density barrier of the battery charger even if GaN devices are used.

Researchers have made a lot of effort to reduce the DC link capacitance to avoid electrolytic capacitor for longer lifetime and meanwhile keep high power density. Ripple cancellation [3-5] can be implemented to reduce the DC link capacitor size, but auxiliary circuitry implemented increases complexity. The way of distorting input current [6,7] in LED driver design to eliminate large DC link electrolytic capacitor is not applicable in PHEV battery charger because of the tighter power factor requirement. Storing two times line frequency ripple energy both in the inductor and capacitor actually reduces the power density [8].

If the battery is able to take the low frequency charging current ripple, the DC link capacitance will be significantly reduced because the capacitors only need to filter the current ripple at the switching frequency. For electric vehicle application, lithium-ion batteries are dominant in the selection of powertrain energy storage. Studies show that the performance of lithium-ion batteries do not deteriorate much with the current ripple at two times line frequency[9,10]. Investigation on the $L_iC_oO_2$ lithium-ion battery cells shows that the cells do not suffer from extra capacity decay contributed by the current ripple if the ripple frequency is

higher than 10 Hz [9]. Short term evaluation on the performance of Lithium Iron Phosphate (LFP) batteries are carried out in [10]. The results show that the 200% current ripple causes a light but noticeable increase in the heat generation of battery cells.

This paper proposes a battery charging scheme which allows the ripple current flowing into the battery to reduce the DC link capacitor volume. The converter topology is selected as Full Bridge (FB) AC-DC plus Dual Active Bridge (DAB) DC-DC. Section II quantifies the volume reduction on the DC link capacitor with the proposed charging scheme. Since the proposed charging scheme mostly influences the operation of the DC-DC stage, section III introduces the operation principles of DAB with sinusoidal charging current, and based on that the controller design and implementation are described in section IV. section V shows the experimental results of the prototype. Section VI concludes the paper.

II. Proposed Sinusoidal Charging Scheme

The specifications of the typical battery charger are listed in Table I. The required capacitance for a single phase AC-DC converter can be derived as [3]

$$C_{dc} > \frac{V_{ac} I_{ac}}{\omega \cdot \Delta V_{dc} \cdot V_{dc}} \tag{1}$$

in which V_{ac}, I_{ac} are the RMS values of line voltage and current, respectively, ω is the line frequency in rad/s, V_{dc} is the DC link voltage, and ΔV_{dc} is the required peak-to-peak value of the DC link voltage ripple. With the specifications given in Table I, the resultant DC link capacitance would be 912 μF if 12% ripple of 400V DC link voltage is assumed. Considering lifetime and reliability, twelve 80 μF film capacitors from the high density series B32778 of EPCOS are needed, which leads to total volume of 56.8 in^3. In [1] the target for high-density integrated power converter above 3 kW is at least 150 W/in^3, and the expected total volume for a 6.6 kW unit to be 44 in^3. The capacitor volume itself is 1.3 times of the total volume budget.

If the less reliable electrolytic capacitors are allowed, the selection of capacitor will be determined by ripple current in the capacitor. If all the ripple power at two times the line frequency is stored in the capacitor, the current ripple can be estimated by

$$I_{Cdc(pk-pk)} \approx \frac{V_{ac} I_{ac}}{\sqrt{2} \cdot V_{dc}} \tag{2}$$

The resultant current ripple from (2) is 12.3 A. As such, six 560 µF electrolytic capacitors from the miniaturized series TS-UQ of Panasonic, with the ripple current rating of 2.82 A at 120 Hz, will lead to total ripple current rating of 16.9 A. The derating ratio in this case is 75.7% for lifetime consideration. The total box volume is 16.5 in^3 and equivalent to 37.5% of the total volume budget. Note that the analysis above only take the low frequency ripple current into account, in fact the high frequency current from both the AC-DC stage and DC-DC stage also flows into the DC link capacitors. This will lead to higher required ripple current rating and larger capacitor bank. In all, even with electrolytic capacitors, the DC link capacitor bank already occupies a large proportion of the total volume budget and leaves quite limited room for all the rest components including magnetics, heatsink, etc.

TABLE I. PHEV Battery Charger Specifications

Input voltage	240Vac
Battery voltage	270V – 430V
Power rating	6.6 kW
DC link voltage	400V

However, if all ripple power flows into the batteries, the charging current will behave in a sinusoidal waveform with a DC bias as

$$\begin{aligned} i_o(t) &= p_{in}(t)/V_{bat} = V_{ac} I_{ac}/V_{bat} \cdot [1-\cos(2\omega t)] \\ &= I_o(1-\cos 2\omega t) = 2I_o \sin^2(\omega t) \end{aligned} \tag{3}$$

The ripple power at two times the line frequency in (3) will compensate the ripple power at the input side, thus ideally the DC link capacitors to store this ripple power can be eliminated. In this paper, charging with current in the form of (3) is named as sinusoidal (current) charging. The battery charger contains one Full Bridge (FB) AC-DC stage and one Dual Active Bridge (DAB) DC-DC stage, as shown in Figure 1. DAB is a promising topology especially for isolated and bi-directional power conversion. It has many benefits, such as Zero Voltage Switching (ZVS) for both primary and secondary bridges, small passive sizes, utilization of parasitic and fixed switching frequency[11,12]. In this configuration, the FB AC-DC stage is controlled to realize power factor correction and DC link voltage regulation, and the DAB DC-DC stage is used to achieve the sinusoidal charging. Since charging current waveform mainly influences the DC-DC stage, this paper will focus on the analysis of the DAB DC-DC stage with sinusoidal current charging.

III. Dual Active Bridge (DAB) Operation with Sinusoidal Charging Current

A. DAB Characteristics with Sinusoidal Output Current

Different modulation schemes exist for DAB. In this paper, phase shift modulation (PSM) is used to demonstrate the concept of sinusoidal charging for simplicity. In phase shift modulation of DAB, each device is driven with 50% duty cycle and the two phase legs at the same side have exactly 180 degree phase shift, so that both full bridge output voltages (V_p and V_s) are 50% duty cycle square wave. These two output square waves have and only have V_{dc} and – V_{dc} values, which show the characteristic of two level modulation. Then the average output current can be derived as (4) as deducted in

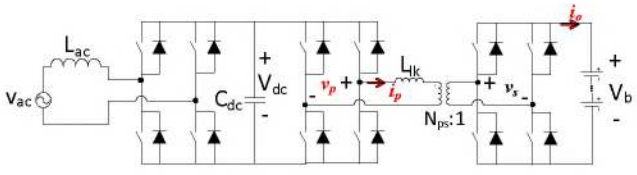

Figure 1. Battery charger topology with a Full Bridge (FB) AC-DC stage plus a Dual Active Bridge (DAB) DC-DC stage

[11].

$$I_o = \frac{N_{ps} V_{dc} \varphi(\pi - \varphi)}{2\pi^2 f_s L_{lk}} \tag{4}$$

in which N_{ps} is transformer turns ratio from primary to secondary sides, V_{dc} is the DC link voltage, φ is the phase shift angle, f_s is the switching frequency, V_b is the battery voltage , L_{lk} is the leakage inductance of DAB transformer. We can see that DAB with phase shift modulation is a current source in nature, and average output current is not influenced by the battery voltage. Considering (3) and (4), the steady state value of phase shift within the line period can be solved as (5)

$$\varphi(t) = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_s L_{lk} I_M (1 - \cos 2\omega t)}{N_{ps} V_{dc}}}\right) \tag{5}$$

The phase shift shown in (5) is the steady state phase shift when sinusoidal charging is achieved.

B. *DAB ZVS Range with Sinusoidal Output Current*

Soft-switching is important to reduce switching loss, especially for converter with a high switching frequency and high power density. For power MOSFET, zero voltage switching (ZVS) is usually preferable. ZVS always means the device turning on transition is initiated by the conduction of body diode or anti-parallel diode. In the ideal case, the influence of device output capacitor and transformer magnetizing inductance are ignored. Hence, ZVS condition is only determined by the current direction before the device is turned on. Therefore, the inductor current at the device transition instants t_0 and t_1, as shown in Figure. 2, should satisfy the following inequalities to achieve ZVS for primary bridge and secondary bridge, respectively.

$$i_p(t_0) < 0 \tag{6}$$

$$i_p(t_1) > 0 \tag{7}$$

When (6) and (7) are satisfied, the other half-cycle ZVS conditions automatically hold because of the half-cycle symmetry of the inductor current waveform.

Making the two current items in (6) and (7) equal to zero yields the PSM DAB ZVS boundary which divides the entire operating range into three regions, as shown in Figure 3. The

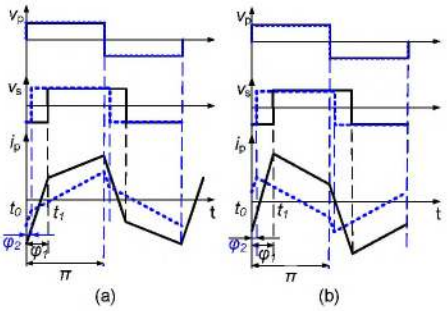

Figure 2. DAB waveforms with phase shift modulation. (a) At $V_{dc}>N_{ps}V_b$, DAB operating condition changes from Region 1 to Region 2 when phase shift angle change decreases from φ_1 to φ_2. (b) At $V_{dc}<N_{ps}V_b$, DAB operating condition changes from Region 1 to Region 3 when phase shift angle change decreases from φ_1 to φ_2.

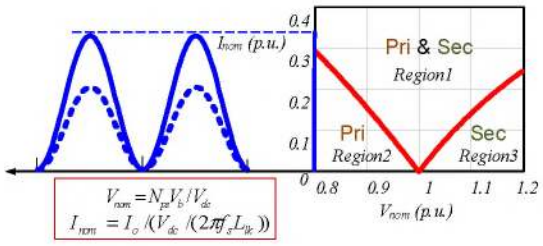

Figure 3. DAB ZVS analysis with phase shift modulation

horizontal axis is the normalized voltage, which is defined as

$$V_{nom} = N_{ps} V_b / V_{dc} \tag{8}$$

The vertical axis represents the normalized output current, defined as

$$I_{nom} = I_o / (V_{dc} / (2\pi f_s L_{lk})) \tag{9}$$

Therefore, this chart demonstrates the ZVS characteristic among entire DAB operating conditions for different input voltages, output voltage and output current. If we examine the case of $V_{dc} > N_{ps}V_b$ in Figure 2(a) we can see that DAB is operating with both bridges achieving ZVS when the output current is large enough. However, as the output current decreases, the phase shift angle changes from φ_1 to φ_2, the inductor current at t_1 becomes negative, which results in losing of ZVS on the secondary bridge. It is clear that with lower output current, the phase shift angle decreases from φ_1 to φ_2, DAB will eventually drop into hard switching region in which (7) does not hold any more and secondary bridge encounters hard switching. Corresponding to the ZVS boundary chart in Figure 3, DAB operating region changes from Region 1 to Region 2.

Similarly, in the case of $V_{dc} < N_{ps}V_b$ in Figure 2(b) initially the output current is high enough to keep both bridges switching at ZVS condition. When the output current decreases, the phase shift angle also changes accordingly from φ_1 to φ_2, thus the inductor current at t_0 becomes positive which violates (6), leading to hard switching on the primary bridge. In this case, the operating region changes from Region 1 to Region 3. From the above analysis, we can see that hard switching of the devices always happens due to the severe variation of the sinusoidal output current.

IV. CONTROL DESIGN AND IMPLEMENTATION OF BATTERY SINUSOIDAL CHARGING CURRENT

This section will focus on the influence of the sinusoidal charging in the control of the output current of the DAB. The target of the control strategy is to obtain the regulation of DAB output current in the form of (3). In order to achieve this, the first possible control strategy is the open loop control strategy based on the correspondence between the output current and phase-shift for the DAB, as quantified in (5). As the required phase-shift is solved based on the circuit parameters and required output current , this control strategy

would be the most desirable to use, as it allows a reduction of the computation time and the complexity of the control stage. It is clear that all of the circuit parameters in (5), such as leakage inductance L_{lk}, input voltage V_{dc}, etc., need to be quite accurate to derive expected output current values. Those parameters in (5) can be fine-tuned in the digital implementation of the control strategy to match with measurement results at certain operating point. For example, the input voltage V_{dc} and output voltage V_b are fixed as 100V and 90V, respectively, and the DAB output current values are measured at different phase shift. The data are collected and plotted as the purple curve in Figure 4. The parameters of the analytical expression in (5) are then tuned to match with this measured curve, which is plotted as the dotted line in Figure 4. It can be seen that the measured curve matches with fine-tuned analytical prediction curve only at high phase shift values, the match becomes worse when the phase shift approaches zero. The analytical prediction becomes even worse when the output voltage changed to 60V or 120V (red and blue curve in Figure 4). In other words, different current values are obtained from the same phase-shift applied to DAB at different conditions of the output voltage V_b, therefore it can be concluded that the analytical prediction based on (5) is not precise at all operating conditions. Even the fine-tuned analytical expression obtained above at 100V input voltage and 90V output voltage is implemented experimentally at the same operating conditions for sinusoidal charging, some degree of distortion still can be observed in the waveform of the output current, as shown in Figure 5. This distortion will consequently lead to the imbalance between the input and output ripple power, and the imbalanced power need to be stored in the DC link capacitor, which increase the DC link capacitance. Therefore open loop control cannot be used, and closed loop control is needed.

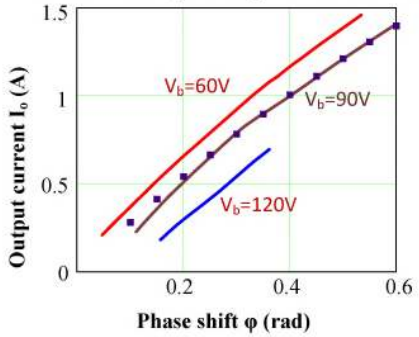

Figure 4. Relationship between DAB phase shift and output current on different operating conditions. Solid line: measurement; Dots: analytical prediction

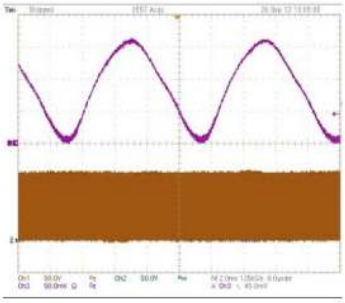

Figure 5. Sinusoidal charging with open loop control at V_{dc} =100V and V_b = 90V (2ms/div and 0.5A/div)

Now we consider build a closed current loop to regulate the output current of DAB to be in the form of (3). In the state of the art, a low bandwidth PI controller is normally used to control the DC charging current of the battery [13], [14], [15] and in [16], where a 20Hz current regulator is used. The main advantages of this implementation are good performance and simplicity. However, for this particular application, the sinusoidal charging of the batteries requires a control strategy with a bandwidth as high as possible, in order to obtain a high instantaneous power balance between the mains and the batteries, as explained in section II. This strategy will allow, as detailed previously, a DC-bus capacitance reduction and therefore a power density increase.

A digital control implementation has been chosen for the control stage of the two-stage (PFC and DAB) AC/DC converter due to the high flexibility and reliability, the possibility to synchronize the control of both stages, and ease of monitoring the control and the converter parameters. The block diagram of the control scheme of DAB can be seen in Figure 6. The phase shift to output current transfer function $G_{i\varphi}$ can be obtained as (10) by perturbation and linearization on (4)

$$G_{i\varphi} = \frac{V_{dc} N_{ps}}{\omega L_{lk}} \left(1 - \frac{2\Phi}{\pi}\right) \tag{10}$$

The output current is then filtered by a low pass filter (LPF) to attenuate the switching frequency noise. The current reference is given by (3). The DC value of the output current is given based on the charging current requirement and the phase information is obtained from phase lock loop (PLL) in the AC-DC stage. $H_i(s)$ is the current regulator to design.

It can be noticed in (10) that the transfer function from

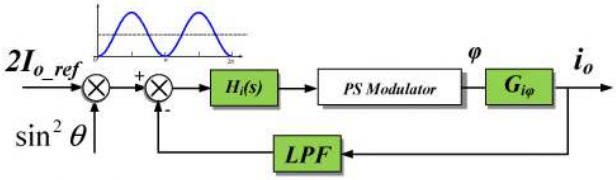

Figure 6. Block diagram of the control loop strategy

DAB phase shift to DAB output current behaves as a constant gain. Therefore, the main part of the dynamic behavior of the DAB will be determined by the low pass filter used to attenuate the high current ripple at the output to obtain the proper measurement of the output current. Depending on the order of the filter, the type of regulator that has to be used to obtain a high bandwidth and stable control loop is determined. If a first order filter is used, a PI regulator has to be used, as shown in Figure 7. It is also considered 1.2 kHz as the minimum cutoff frequency of the filter to avoid interferences in the sinusoidal current of twice the line frequency of 120Hz.

V. EXPERIMENTAL RESULTS

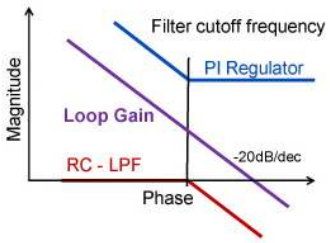

Figure 7. PI regulator design with a first order RC filter

The closed-loop control strategy in section IV is applied to a scale-down DAB converter with the input voltage at 100V and output voltage at 90V. The DAB inductor is 53.4 µH and the transformer turns ratio is 40:36. A first order filter and a PI controller have been chosen for the experimental validation of the closed loop operation as a compromise between a high bandwidth and a low computation time. Experimental waveforms for DC output current steps are shown in Figure 8 for V_{dc} = 100V and V_b = 90V.

Figure 9(a) shows the experimental closed loop charging current of the DAB for closed loop operation with a 5.5 kHz bandwidth PI controller where it can be seen the good sinusoidal waveform obtained. Compared to the waveform in Figure 5, the sinusoidal current has lower distortion with closed loop control than that of open loop control. At other output voltage Vb, the waveform of the output current for open loop control will be worse due to inaccuracy of analytical prediction, as discussed in section IV. Therefore, it is validated that the closed loop control scheme is more suitable to control the sinusoidal current charging of the battery.

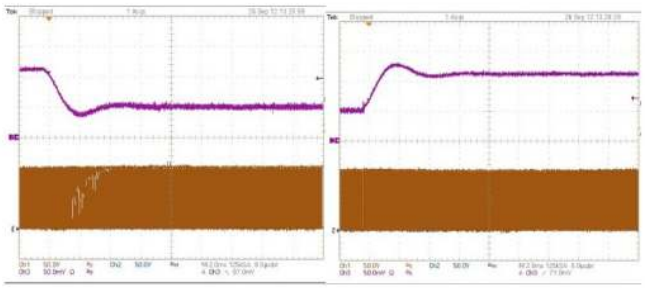

Figure 8. Closed loop DC charging current step up and down validation test 0.5A/div 2ms/div

Figure 9(a) shows the DAB inductor current and output current throughout entire 120 Hz sinusoidal cycle, which indicates that sinusoidal charging is achieved. Figure 9(b) and Figure 9(c) show the zoom-in waveforms at the peak and valley of output current waveform, respectively. We can observe that the drain-to-source voltage waveforms for both full bridges are clean from resonance at current peak, because they are all turned on with ZVS. However, at current valley, switches in secondary full bridge lose ZVS because ringing appears at the turn-off edge. It verifies that DAB converter always suffers from hard switching at the valley of sinusoidal current waveform, which corresponds to the description of Region 2 as analyzed in section III.

Full system test with FB AC-DC stage and DAB DC-DC stage is carried out. The input AC voltage is 60 V (rms), the output voltage 90 V, the DC link voltage is regulated as 120 V, and the average output current is 1 A. An electronic load in constant voltage mode with a paralleled capacitor bank is used to emulate the battery. The test waveform is shown in Figure 10. We can see that the power factor correction is achieved at

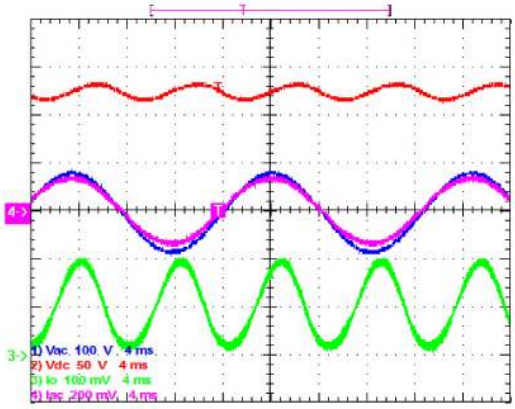

Figure 10. Full system sinusoidal charging at V_{ac} = 60V, V_b = 90V, $I_{o(avg)}$ = 1A. Red: DC link voltage 50 V/div; Blue: AC input voltage 100 V/div; purple: AC input current 4 A/div; Green: battery charging current 1 A/div

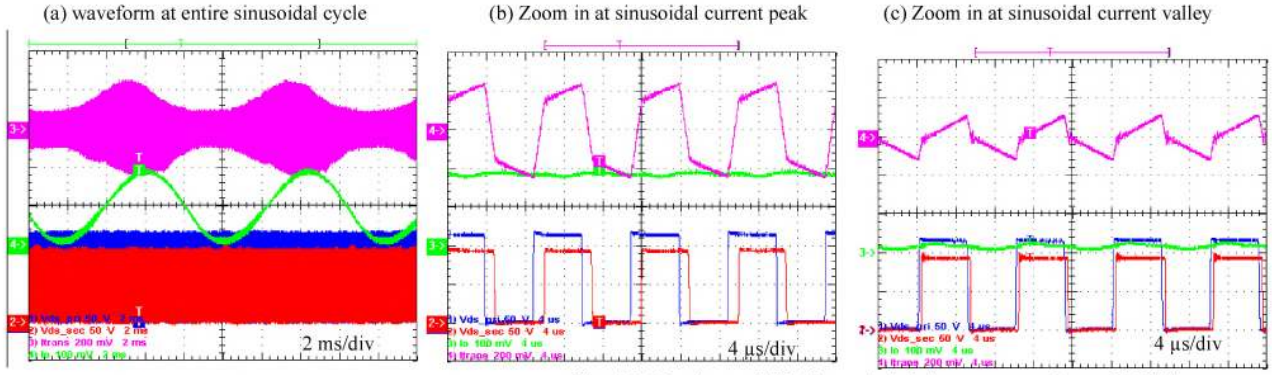

Figure 9. Closed loop sinusoidal charging at V_{dc} =100Vand V_b=90V

the AC side. The DC link voltage is well regulated. The charging current is sinusoidal and synchronous with the AC voltage. Note that a set of non-idealities actually prevent the complete ripple cancellations, so there is still ripple at the DC link voltage. Among these, the most relevant ones are the current control delay, which give a phase-shift between the reference and the actual current.

VI. Conclusion

In PHEV battery charger, if current ripple at two times line frequency is allowed into the battery, theoretically the DC link capacitor volume can be significantly reduced compared to pure DC current charging, which gives potential to achieve very high power density. The operation of dual active bridge (DAB) converter under sinusoidal charging is analyzed. It is found that due to variation of charging current, switches in DAB always suffer from hard switching at different battery voltages, which is verified by experimental results on a scaled-down low power prototype. Two ways of sinusoidal charging control strategies of DAB are proposed and implemented, and it is proved that closed loop current control outperforms the open loop control. The test on full system including both full bridge AC-DC stage and DAB DC-DC stage verifies the feasibility of a battery charger with sinusoidal charging. Synchronization between the charging current and the line voltage indicates the balance of the ripple power at the two times line frequency. The DC link capacitor volume can be highly reduced, which enables the design of battery chargers with very high power density.

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