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Dual-Gate Thin-Film Transistors, Integrated Circuits and Sensors

Mark-Jan Spijkman, Kris Myny, Edsger C. P. Smits, Paul Heremans, Paul W. M. Blom, and Dago M. de Leeuw*

The first dual-gate thin-film transistor (DGTFT) was reported in 1981 with CdSe as the semiconductor. Other TFT technologies such as *a*-Si:H and organic semiconductors have led to additional ways of making DGTFTs. DGTFTs contain a second gate dielectric with a second gate positioned opposite of the first gate. The main advantage is that the threshold voltage can be set as a function of the applied second gate bias. The shift depends on the ratio of the capacitances of the two gate dielectrics. Here we review the fast growing field of DGTFTs. We summarize the reported operational mechanisms, and the application in logic gates and integrated circuits. The second emerging application of DGTFTs is sensitivity enhancement of existing ion-sensitive field-effect transistors (ISFET). The reported sensing mechanism is discussed and an outlook is presented.

1. Introduction

Conventional silicon CMOS integrated circuits, *e.g.* microchips, are processed in the substrate itself, typically Si wafers. Thin-film transistors (TFT) however are field-effect transistors manufactured by depositing thin films of semiconducting and dielectric materials, as well as the electrical contacts, on a carrier substrate.[1] Applications are in the field of high-volume large-area electronics where numerous discrete transistors are required on low-cost substrates. The most common substrate is glass, as the most important application of thin-film transistors is as pixel engine in active matrix liquid crystal displays (AM-LCD) and recently in organic light emitting diode (AMOLED) displays. As compared to passive matrix addressing, the small charge needed to drive a single pixel reduces the write time of a screen and allows for, optically, smooth frame rates. In addition TFTs are used in image intensifiers for medical radiography. When applied on a mechanically flexible substrate,[2,3] TFTs can be processed in a high volume roll-to-roll process and used in flexible displays,[4] RFID tags[5,6] and sensors.[7]

Besides glass, a variety of plastics has been used as carrier substrate. Depending on the type of substrate, deposition technologies such as plasma-enhanced vapor deposition (PECVD), sputtering, evaporation, spincoating and ink-jet printing are possible. Because the substrate is generally incompatible with high annealing temperatures, processing of TFTs has to be performed at relatively low temperatures.

TFTs can be made from a wide variety of semiconductors. A common material is amorphous-Si (*a*-Si:H), but compound semiconductors such as CdS, metal oxides as ZnO and organic molecules like pentacene have also been used. The main advantages of organic semiconductors are their easy processing, *e.g.* spincoating, ink-jet or silk-screen printing without a temperature hierarchy, and their mechanical flexibility.

A transistor acts as an electrical switch of which the resistance depends on the voltage applied to the gate electrode. Transistors made in a bulk semiconductor operate in inversion: source and drain diodes are formed in the semiconductor, and the gate electrode is biased such as to invert the bulk semiconductor at its interface with the gate dielectric, effectively creating a conductive path between the source and the drain.

A thin-film transistor, however, operates in accumulation. Since the semiconductor is very thin, it can be fully depleted under the gate to switch off the transistor (depletion regime). Most semiconductors are unipolar, they can only support one type of charge carrier. Hence the transistor can be depleted, inversion does not occur. Only in special cases inversion is obtained. When the gate is biased towards depletion, then a conductive channel of carriers with opposite polarity is formed. Such inversion operation is usually unwanted, and will not be used in the present paper, but can be exploited in some circumstances in so-called ambipolar transistors.[8,9]

When the gate is biased towards accumulation, a conductive channel is formed between source and drain (formed as Ohmic

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contacts to the semiconductor film). The channel is formed initially by the intrinsic conductivity of the (unintentionally) doped semiconductor, and later by the accumulated charge carriers.

The threshold voltage[10] (V_{th}) of a thin-film transistor is the gate bias at which the transistor switches between the low current depletion regime and the high current accumulation regime. For any envisioned application, control of the threshold voltage is essential. For logic gates, the threshold voltage determines the trip point, which is the input bias at which the gate inverts the output signal. For sensing applications, the threshold voltage signifies the bias at which the largest change in current occurs, *i.e*. the point of the highest sensitivity.

For standard Si CMOS transistors, the threshold voltage (at the onset of inversion) can be accurately set by the amount of doping applied by ion implantation.[11,12] In thin-film transistors local doping of individual transistors in a circuit is not an option. To get around this constraint and to externally set V_{th}, several options have been published such as level shifters in circuits,[5] modification of the dielectric to set the interface charge[13] or the use of a gate metal with a specific work function.[14] An alternative solution is to set V_{th} is a dual-gate transistor, schematically depicted in the top right inset of **Figure 1**. A dual-gate transistor is comprised of a bottom gate and its dielectric, the semiconductor with source and drain electrodes and finally the top gate and top dielectric. The second gate electrostatically modifies the charge carrier distribution in the channel accumulated by the first gate. Hence the second gate can accurately set V_{th}, but at the cost of an extra electrical contact in the circuit and of additional processing steps during fabrication.

One of the first dual-gate thin-film transistors (DGTFT) was based on CdSe and reported in 1981 by Luo et al.[15] for use in flat panel displays. In 1982, Tuan et al.[16] demonstrated an *a*-Si:H based DGTFT, which was reproduced by Kaneko et al. in 1992.[17] In 2005, the first organic DGTFT, based on pentacene was reported by Cui and Liang.[18] Various papers based on a range of other organic semiconductors were published in the following years. In 2009, ZnO and "InGaZnO" DGTFTs were demonstrated by various groups from Korea.[19–21] Finally, in 2010 the group of Avouris presented graphene based DGTFTs.[22,23] Advantages reported in almost all papers on DGTFTs are a steeper subthreshold slope and an increased gate modulation, with a higher on-current and lower off-current due to decreased leakage current[24] and enhanced device stability.[17]

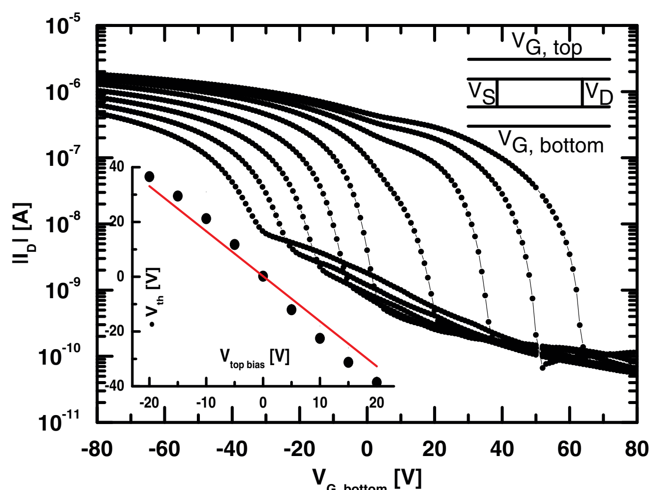

Figure 1. The absolute value of the drain current of a dual-gate transistor is presented on a semi logarithmic scale as a function of the bottom gate bias. The top gate bias is varied from left to right in steps of 5 V starting at +20 V to −20 V. The inset graph shows the measured (circles) and calculated (line) threshold shift. The other inset is a schematic of a dual-gate transistor. The transistor consists of a Si bottom gate with thermally annealed SiO_2 as the bottom dielectric, a spincoated layer of *p*-type polytriarylamine on top of which the top dielectric, poly-isobutyl methacrylate was applied followed by an evaporated Au top gate. Reproduced with permission.[30] Copyright 2008 American Institute of Physics.

Amorphous Si (*a*-Si:H) is an intrinsic *n*-type semiconductor. The advantage for large area electronics is the ability to produce thin layers by low-cost processing as PECVD in combination with a low temperature regime on plastic films. The disordered configuration of *a*-Si:H makes it difficult to accurately set V_{th}, even with doping. Employing a dual-gate layout in *a*-Si:H can therefore be advantageous.

The first organic DGTFT was reported in 2005 by Cui and Liang.[18] During the same year, Iba et al.,[25] Gelinck et al.,[26] Chua et al.[27] and Morana et al.[28] published papers on dual-gate transistors. Since then, numerous papers on organic DGTFTs have appeared in literature. Typical semiconductors used are pentacene, poly(9,9-dioctylfluorene-co-)phenylene-(N-4-sec-butylphenyl)-iminophenylene) (TFB) and [9,9]-dioctylfluorene-*co*-bithiophene (F8T2). Dielectrics are commodity insulating polymers like divinyltetramethyldisiloxanebis (benzocyclobutene) (BCB), parylene, polyimide and polyvinylphenol (PVP). The multilayer stacks can be quickly manufactured by spincoating, making organic materials ideally suited for dual-gate transistors. For solution processing, it is important that the solvents of consecutive layers are orthogonal, *i.e*. the solvent of the next layer should not dissolve the previous one. Both rigid substrates such as Si/SiO_2 and glass and flexible substrates like polyethylenenaphtalate and polyimide were used.

In this paper, the field of thin film organic dual-gate transistors is reviewed. We summarize in section 2 the reported operational mechanisms. The threshold voltage can be set as a function of the applied biases. The effective threshold shift depends on the ratio of the capacitances of the two gate dielectrics. The application of DGTFTs in logic circuits is reviewed in section 3. Besides setting the threshold voltage to improve circuit performance, DGTFTs are demonstrated as self-contained logic gates. An overview of DGTFTs as sensors is given in section 4. Amplification of small changes in the surface potential makes DGTFTs attractive for biosensing applications for which currently ion-sensitive field-effect transistors (ISFETs) are used. The amplification is due to the capacitive coupling between the two gate dielectrics. A summary and outlook is presented in section 5.

2. Discrete Dual-Gate Transistor

The schematic layout of a dual-gate transistor is shown in the top right inset of Figure 1. From top to bottom, the transistor consists of the top gate, top insulator, the semiconductor with source and drain electrodes, the bottom gate dielectric and

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finally the bottom gate. Both gates can deplete or accumulate charges in the semiconductor. The accumulated charges are concentrated in the first nanometers at the dielectric-semiconductor interface.[29] Hence, when the semiconductor thickness is larger than ten nanometers, two separate channels are formed, one at the bottom gate dielectric and one at the top gate dielectric. The current in the DGTFT at a given source-drain bias is determined by the interplay between the biases on the two gate electrodes.

A typical example of an organic *p*-type DGTFT is presented in Figure 1. The linear transfer characteristics measured at a drain bias of –2 V are presented in Figure 1 for top gate biases ranging from –20 V to 20 V in steps of 5 V. The transfer curve for 0 V top gate bias shows that the transfer curves systematically change with the applied top bias. The origin of the shift and the relation with the capacitive coupling can be understood from electrostatics.[26,28,30] For a top bias of 0 V, the middle transfer curve in Figure 1, there is no charge accumulated at the top gate. The effect of the top gate on the transistor is negligible when grounded. The DGTFT acts as a conventional single-gate transistor and charges are only accumulated by the bottom gate at the bottom interface. The drain current and the threshold voltage are the same as for a conventional single gate thin-film transistor.

For a positive top gate bias, the curves on the left in Figure 1, there is an effect on the transistor behavior. PTAA is a unipolar *p*-type semiconductor, hence electrons cannot be accumulated. PTAA is unintentionally doped, so there is no screening of the top gate bias by the semiconductor. The net effect is that the accumulated charges in the bottom channel are depleted. The amount of the depleted charges per unit area depends on the top gate bias (V_{top}) and is given by:

$$Q = C_{top} V_{top} \tag{1}$$

where C_{top} is the top gate capacitance per unit area. Mobile charge carriers in the bottom channel are accumulated by the bottom gate, but depleted by the top gate. To compensate for the top gate bias and to attain the original drain current at 0 V top gate bias, the bottom gate bias needs to be increased. Effectively the transfer curve is shifted in Figure 1 to the left.

When we apply the opposite polarity, a negative top gate bias, the top gate channel is formed. The top gate bias is fixed, so an additional constant drain current is added to the transfer curve of the bottom gate. The top channel is only depleted by the bottom gate at a positive bias beyond the threshold voltage of the bottom channel. Effectively, the entire transfer curve is shifted to the right.

The shift in V_{th} can be quantified from the total charge (Q_{total}) induced by the two gates from:

$$Q_{total} = C_{bottom} V_{bottom} + C_{top} V_{top} \tag{2}$$

At the threshold voltage of the DGTFT the total induced charge is zero, which implies that $C_{bottom} V_{bottom} = -C_{top} V_{top}$. If we assume that the top gate is fixed and the bottom gate is swept, the shift in threshold voltage is given by:

$$\Delta V_{th,bottom} = -\frac{C_{top}}{C_{bottom}} \Delta V_{top} \tag{3}$$

For the situation where the top gate is swept, Eq. [3] can simply be inverted. Eq. [3] is a general formula and holds for both unipolar *p*-type and *n*-type dual-gate transistors. The factor C_{top}/C_{bottom} is the capacitive coupling, *i.e.* the measure by which the V_{th} of the bottom gate can be modified as a function of gate bias on the top gate. For the transfer curves in Figure 1, the shift in V_{th} as a function of the applied top bias is shown in the bottom left inset. For a top gate bias of 20 V, the threshold was shifted by about 40 V. The capacitive coupling was then roughly two.

A complication has been reported for organic semiconductors.[31] The depleted part of the semiconductor forms a capacitor in series with the gate dielectric. This semiconductor capacitance cannot be ignored when the semiconductor capacitance is comparable to that of the gate dielectric. Then, in Equation (3), C_{top} and C_{bottom} have to be replaced by:

$$C_{eff} = \left(\frac{1}{C_{ins}} + \frac{1}{C_{sc}}\right)^{-1} \tag{4}$$

for the channel that is in depletion.

The transfer curves for a negative top gate bias, on the right in Figure 1, exhibit a distinct hump in the transfer characteristics. The steps in the pinch-off voltage for negative top bias are also significantly larger than the steps for positive top gate bias. Maddalena et al. use Equation (4) to explain the hump in the transfer curves and derive two distinct regimes for the threshold voltage shift.[31] Therefore, the shape of the transfer curves in Figure 1 likely has the same origin.

The shift in threshold voltage as a function of the capacitive coupling is generally observed. Only Gelinck et al. observed that the threshold voltage is not due to the formation of a second channel at the top interface. Precursor pentacene was used as the semiconductor. The surface is rough, which led to a field-effect mobility which was a factor of 10^4 lower than that of the bottom channel. Therefore, the top gate channel had a negligible influence on the drain current of the total device. Although the capacitive coupling is about unity, the accumulated charges in the top channel are immobile and do not contribute to the total current.

We note that most papers report as a common feature an increased on/off current ratio,[18,20,21,25–28] improved mobility,[18,28] and a steeper subthreshold slope.[18,20,26,28] Chua et al. report that dual-gate transistors can achieve a considerably deeper gate modulation than possible with single gating. Gelinck et al. also report the capability to provide a higher on current and a steeper subthreshold slope. The second gate effectively doubles the width of the channel, yielding a higher current. Additionally, the opposing gate improves the gate modulation by deeper depletion of the bulk semiconductor, yielding a steeper subthreshold slope.

The thickness of the charge accumulation layer is only several nanometers. DGTFTs with semiconductor thicknesses of more than about 10 nm therefore contain two channels which are spatially separated and can be tuned independently. A dual-gate transistor with a *p*-channel and an *n*-channel on opposite sides of a thick singe crystal of tetracene has been suggested to behave as a solid state injection laser.[32] However, for a thick semiconductor the channels operate independently and the claim has been retracted.[33] Upon reducing the semiconductor

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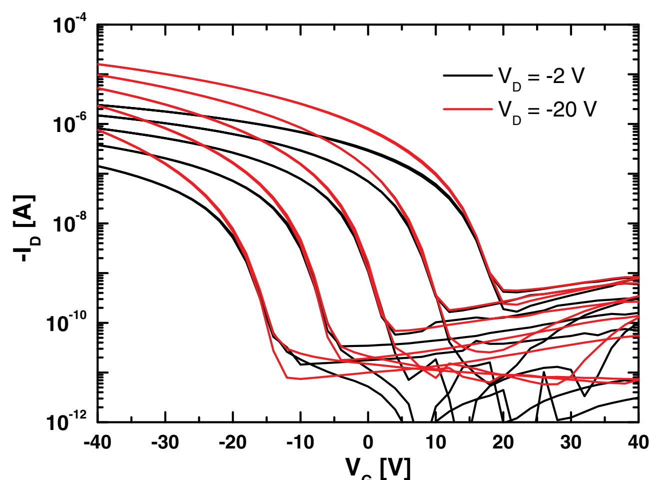

Figure 2. Drain current plotted as a function of the top gate bias of a dual-gate SAMFET for the linear (black lines for –2 V) and saturated (red lines for –20 V) regimes. The bottom gate bias is varied from left to right in steps of 10 V from +20 V to –20 V.

thickness, electrostatic interference between top and bottom channel might be expected. Recently, a dual-gate self-assembled monolayer field-effect transistor (SAMFET) was reported.[34] The semiconductor is only a monolayer thick. The accumulated charges of both the bottom and the top gate electrode are both contained inside the single monolayer. In **Figure 2**, the transfer characteristics of the dual-gate SAMFET are presented. The SAM is chemically attached to a SiO_2 bottom dielectric grown on a Si bottom gate. On the resulting SAMFET as the top dielectric the insulating polymer poly-isobutyl methacrylate (PIBMA) was spincoated, followed by evaporation of the Au top gate. Figure 2 shows that the dual-gate SAMFET behaves similarly to the DGTFT described in Figure 1. The main difference is the absence of the distinct 'hump' for positive gate bias, as expected because there is no bulk semiconductor. In a dual-gate SAMFET the accumulated charge carriers spatially overlap and form a single conduction channel. The transistor however behaves electrically as a single channel OFET where the effective charge accumulation is a superposition of the two gate biases modified by their capacitances. Distinct evidence of electrostatic interplay between the top and bottom channel of the dual-gate transistor was not observed.

3. Dual-Gate Logic Gates and Integrated Circuits

Functional digital integrated circuits, such as a 64 bit code generators for RFID tags,[5,6,35] shift registers for flexible displays[36] and driver circuits for actuators[37] have been reported. These complex circuits comprise hundreds to thousands of transistors combined into logic gates, such as inverters and two input NAND gates. The complexity leads to an inherent reliability issue. The output of one logic gate is the input of the next. Hence when one of the logic gates does not function properly, the integrated circuit usually fails. The larger the population of logic gates, the larger the probability for failure. A key parameter to define the reliability and robustness of logic gates is the noise margin, which can be described as the maximum allowable spurious signal that can be accepted by a gate while still giving correct operation.[38] The noise margin is calculated as the side of the largest square that can be inscribed between the input-output characteristics of the logic gate and its mirrored image. De Vusser et al.[39] calculated the influence of TFT parameters on the noise margin of unipolar logic gates and made a yield analysis of unipolar circuitry incorporating the statistical variations of the transistor parameters.

TFT based integrated circuits are typically based on unipolar *p*-type transistors for organic circuitry and unipolar *n*-type transistors for metal-oxide circuitry. For organic *p*-type transistors, the threshold voltage is in most cases slightly positive which results in 'normally on' characteristics. Therefore, integrated circuits are commonly based on a zero-V_{GS}-load topology, whereby the gate of the load-transistor is connected to its source. This topology suffers from an inherently small noise margin.[35,40] In this section of the review, we will describe the advantages of DGTFTs when incorporating them into integrated circuits. One obvious possibility is to adjust the V_{th} of the transistors in the logic gates and hence to move the trip point (V_{trip}) of the inverter (or another logic gate), leading to an increase in some cases of the noise margin of these unipolar dual-gate inverters.[30,35,41,42] DGTFTs can also be integrated in complementary technologies, to increase the noise margin which consequently can lower the operation voltage of complementary inverters.[6] In driver circuits for actuators,[37] DGTFTs are introduced into static random access memory (SRAM) cells to adjust the threshold voltage and hence to increase the noise margin of these cells. In analog circuits, advantages of DGTFTs have been found in the increase of the transconductance leading to an increased gain band width of differential amplifiers.[6] Furthermore, DGTFTs have been implemented to operate as self-contained logic gates.[20,21,27] Finally, DGTFTs in *a*-Si:H technologies targeting AM-LCD and AMOLED displays are discussed.

The first dual-gate inverter was reported in 2006 by Koo et al.[42] They report a dual-gate inverter based on pentacene as the *p*-type semiconductor, with an Al_2O_3 bottom dielectric and a parylene top dielectric. The transistors were combined into an inverter using zero-V_{GS}-logic. The driver is a dual-gate transistor, while the load remains a standard single gate transistor. They showed that the input-output characteristics of the inverter change upon applying a bias to the top gate of the driver. However, the trip point of the inverter could not be shifted into the supply range, between ground and rail bias V_{dd}, because the original V_{th} was too positive to compensate for. Hence the logic gate did not invert. In a subsequent paper[41] they reported a functional dual-gate inverter by replacing the top dielectric parylene with Al_2O_3. During parylene deposition, the pentacene layer was affected, leading to a limited depletion performance. The trip point of the inverter could now be controlled. No values for the noise margin were reported however.

A dual-gate inverter with back gates on both the load and driver transistor was reported by Spijkman et al. in 2008.[30] The semiconductor is PTAA, with SiO_2 and PIBMA as the bottom and top dielectric respectively. The noise margin is shown in **Figure 3** as a function of the applied bias to the back gate of the driver transistor, for different bias voltages to the load transistor.

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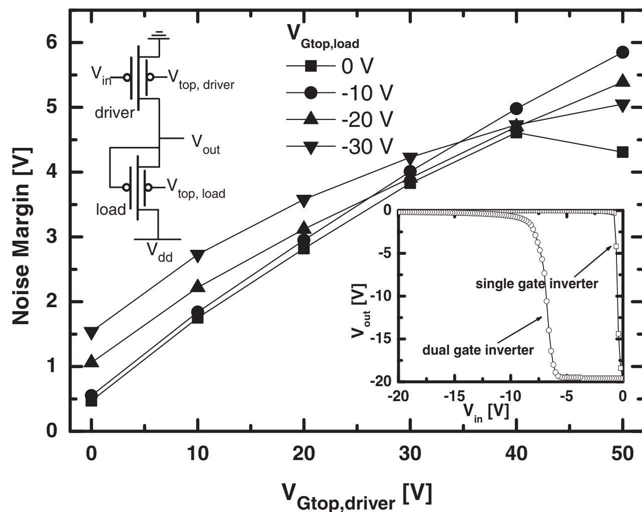

Figure 3. The noise margin of dual-gate inverters as a function of the top gate bias on the driver transistor for several top gate biases on the load transistor. The supply voltage V_{dd}, was set at –20 V. The insets show the schematic of the dual-gate inverter and the improvement gained in input-output characteristics by using a dual-gate inverter. Reproduced with permission.[30] Copyright 2008 American Institute of Physics.

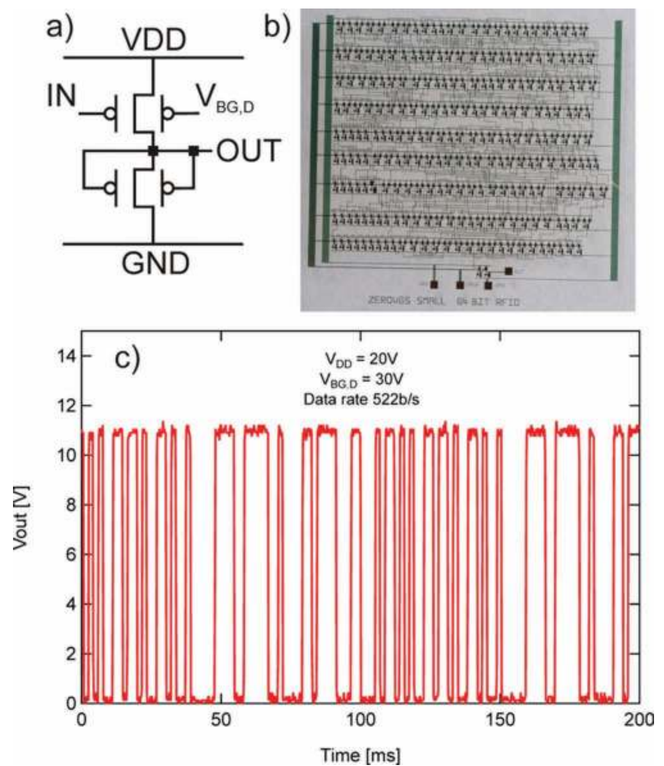

Figure 4. (a) Schematics of an enhanced zero-V_{GS}-load dual-gate inverter. (b) Photograph of a 64 bit organic RFID transponder chip. (c) The measured output signal of the transponder chip using the topology of Figure 4a, yielding a data rate of 522 bps at a 20 V supply voltage. Reproduced with permission.[35] Copyright 2011 IEEE.

The bias on the load transistor has a much smaller influence on the noise margin, but during dynamic operation the switching speed is dominated by the pull-down current flowing through the load transistor. By advantageously tuning the back gates of both dual-gate transistors in the inverter, the noise margin could be increased six-fold to almost 6 V, which has to be compared to a single gate inverter having a noise margin less than 1 V, both at a supply voltage of 20 V.

A comprehensive study of the use of dual-gate transistors to control the threshold voltage of load transistor and drive transistor of inverters and digital circuits has been performed by Myny et al.[35] The authors compare unipolar *p*-type zero-V_{GS}-load and diode-load inverters, whereby all transistors in the inverters are DGTFTs. In a diode-connected load the gate of the transistor is connected to its drain. The semiconductor used in this work is pentacene. Two solution-processed organic dielectrics serve as the bottom and top gate dielectric. The top gate dielectric is coupled much weaker to the semiconductor. Therefore, the V_{th} of the transistor shifts with about 35% of the applied back-gate voltage. By applying different back-gate voltages to the load and driver transistor, the trip point of the inverters can be shifted towards the ideal position, resulting in an increased noise margin of 2.8 V and 0.7 V for zero-V_{GS}-load and diode-load inverters respectively, for a supply voltage of 20 V. As explained above, varying the back-gate voltage of the load transistor has a much stronger effect on the frequency of ring oscillators than varying the back-gate voltage of the drive transistor. The authors also studied an enhanced dual-gate architecture for logic gates, where the back-gate node of the load-transistor is connected to its source, in this case the output node, as schematically depicted in **Figure 4**a. By means of these enhanced topologies, the noise margins can be increased to voltages above 6 V and 1.4 V for zero-V_{GS}-load and diode-load inverters respectively. Another advantage of this enhanced architecture is that only one additional voltage rail is present, instead of two voltages to control both the V_{th} of the driver and load transistor. In terms of ratio between the sizing of the driver and load transistor in logic gates, the authors conclude that enhanced zero-V_{GS}-load topologies can make use of the optimal 1:1 ratio, which is beneficial regarding the consumed area for integrated circuits. Next, these enhanced dual-gate logic gates were integrated into ring oscillators and 64 bit transponder chips. Figure 4b shows a photograph of a 64 bit RFID transponder chip, implemented with enhanced dual-gate zero-V_{GS}-load logic gates. The measured output signal of a 64 bit transponder chip is shown in Figure 4c, at a 20 V supply voltage. While the onset voltage of all measured single gate 64 bit transponder chips were situated between 20 V and 26 V, caused by the origin of the V_{th} of the single gate TFT, the enhanced zero-V_{GS}-load topology could lower this onset voltage to 10 V for all measured transponder chips on three different wafers, which is the lowest onset voltage published for 64 bit organic transponder chips. The authors also demonstrate that enhanced diode-load topology yields faster circuits than the zero-V_{GS}-load topology.

All previous papers describe the use of a DGTFT into unipolar inverters and circuits. Hizu et al.[43] have integrated DGTFTs into organic complementary inverters, targeting a reduced operation voltage. The technology consists of pentacene as *p*-type semiconductor and fluoroalkyl naphthalenetetracarboxylic di-imide

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(NTCDI) as *n*-type semiconductor. The bottom gate dielectric comprises a 500 nm thick polyimide layer, while the top gate dielectric is a 600 nm parylene layer. The back-gate voltages of the *n*-type as well as of the *p*-type transistor in the inverter can be varied. The inverter without threshold voltage control is only functional when the applied supply voltage exceeds 15 V. Varying the back-gate voltage to enable different threshold voltages, then leads to a decrease in minimum applied supply voltage of 5 V, at which the trip point can also be shifted to its ideal position of 2.5 V, at exactly half the supply range.

Besides inverters and digital integrated circuits, Takamiya et al.[44] reported in 2007 the integration of DGTFTs in organic SRAM cells to increase the static noise margin. The SRAM cells were afterwards integrated into a Braille sheet display to improve the display switching speed and to reduce the number of bit lines and cell area. The actuators have a slow switching speed. Therefore the SRAM cell was used to simultaneously drive all the actuators. A picture of the Braille sheet display is presented in **Figure 5**a. Figure 5b shows the device structure and the layer stack of the Braille sheet display. The whole display including the actuator was manufactured on foil, with DGTFTs based on pentacene as a semiconductor and with parylene and polyimide as the two gate dielectrics. The authors did note that controlling the threshold voltage is necessary to compensate for the large parameter spread in organic transistors. To achieve reliable and stable SRAM operation, DGTFTs were used to set the threshold voltage. A bias of 30 V was applied to the control gate to define the threshold voltage. The noise margin could be increased by a factor of 2.6 over the situation with no effective bias applied to the gate. Moreover, chemical degradation of the semiconductor in ambient atmosphere leads to a drift in the threshold voltage. Therefore, DGTFTs were used to compensate for the threshold drift during 15 days of operation. In a second part of the paper, the authors did use the V_{th} control gate to tune the oscillation frequency of a 5-stage ring oscillator. The inverter-stages were realized from a unipolar *p*-type configuration, whereby the front-gate of the load transistor is constantly biased at –20 V. Both the load and driver transistors share the same back-gate voltage. The obtained frequencies could be tuned between 62 Hz and 383 Hz, by varying the back-gate voltage.

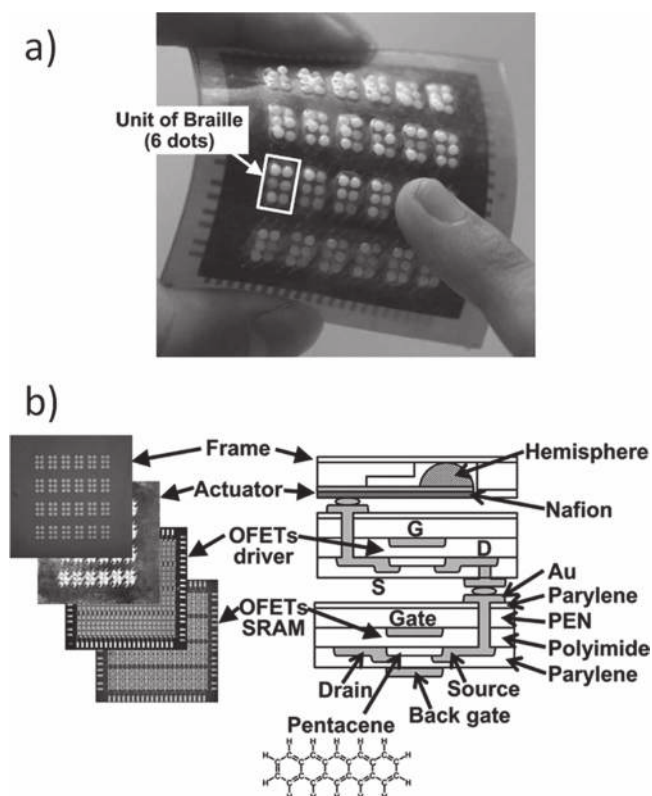

Figure 5. (a) Braille sheet display. (b) Device structure for the Braille sheet display with the dual-gate transistor of the SRAM cell on the bottom. Reproduced with permission.[44] Copyright 2007 IEEE.

Recently, Marien et al.[45] published the first organic analog circuits using DGTFTs. The technology used pentacene as *p*-type semiconductor and consisted of solution-processed bottom and top gate dielectrics. In analog circuits an important figure-of-merit of the transistor is the transconductance, which is the increase of channel current with gate voltage. The threshold-voltage control by the back gate is therefore optimized for increasing the transconductance. This was realized by permanently connecting the back gate to the front gate. When varying the gate voltage to increase the channel current, the threshold voltage of the transistor is then simultaneously shifted to more normally-on. This boosts the increase of the channel current with gate voltage, *i.e.* the transconductance by about 80% as compared to a single-gate transistor. The advantage of this technique has been demonstrated in a single-stage differential amplifier where all transistors are DGTFTs. The authors have verified the effect of the DGTFTs by comparing measurements of the single-stage differential amplifier with and without back gates. This yielded an increase of the DC gain from 8 dB to 15 dB and an increase of the gain band width from 3 kHz to 10 kHz for the dual-gate versus the single gate implementation. Finally, the authors have integrated these amplifiers successfully into a fully integrated, organic delta-sigma analog-to-digital converter.

DGTFTs can also be used as self-contained logic gates, preferably when the bottom gate and top gate dielectrics are matched. The first example was reported by Chua et al. in 2005,[27] who demonstrated a logic-AND operation using one single dual-gate transistor. The DGTFT consisted of TFB as a *p*-type semiconductor. The bottom SiO_2 gate dielectric and the organic BCB top gate dielectric thicknesses were matched to yield the same capacitances. The two gates acted as two different input gates. The drain current was the obtained output signal. On the left side in **Figure 6**a is a schematic of the transistor with the conduction channels depicted as a result of the applied gate biases to both gates. By switching the opposing gates between accumulation (–60 V) and depletion (20 V), they observed AND type logic operation, as depicted on the right side in Figure 6a. The two gates acting as the two inputs are shown on top, and the resulting output current is shown at the bottom. The drain current is only high (>10^{-5} A) if both gates are in accumulation. In all other combinations, the current is lower than ~10^{-8} A, resulting in an on/off current ratio larger than three decades.

Apart from AND gates, self-contained logic NOR-gates have been described by Park et al.[21] In a NOR-gate, the output is '1'

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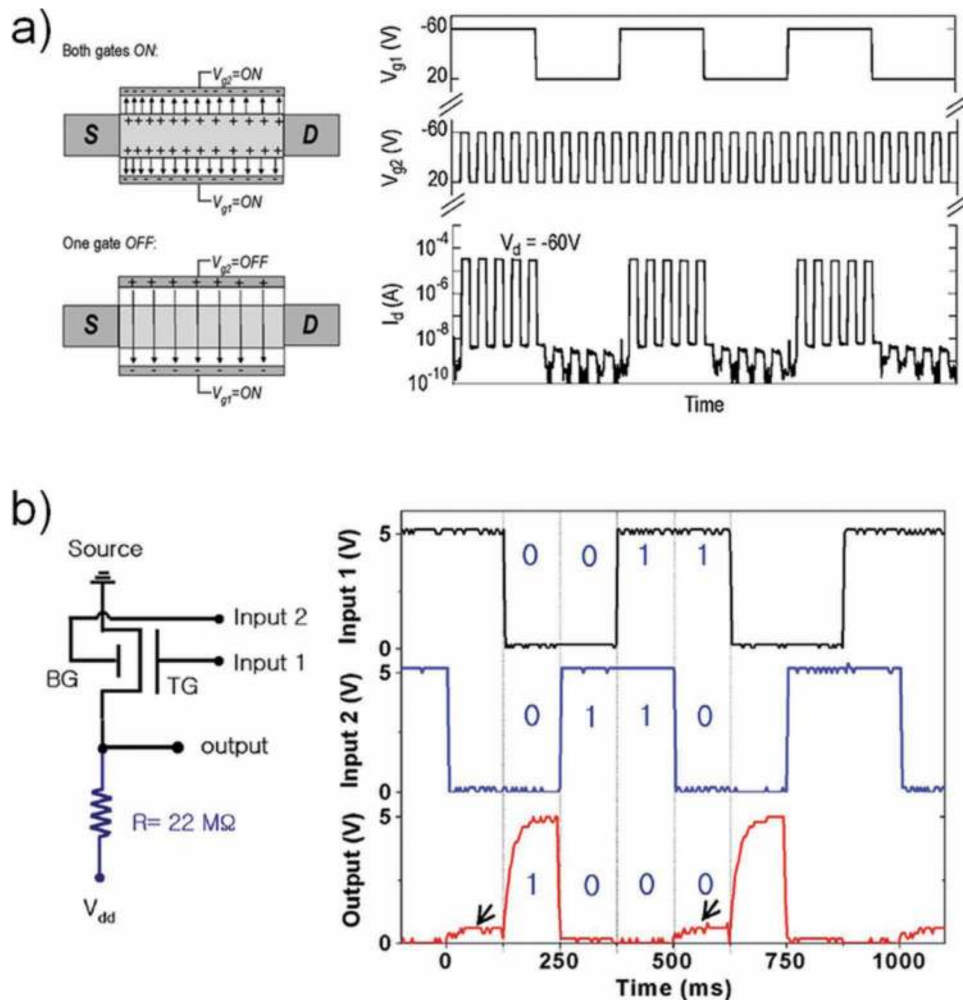

Figure 6. (a) Left: Operation of a DGTFT operated as a self-contained AND gate. With both channels ON (–60 V), two separate channels are formed. With the gate sufficiently OFF (+20 V) that gate depletes both the associated and the opposite channel, resulting in a low drain current. Right: An AND logic element from a single four-terminal DGTFT. On top the two input traces of the two gates with input signals of –60 V (accumulation) and 20 V (depletion). Below the resulting drain current as the output signal, only yielding a high current when both inputs are ON. Reproduced with permission.[27] Copyright 2005 American Institute of Physics. (b) NOR logic gate operation using a circuit combining a 22-MΩ load resistor and a DGTFT, where each of the two gates provides an independent logic input signal. 5 V and 0 V correspond with logical '1' and '0' respectively. Reproduced with permission.[21] Copyright 2009 IEEE.

only when both inputs are '0'. The input signals are applied to both gates of the transistor. A load-resistor of 22 MΩ was added to read out the signal. *n*-type ZnO is the used as semiconductor, having a 20 nm thick Al_2O_3 layer for both top and bottom gate dielectric. The circuit schematic and input-output characteristics are reproduced in Figure 6b. The input gate biases are 5 V (logical '1') and 0 V (logical '0'). The circuit is a voltage divider, switching the output between the ground and supply voltage of 5 V. With the dual-gate transistor in accumulation on one or both gates, the resistance is low. A large part of the voltage drops over the readout resistance and the output is 0 V. With both gates in depletion, the resistance of the dual-gate transistor is higher than the readout resistance, resulting in a 5 V output voltage.

The NOR gate can be transformed into an OR gate by reversing the ground and the supply bias, as demonstrated by Lim *et al.*[20] The output is '0' only when both inputs are '0'. In this work, InGaZn-oxide (GIZO) has been used as *n*-type semiconductor and SiO_2 for both gate dielectrics. 5 V ('1') and 0 V ('0') were used as the input signals. With both gates at 0 V, the effective resistance was larger than the readout resistance, which leaded to an output voltage of 0 V. For one or both gates in accumulation, the voltage drops over the readout resistance, resulting in an output voltage of 5 V.

Finally we note that *a*-Si:H DGTFTs are implicitly and explicitly being used in displays. The transistors are the pixel engines that drive the liquid crystals in LCD and OLEDs in AMOLED displays. The back electrode of the display acts as an effective back gate of the TFT forming a DGTFT. However, the implicit dual-gate layout causes a parasitic coupling. To prevent the back electrode from biasing the *a*-Si:H channel area, an additional back gate can be added to the TFT, which shields the channel,[24,46] as

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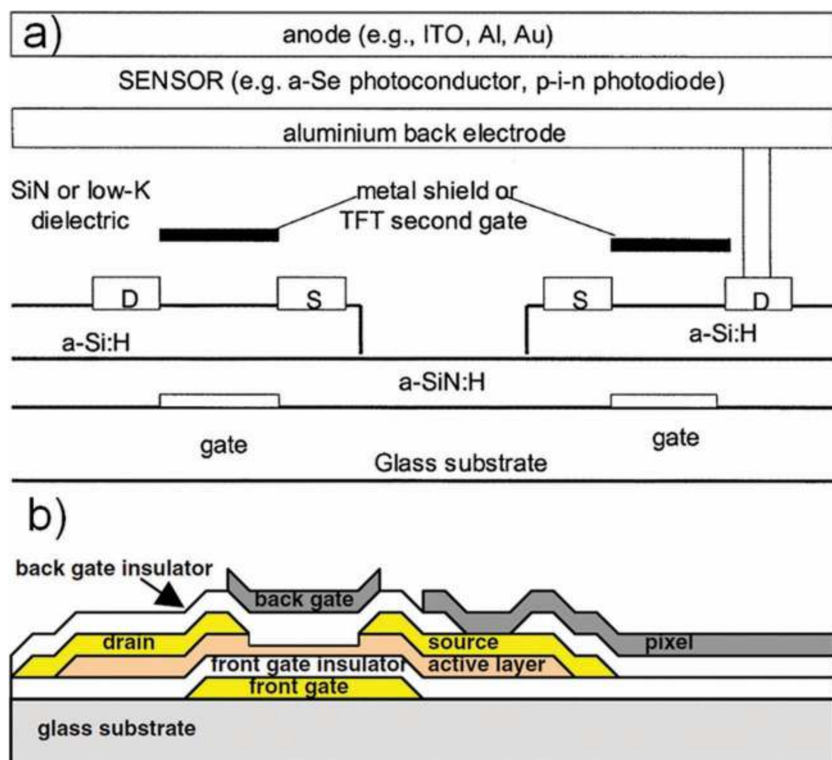

Figure 7. (a) Extra back-gate implemented as a shield for the back electrode in a *a*-Si:H TFT. Reproduced with permission.[24]. Copyright 2003 IEEE. (b) Cross-section of the layer stack in a *a*-Si:H process where back gate and pixel electrode are defined during the same patterning step. Reproduced with permission.[47]. Copyright 2009 Japanese Society of Appl. Phys.

shown in **Figure 7**a. As with organic and metal-oxide DGTFTs, *a*-Si:H DGTFTs can be used to actively set the threshold voltage and thereby increase long term display stability,[46] or to provide a higher on-current as compared to single gate TFTs.[16,17,47] The higher current reduces the footprint of the transistors, leading to a larger aperture ratio and to the ability to defining smaller pixels yielding a higher resolution.[46,47] Alternatively, the supply voltage can be reduced, leading to lower power consumption which is advantageous for mobile displays. As an example, Figure 7b shows the cross-section of a pixel where the back gate is applied without an additional lithographic mask step.[47]

4. Sensing Analytes in Aqueous Solutions

Transistors as sensors were first demonstrated in the form of ISFETs almost forty years ago[48] and are now commercially available as pH-detectors.[49] ISFETs are attractive for sensing applications, because they can respond with a large change in current to a relatively small change in the threshold voltage. The intended use of ISFETs is in the field of biosensing as label-free detection of biological analytes,[50] but the low sensitivity of ISFETs imposes a hard limit. To make biosensing possible, approaches such as carbon nanotubes,[51] Si nanowires[52] and diamond-based ISFETs[53] have all been tried. Because ISFETs measure a change in the threshold voltage, dual-gate transducers are a self-evident approach to increase their sensitivity. Here we briefly discuss present ISFETs as a benchmark and review SWNT, nanowires and thin-film organic dual-gate transistors.

ISFETs are standard metal-oxide field-effect transistors (MOSFET) where the gate electrode has been replaced with an electrolytic gate. ISFETs have been investigated as biosensors, *e.g.* for label-free detection of DNA-hybridization,[53] negating the need for costly polymerase chain replication (PCR). It has been shown that direct detection of protein charges with standard ISFETs is almost impossible.[50] Several solutions to increase the sensitivity have been proposed, such as single-walled carbon nanotubes (SWNT),[51] silicon nanowire transistors (NW-FET)[52] and diamond based ISFETs.[53] A self-evident improvement is a dual-gate transistor.[54–56] The additional gate has been used to enhance the sensitivity. Here we explain the operation and limitations of a standard ISFET and review the suggested improvements.

The layout of an ISFET is depicted in **Figure 8**a. The transducer is a standard Si MOSFET gated with an electrolyte, the potential of which is set by a reference electrode.[57] Ionic interactions at the interface between the SiO_2 gate dielectric and the electrolyte cause a change in the surface potential, Ψ_0. This change is detected as a change in threshold voltage, V_{th}, as $\Delta V_{th} = -\Delta\Psi_0$.[57] The sensitivity of ISFETs has been optimized for pH detection. The proton activity at the interface is related to the surface potential Ψ_0 by the Nernst equation as:

$$\Psi_0 \frac{k_B T}{q} \ln \frac{a H^+_{\mathrm{bulk}}}{a H^+_{\mathrm{surface}}} \tag{5}$$

where k_B is the Boltzmann constant, q is the elementary charge and the symbol a denotes the proton activities in the bulk electrolyte and at the gate dielectric-electrolyte interface. The surface

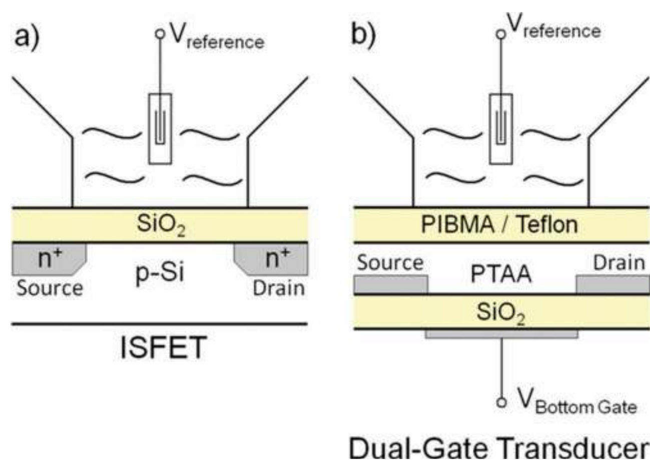

Figure 8. Schematic representation of an ISFET (a) and of a dual-gate transducer (b).

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potential can be related to the pH. A detailed analysis has been given by Bergveld,[57,58] leading to:

$$\frac{\delta \Psi_0}{\delta pH} = -2.3 \frac{k_B T}{q} \alpha \quad (6)$$

where α is a dimensionless parameter, the so-called proton buffer capacity, that varies between 0 and 1 and which is a measure for the proton activity of the interface. If α is 1 the ISFET has a Nernstian sensitivity of 59 mV/pH at 25 °C, which is also the maximum achievable sensitivity. In practice, the value of α is smaller than unity. For SiO_2, α is typically 0.5;[57] slightly higher values have been reported for more reactive oxides, such as tantalum oxide and erbium oxide.[59]

The detection of biomolecules is limited by the sensitivity. The gate dielectric–solution interface behaves as a capacitor. The compensating charges are absorbed ions and oriented dipoles. The whole array at the gate dielectric-solution interface constitutes the Helmholtz electrical double layer. The surface potential, Ψ_0,[60] decays exponentially with distance. The characteristic length scale is the Debye screening length, which in physiological solutions is in the order of a nanometer.[60,61] A physiochemical change in the environment is detected as a change in potential at the gate dielectric interface. Any changes in the physiological solution outside the Debye length are screened. The size of biomolecules is typically in the order of the screening length. Hence the change in surface potential is only a few mV.[50] A higher sensitivity is needed for the detection of biochemical analytes.

Several approaches have been reported. SiO_2 as gate dielectric has been replaced with more reactive surface materials such as Er_2O_3.[59] Another option to increase the ion interaction is surface modification for specific target recognition.[53,62] Finally the sensitivity is enhanced in diamond based ISFETs by using extremely thin dielectrics to increase the gate capacitance.[53] Alternatives to increase the capacitive coupling are the use of semiconducting nanotubes,[51,52] where the Helmholtz double layer itself is used as gate capacitance, and the use of dual-gate transistors.

Transducers using single-walled carbon nanotubes (SWNT) have been reported. A comprehensive review has been written by Allen et al. in 2007.[51] The nanotubes are applied onto a standard transistor substrate and immersed in the physiological solution. The single tubes are contacted at both ends. The SWNT is surrounded with electrolyte. The gate field is completely screened, and gating with the bottom gate is almost impossible. Instead the Helmholtz double layer is used as the gate capacitance, yielding a high gate coupling. The small size of the nanotubes combined with the high gate capacitance yields to a large increase in current; even single-molecule events can be detected.[63–66] Current emphasis is on functionalization with antibodies and other specific binding groups.

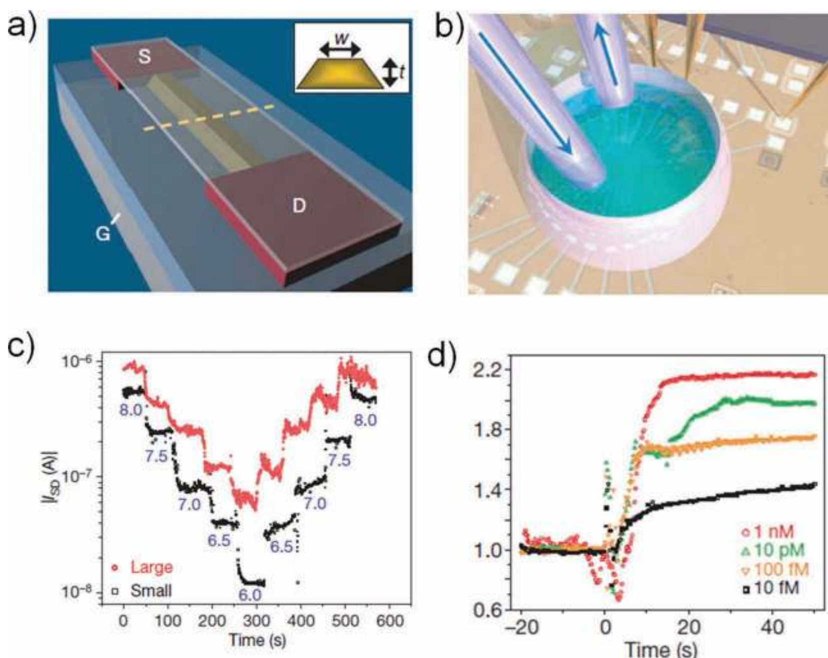

Figure 9. (a) schematic of a semiconducting nanowire (yellow) between source and drain electrodes. The inset shows the channel profile. (b) Artist impression of a fluid exchange system superimposed on optical micrographs of the chip. Fluid flow is indicated by the arrows. (c) Result of pH measurements performed on the two types of nanowires: a 'large' (red) device with w = 1,000 nm and t = 80 nm and a 'small' device with w = 100 nm and t = 25 nm. (d) Protein binding sensing with a biotin-avidin/streptavidin system for decreasing concentrations of streptavidin. Reproduced with permission.[68] Copyright 2007 Nature Publishing Group.

Other nano-sized semiconductors have been used to enhance the sensitivity. The 3D structure of a Si nanowire allows for a relatively high sensing area as compared to the 2D surface of thin-film transistors.[67] The nanowire can be either p-type or n-type. A schematic drawing of a Si nanowire sensor, as used by Stern et al.[68] is presented in **Figure 9**a. The nanowire was fabricated on top of a SiO_2 gate dielectric by e-beam lithography. The nanowire is covered by a thin layer of oxide acting as a top dielectric, which can be functionalized for detection of specific analytes. Indium oxide for example, is used for detection of lipoproteins and cancer antigens.[69–71] The Si nanowires have been used to detect low concentrations of proteins and DNA[72] as well as single virus particles.[73] Integration of nanowires into arrays allows for simultaneous detection of multiple biomarkers.[74] Stern et al. performed measurements with a microfluidic system on the nanowire as depicted in Figure 9b. The NW-FET showed reproducible pH detection in the range of pH 6 to pH 8, in steps of 0.5 pH, as shown in Figure 9c. Protein detection was demonstrated on the biotin-avidin/streptavidin couple, with which concentrations down to 10 fM could be measured (Figure 9d). For immunodetection, in this case performed on two types of mouse immunoglobulin (IgA & IgG), NW-FETs were first functionalized with the appropriate antibodies. In the experiments of Stern et al. a reference electrode in the solution was omitted. The authors argue that, since the signals are all relative potential changes in a short time, grounding the solution is not necessary.

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A nanowire FET with reference electrode has been described by Knopfmacher et al.[54] A *p*-type Si wire is covered by AlO_x deposited by atomic layer deposition (ALD). Contrary to Stern et al., the electrolyte potential was set with a reference electrode and the bottom gate was swept. For the pH measurements, the observed behavior of the threshold voltage shift was in agreement with the results obtained by Stern et al.

Knopfmacher et al. noted that the nanowire sensors can be considered as a dual-gate ISFET. A schematic of a dual-gate transducer is shown in Figure 8b. The highly doped substrate acts as a the bottom gate and the electrolyte as top gate. A dual-gate ISFET can be used to increase the threshold voltage shift detected at the electrolyte gate by the ratio between the two gate capacitances. The capacitive coupling can be used to amplify the typically small shift in the surface potential, Ψ_0, by the capacitive coupling in the dual-gate transistor analogous to Equation (3) by:

$$\Delta V_{th,bottom} = \frac{C_{top}}{C_{bottom}} \Delta \Psi_0 \quad (7)$$

Knopfmacher et al. have noted that by using an advantageous capacitive coupling, where the bottom oxide capacitance is lower than that of the combined top oxide and interfacial electric double layer, a pH sensitivity can be obtained with an apparent sensitivity exceeding the Nernst limit of 59 mV/pH.

The use of DGTFTs to improve the sensitivity of organic sensors is not limited to sensors in solution. In 2009, Park and Salleo[55] described a dual-gate field-effect transistor for the measuring of the relative humidity. The transistor consisted of a highly doped Si gate covered with a 200 nm thick layer of SiO_2. The organic semiconductors poly (3-hexylthiophene) (P3HT) and poly(2,5-bis(3-dodecylthiophen–2yl(thieno[3,2-b]thiophene) (PBTTT) were applied by spincoating and covered with various thicknesses of AlO_x deposited by ALD. The humidity was derived from the threshold shift after exposure to water vapor. The shift was inversely proportional to the thickness of the AlO_x layer, from which it was concluded that the operating mechanism was based on capacitive coupling between the top and bottom gate dielectrics. The absorbed water layer then should act as the top gate. The positive threshold voltage shift was explained as being due to a negative surface potential arising from oriented water molecules.

Application of organic transistors as sensors in aqueous solution inevitably leads to Faradaic leakage currents due to electrolysis. Direct contact of both the electrodes and semiconductor with water has to be avoided. To prevent this contact, the semiconductor has to be covered with a barrier layer. This additional layer then acts as a second gate dielectric. The operation mechanism of a dual-gate transistor based on spin-coatable polymers as sensors for analytes in solution has first been reported by Spijkman et al.[56] The transducer is schematically depicted in Figure 8b. The semiconductor polytriarylamine (PTAA) was spincoated on a Si/SiO_2 gate/gate dielectric substrate. For the top dielectric, a dual layer of polyisobutylmethacrylate and amorphous Teflon was used. The top gate dielectric thickness was about 700 nm to prevent water penetrating to the semiconductor layer. This limited the capacitive coupling to a factor of two. The sensitivity to pH was roughly 100 mV/pH.

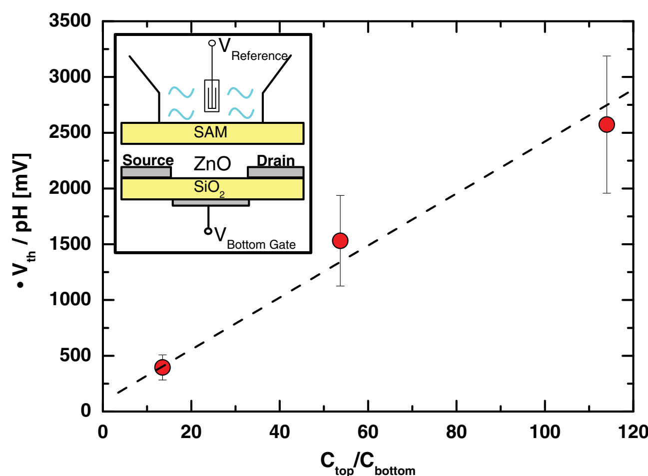

Figure 10. The sensitivity of ZnO/SAM based dual-gate transducers plotted in mV/pH as a function of the capacitive coupling, the ratio between the top and bottom gate capacitances. The data points correspond to bottom gate dielectrics of (from left to right) 200, 600 and 1,200 nm SiO_2. Each data point is averaged over about 10 measurements. The inset shows the device layout. Reproduced with permission.[75] Copyright 2001 American Institute of Physics.

To prevent Faradaic leakage currents, the drain bias has to be kept below about 1 V.[60] To measure drain currents for a low drain bias, high mobility semiconductors are required. The organic semiconductor was therefore replaced by a semiconducting ZnO, deposited by pulsed laser ablation. To arrive at a high capacitive coupling, an ultrathin SAM of octadecylphosphonic acid on the ZnO layer was used as top dielectric.[75] The sensitivity to pH as a function of the capacitive coupling is presented in **Figure 10**. The bottom gate SiO_2 thickness was varied to investigate the capacitive coupling and a maximum value of over a hundred was obtained. The scaling of the sensitivity with the capacitance ratio is linear. A significant amplification of the change in surface potential on top of the transducer is possible. The maximum achieved sensitivity was roughly 2.5 V/pH.

5. Outlook and Conclusions

A dual-gate transistor consists of a single field-effect transistor with an additional second gate and second dielectric. Each gate induces a channel. The thickness of the accumulation layer is only several nanometers. For standard semiconductor thicknesses the channels are spatially separated and can be tuned independently. DGTFTs were first reported in 1981 for CdSe and in 1982 for *a*-Si:H. The first organic DGTFTs were reported in 2005. Since then numerous papers on DGTFTs have appeared in literature.

Commonly reported features are an increased on/off current ratio, improved charge carrier mobility and a steeper subthreshold slope. The main difference between single-gate and dual-gate transistors however is a shift of the transfer curve with applied second gate bias. The shift in the threshold voltage depends linearly on the capacitive coupling, *i.e.* the ratio between the top and bottom gate capacitances.

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Tuning of the threshold voltage by the second gate has been applied in logic gates and integrated circuits. The noise margin for unipolar logic is inherently small. Dual-gate inverters have been reported. By advantageously adjusting the top gate bias the noise margin could be increased six-fold. Dual-gate logic gates have been integrated into ring oscillators and 64 bit RFID transponder chips. Dual-gate digital integrated circuits have been used to drive actuators in a Braille sheet display. The dual-gates were introduced to compensate for the large parameter spread and the shift of the threshold voltage during operation.

DGTFTs have also been applied in analog circuits. A single-stage differential amplifier with and without back gates yielded an increase of the DC gain from 8 to 15 dB and an increase of the gain band width from 3 to 10 kHz. These amplifiers have been successfully combined into a fully integrated, organic delta-sigma analog-to-digital converter.

DGTFTs cannot only be used to adjust the threshold voltage but can also be configured as self-contained logic gates. OR, AND and NOR gates have been reported. The need for dual-gate transistors in organic logic circuits will diminish with increasing shelf-life and operational stability of unipolar *p*-type transistors. Furthermore high performance *n*-type organic semiconductors are commercially available.[76,77] Unipolar logic will be replaced by complementary logic. The noise margin is inherently larger, reducing the need for dual-gate organic transistors.

A promising application of dual-gate transistors is in biosensors. The standard sensor is a silicon based ion-sensitive field-effect transistor (ISFET) introduced more than 40 years ago. However, direct detection of protein charges with standard ISFETs is almost impossible; the sensitivity is too small. The operation of an ISFET relies on detection of a current change due to a shift of the threshold voltage. The sensitivity can be enhanced by using dual-gate transistors. The sensitivity scales linearly with the capacitive coupling. By using a self-assembled monolayer as gate dielectric a high capacitance was obtained and the sensitivity could be enhanced beyond the Nernstian limit of 60 mV/pH to roughly 2.5 V/pH. The reported papers indicate that dual-gate transducers are a worthwhile platform for biosensing.

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