

Dual Standard Re-configurable Hardware Interleaver for Turbo Decoding

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Abstract—A very low cost re-configurable hardware interleaver for two standards, 3GPP-WCDMA and 3GPP Long Term Evolution (3GPP-LTE) is presented. The interleaver is a key component of radio communication systems. Using conventional design methods, it consumes a large part of silicon area in the design of turbo encoder and decoder. The presented hardware interleaver address generation architecture, utilizes the algorithmic level hardware simplifications to achieve very low cost solution. After doing the hardware optimizations the proposed architecture consumes only 3.1k gates with a 256x8 bit memory for the fully re-configurable dual standard interleaver address generator. The interleaved address is computed every clock cycle except the case of pruning (if block size is less than the row-column matrix) in 3GPP-WCDMA. In this case one additional clock cycle is consumed for valid address generation.

Keywords—Hardware interleaver, WCDMA, LTE, turbo codes, permutation polynomial

I. INTRODUCTION

MOST mobile phones and PC wireless connections have to support multi-mode (multi-standards). We therefore realize the importance of hardware reuse of FEC modules for low silicon costs. Hardware reuse for symbol processing was extensively discussed in [4]. However, hardware reuse of forward error correction (FEC) is seldom discussed. Among FEC modules, interleavers and de-interleavers are silicon consuming because of the silicon cost of the addressing tables. We therefore started the hardware reuse for interleaver address generation in FEC instead of using addressing memory. The newly evolved “3rd Generation Partnership Project (3GPP), Evolved Universal Terrestrial Radio Access (E-UTRA)” or 3GPP-LTE standard [1] is considered to be major step towards 4G systems. 3GPP-LTE uses turbo coding scheme for multiple applications. Wideband CDMA systems in 3G standard [2] also use turbo codes for forward error correction. The turbo codes [3] invented in 1993 captured great importance due to exhibiting near Shannon-limit performance. The superior error correcting performance of turbo codes over convolutional codes is associated with the suitable interleaver design. The primary function of the interleaver is to improve the distance properties of the concatenated coding schemes and to disperse

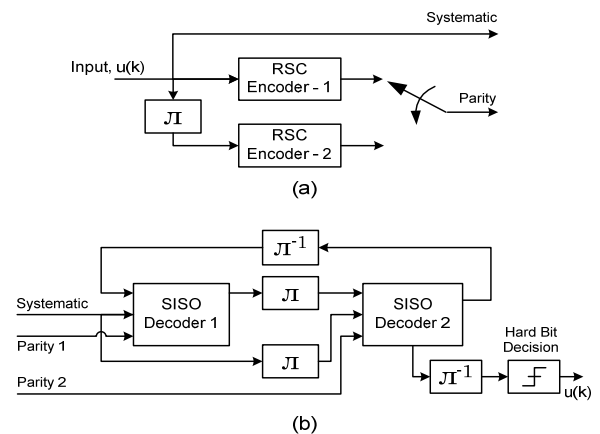


Fig. 1. Structure of Turbo Encoder and Turbo Decoder.

the sequence of bits in a bit stream so as to minimize the effect of burst errors introduced in transmission. Error correcting codes like turbo code can correct errors successfully as long as there are not too many errors in a single code word.

The scheme of turbo code adapted in both 3GPP-WCDMA and 3GPP-LTE is the parallel concatenated code (PCCC) with two 8-state constituent encoders. One turbo code internal interleaver is used in between the two recursive systematic convolutional encoders (RSC) as shown in Fig. 1a, while the turbo decoder as shown in Fig. 1b uses multiple instances of interleaver and de-interleaver to decode the received bits iteratively. The interleavers used in both the standards have different structure. Our research is to merge these two interleavers /de-interleavers structures into one low cost hardware module to demonstrate the way to reuse FEC hardware.

Our method in general is so called hardware multiplexing technique. It starts at analyzing / profiling multi CFG, identify opportunities of hardware multiplexing, and eventually fine tune the micro-architecture, using minimal hardware, and maximally reuse for multi functions.

Some comments on the previous work done for the design for hardware interleavers are provided in Section II. Section III provides the simplifications made for 3G-LTE standard. The detail of WCDMA hardware and its multiplexing with the LTE hardware is discussed in Section IV and V. The controller design and hardware implementation for the address generation of interleaver is described in Sections VI and VII respectively.

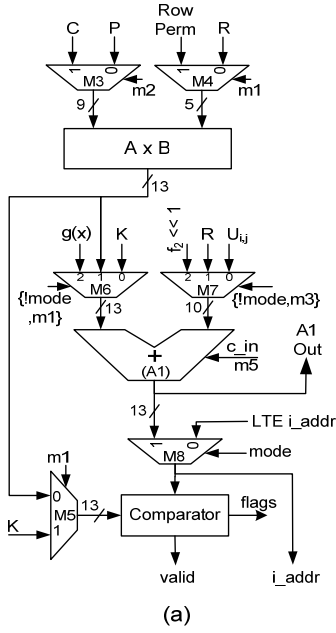


Fig. 3. (a) Hardware Multiplexing of Multiplication, Addition and Compare, (b) Flow Graph for Interleaved Modulo Multiplication Algorithm.

- Find $q(i)$ for $i=1,2, \dots, R-1$, take $q(0) = 1$, Determine the least prime integer $q(i)$ in the sequence such that $\text{g.c.d}(q(i), p-1) = 1$ and $q(i) > 6$ and $q(i) > q(i-1)$
- Apply inter row permutations to $q(i)$ to find $r(i)$
 $r(i) = T(q(i))$;
- Perform the intra row permutations $U_{i,j}$; (for $i = 0,1, \dots, R-1$;
 $j = 0,1, \dots, p-2$):
 If $(C=p)$: $U_{i,j} = S[(j * r(i)) \bmod (p-1)]$ and $U_{i,(p-1)} = 0$;
 If $(C=p+1)$: $U_{i,j} = S[(j * r(i)) \bmod (p-1)]$;
 and $U_{i,(p-1)} = 0$; $U_{i,p} = p$; and if $(K = R * C)$
 then exchange $U(R-1,0)$ with $U(R-1,p)$
 If $(C=p-1)$: $U_{i,j} = S[(j * r(i)) \bmod (p-1)] - 1$;
- Perform the inter row permutations
- Read the address columns wise

Looking at the interleaver algorithm in 3GPP-WCDMA standard, the computationally intensive functions found are Modulo Computation, Intra-row and Inter-row Permutations, Multipliers, Finding least prime integers, and Computing greatest common divisor. Some of these complex functions are implemented using the support from ROM, while the others are simplified to reduce the hardware usage.

V. WCDMA PRE-COMPUTATION HARDWARE AND MULTIPLEXING FOR LTE

As different block sizes has different interleaving patterns, thus every time some pre-computation is needed while changing the block size. The only parameter passed to interleaver is the block size (K) and rest of the parameters is computed by the hardware itself. The hardware interleaver parameters for WCDMA computed in the pre-computation phase are number of rows (R), no of columns (C), least prime number sequence ($q(i)$), inter-row permutation pattern ($T(i)$), prime number (p) and associated integer (v). Additionally the

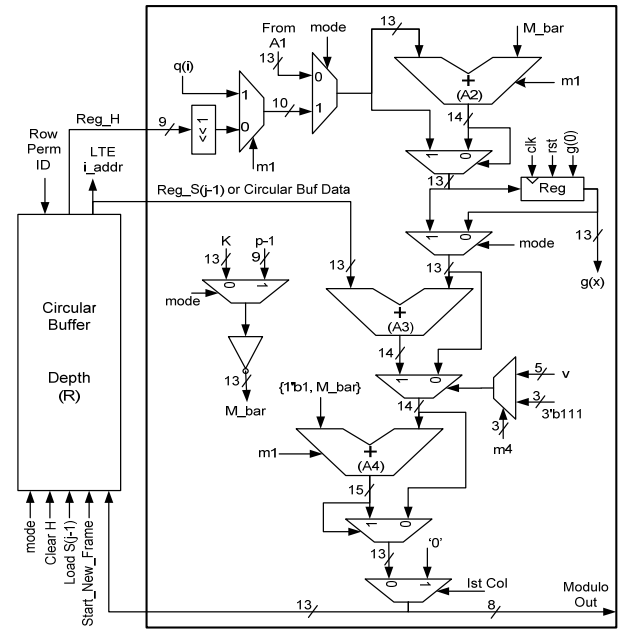


Fig. 4. Hardware for Modulo_Computation Block.

intra-row permutation pattern ($S(j)$) is also computed in the pre-computation phase and placed in a RAM of size 256x8 bit.

The computation of parameters in pre-computation for 3GPP-WCDMA is discussed in detail in [8]. Some parameters are computed using lookup tables while the others need some close loop or recursive computations. For computation of p and C, the multiplication, addition and comparison are needed. These blocks are shown in Fig. 3a. These blocks are multiplexed to serve in pre-computation phase as well as in run time for 3GPP-WCDMA and 3GPP-LTE. The computation of intra-row permutation pattern also need modulo computation. Here, the modulo function is computed iteratively using the Interleaved Modulo Multiplication Algorithm [11]. The required modulo function is $[S(j-1) * v \bmod P]$, so looking at v, which is 5bits, maximum of 5 iterations are needed to compute one modulo multiplication. The algorithm to compute the Interleaved Modulo Multiplications is shown in Fig. 3b. Three adders are needed to compute the $S(j)$ values. The hardware for the computation of $S(j)$ is shown in Fig. 4. Hardware multiplexing is done in such a way that all the hardware is being used in pre-computation phase, run time for 3GPP-WCDMA and run time for 3GPP-LTE. During pre-computation phase the ram write address is generated by the controller while in run time it is generated as the Modulo_Out signal in Fig. 4. The computed $S(j)$ values are placed in a 256*8bit RAM. The usage of this RAM depends on parameter p and it will be filled up to (p-2) locations starting from zero.

The parameters needed for 3GPP-LTE are only f2 and $g(0)$, which are found using the lookup table as mentioned in section III, so no parameter computation is needed for LTE in the pre-computation phase.

VI. CONTROLLER DESIGN

The controller mainly works for the pre-computation phase of 3GPP-WCDMA. It utilizes multiply, add, compare and modulo computation hardware to find all the vital parameters

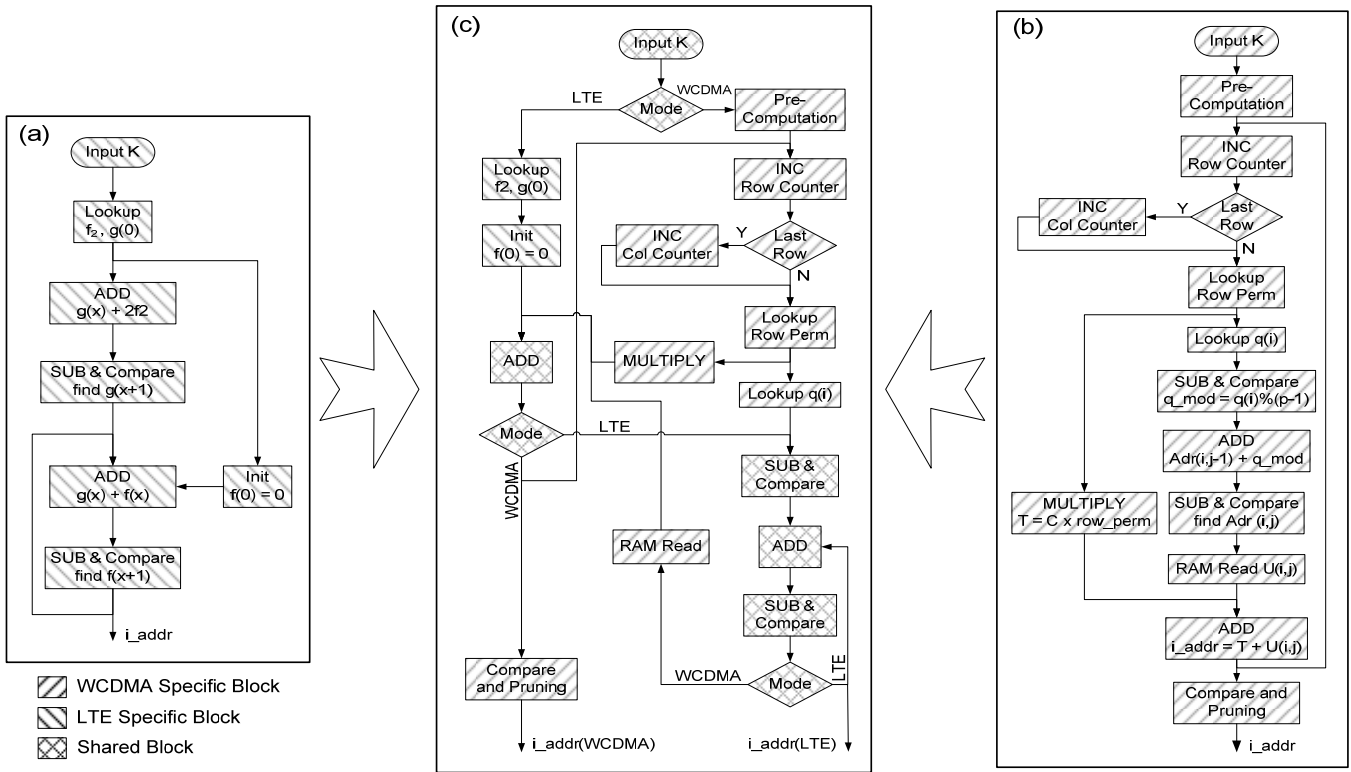


Fig. 5. Flow Graph for (a) The interleaver address computation in LTE, (b) The interleaver address computation in WCDMA, (c) The interleaver address computation for WCDMA and LTE in combined fashion.

R, C, p, v and S(j). The state diagram of the controller for our design is shown in Fig. 6. For 3GPP-LTE standard the controller only checks the mode and directly jumps into the ‘RUN’ state. The new frame can always be initiated by just changing the block size parameter K and providing one pulse named ‘start_new_frame’.

VII. THE HARDWARE IMPLEMENTATION FOR ADDRESS GENERATION

After completing the pre-computation phase or looking at the input mode (WCDMA / LTE), the controller is set in ‘RUN’ state and the hardware is configured to perform run time computations for the generation of the interleaved addresses. The computation of least prime number q(i) is handled by computing q mod (p-1) with the help of a lookup table and a subtractor. For 3GPP-WCDMA hardware interleaver the final RAM Address is computed mainly using the hardware shown in Fig. 3a. The recursive function used to compute the RAM address and multiply-add function to compute the final interleaved address are as follows:

$$\text{Ram_Adr}(i,j) = [\text{Ram_Adr}(i, j-1) + Q_mod(i)] \text{ mod } (p-1)$$

$$i_addr = (C * \text{Row_Perm}) + U(i,j)$$

Where U(i,j) is the intra row permutation coming from RAM. The final interleaved address is tagged valid or invalid using the comparator. This is called pruning of the interleaver and is needed for the case when interleaver block size is not exactly equal to R*C. The exception handling is done by using some flags and a couple of multiplexers.

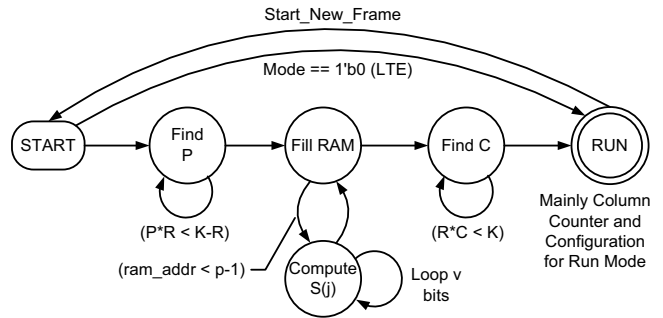


Fig. 6. Controller for WCDMA and LTE Hardware Interleaver.

For the computation of the interleaver address for 3GPP-LTE systems the same hardware is used after getting the mode input as LTE (1’b0). The controller jumps into ‘RUN’ state directly and with a small difference of configuration vectors the same hardware is mapped to the hardware shown in Fig. 2 for computation of interleaver address for LTE.

The flow graph for the run time operations in 3GPP-LTE and 3GPP-WCDMA are shown in Fig. 5(a) and 5(b) respectively. Fig. 5(c) shows the flow graph illustrating the sharing of both the standards to achieve the reusable hardware architecture. The complete hardware blocks to compute the interleaved address in a multiplexed way for 3GPP-WCDMA and 3GPP-LTE systems is shown in Fig. 7. It can be seen that all the vital computing parts are being shared by the two standards which provides an illustration of the hardware re-use to get the low cost solution for multiple applications.

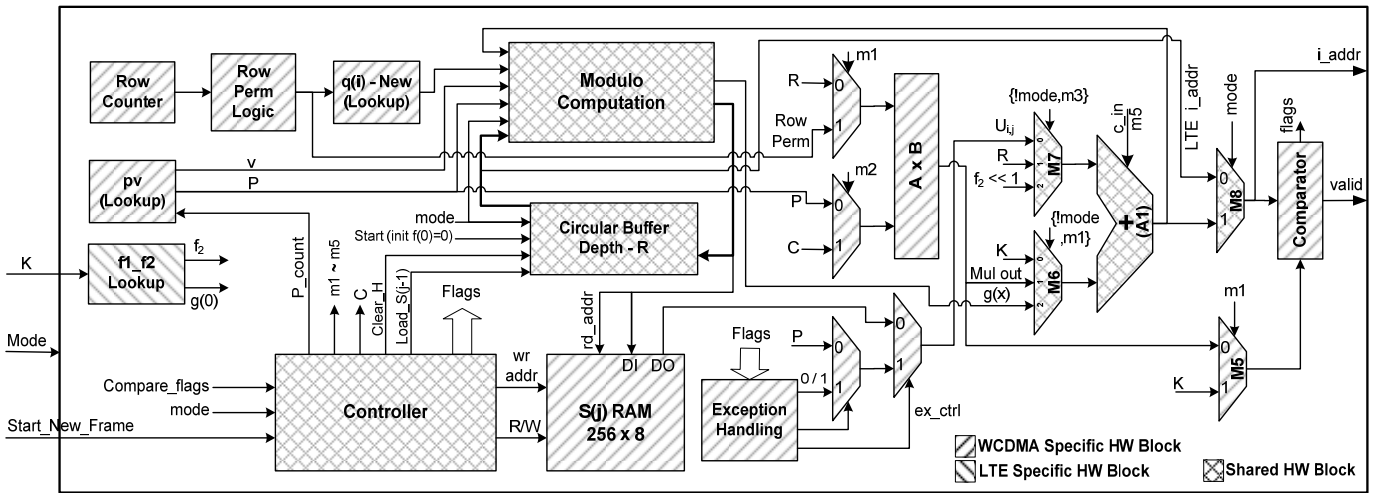


Fig. 7. Complete Hardware for Combined Interleaver Design.

VIII. IMPLEMENTATION RESULTS

The RTL code for the hardware blocks is written in Verilog and the correctness of the design is checked by comparing the results generated by hardware with those generated using MATLAB. The throughput of the address generator is one permutation address per clock cycle, except the case of pruning in WCDMA. In this case the interleaved address is computed at most every two clock cycles.

The design is synthesized after setting constraint as area using 90nm standard CMOS technology. Excluding the 256x8 RAM, the total hardware consumed by the presented design is 3.1 k gates. The presented design provides support for two standards which is not provided in reference designs [6], [7] and [8]. So comparing with the reference designs as shown in Table 1, the design presented here is good in terms of multiple standard support as well as hardware efficiency.

IX. CONCLUSION

In this paper a very low cost dual standard design for hardware interleaver address generation for 3GPP-WCDMA and 3GPP-LTE turbo decoding is presented. The final results show that it is a small design with the benefit of having two standard supports. Comparing with the conventional methods of using RAM for the interleaver, the silicon cost is about 20 times lower and the power consumption can therefore be much lower. The proposed architecture can act as a re-configurable interleaver accelerator with any kind of processor environment, thus providing performance with flexibility. Our principle goal is to investigate the hardware interleaver for multiple standards. In this regard the proposed architecture is the milestone towards our principle goal of architecture exploration for multiple radio communication standard support and further it can open more opportunities to cover more standards.

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TABLE I
HW USAGE COMPARISON FOR DIFFERENT ADDRESSING CIRCUITS

Sr. No	Implementation	Standard Support	Size
1.	ROM (all patterns)	---	> 100 Mbit
2.	RAM (big off-chip Mem. required)	---	~ 80 Kbit
3.	Design - 1 [5]	2	~ 32K gates
4.	Design - 2 [6]	1	~ 30K gates
5.	Design - 3 [7]	1	~ 4K gates
6.	Design - 4 [8]	1	~ 2.2K gates + 2Kbit RAM
7.	This Design	2	~ 3.1K gates + 2Kbit RAM

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