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Dual Threshold Voltage Organic Thin-Film Transistor Technology

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***Abstract*—A fully photolithographic dual threshold voltage (V_T) organic thin-film transistor (OTFT) process suitable for flexible large-area integrated circuits is presented. The near-room-temperature ($\leq 95\ ^\circ$C) process produces integrated dual V_T pentacene-based p-channel transistors. The two V_T's are enabled by using two gate metals of low (aluminum) and high (platinum) work function. The Al and Pt gate OTFTs exhibit nominally identical current–voltage transfer curves shifted by an amount ΔV_T. The availability of a high-V_T device enables area-efficient zero-$V_{\rm GS}$ high-output-resistance current sources, enabling high--gain inverters. We present positive noise margin inverters and rail-to-rail ring oscillators powered by a 3-V supply—one of the lowest supply voltages reported for OTFT circuits. These results show that integrating n- and p-channel organic devices is not mandatory to achieve functional area-efficient low-power organic integrated circuits.**

***Index Terms*—Digital integrated circuits, inverters, organic compounds, thin-film transistors (TFTs).**

I. Introduction

THIN-FILM transistors (TFTs) based on organic semiconductors offer the potential of large-area mechanically flexible integrated circuits due to their low temperature processing. For this reason, organic TFTs (OTFTs) have received much attention in the past ten years, during which there have been significant advances in OTFT performance. Pentacene is currently the organic semiconductor of choice for OTFTs due to its high hole mobility and environmental stability. Mobilities have been reported in excess of 1 cm^2/Vs, equaling the performance of amorphous silicon [1], [2].

Although pentacene OTFTs have been demonstrated with impressive electronic performance, there have been very few reports of functional digital OTFT circuits. OTFT technologies make circuit design challenging for three reasons: 1) the absence of a complementary device; 2) the value of the V_T; and 3) the lack of resistors. To improve OTFT technology, a number of technological enhancements have been proposed.

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The most obvious solution to this problem is to integrate an n-channel device to create a complementary process. Although organic semiconductors are typically hole transporters, small molecule materials such as hexadecafluorocopperphthalocyanine (F_{16}CuPc) have been demonstrated to be suitable electron transporters [3]. State-of-the-art organic digital circuits were created by Klauk *et al.* by shadow-mask patterning pentacene and F_{16}CuPc. Unfortunately, the use of shadow masking prohibits patterning large areas with small features due to bowing of the metal shadow mask. Yan *et al.* also report printed hole and electron transporting semiconductors but employed shadow masking in the device fabrication [4]. In addition, the integration of an n-channel device is only clearly advantageous if the electron mobility is comparable with the hole mobility of pentacene. For example, the electron mobility in [3] is 30× less than the hole mobility.

Another approach is to fabricate OTFTs with top and bottom gates, one of which is used to control the threshold voltage. Conventional enhancement-mode devices with back gates have been demonstrated in inverters with improved noise margins [5], [6]. This process requires the control of both pentacene–dielectric interfaces to achieve reproducible gate control. The added complexity and second power supply make this method unattractive.

In this paper, we present a dual-gate metal process to achieve integrated pentacene OTFTs with two threshold voltages. The current–voltage transfer characteristics of the aluminum and platinum devices are nominally identical but shifted by ΔV_T. To the best of the author's knowledge, this is the first report of OTFT V_T control by changing gate materials. The high-work-function platinum gate device exhibits a high V_T (i.e., more depletion like) and, by shorting its gate to source, can be used as an area-efficient current source with high output resistance. The integrated process is used to fabricate inverters and ring oscillators and can support the design of analog circuits such as amplifiers and comparators. These dual V_T circuits use 30× less area than a single V_T implementation, assuming a trip voltage of $V_{\rm DD}/2$. Powered by a 3-V supply, the nonoptimized inverter was measured to have a noise margin low (NM_L) of 1.3 V, a noise margin high (NM_H) of 0.3 V, and a current of 8 pA at the switching point. An 11-stage ring oscillator swings near rail-to-rail (0.05–2.85 V), with an inverter delay of 27 ms. Due to the low voltage operation and the small feature size enabled by photolithography, this paper has significantly better power-delay products than other works [3]. The inverters shown here use one of the lowest $V_{\rm DD}$s of any

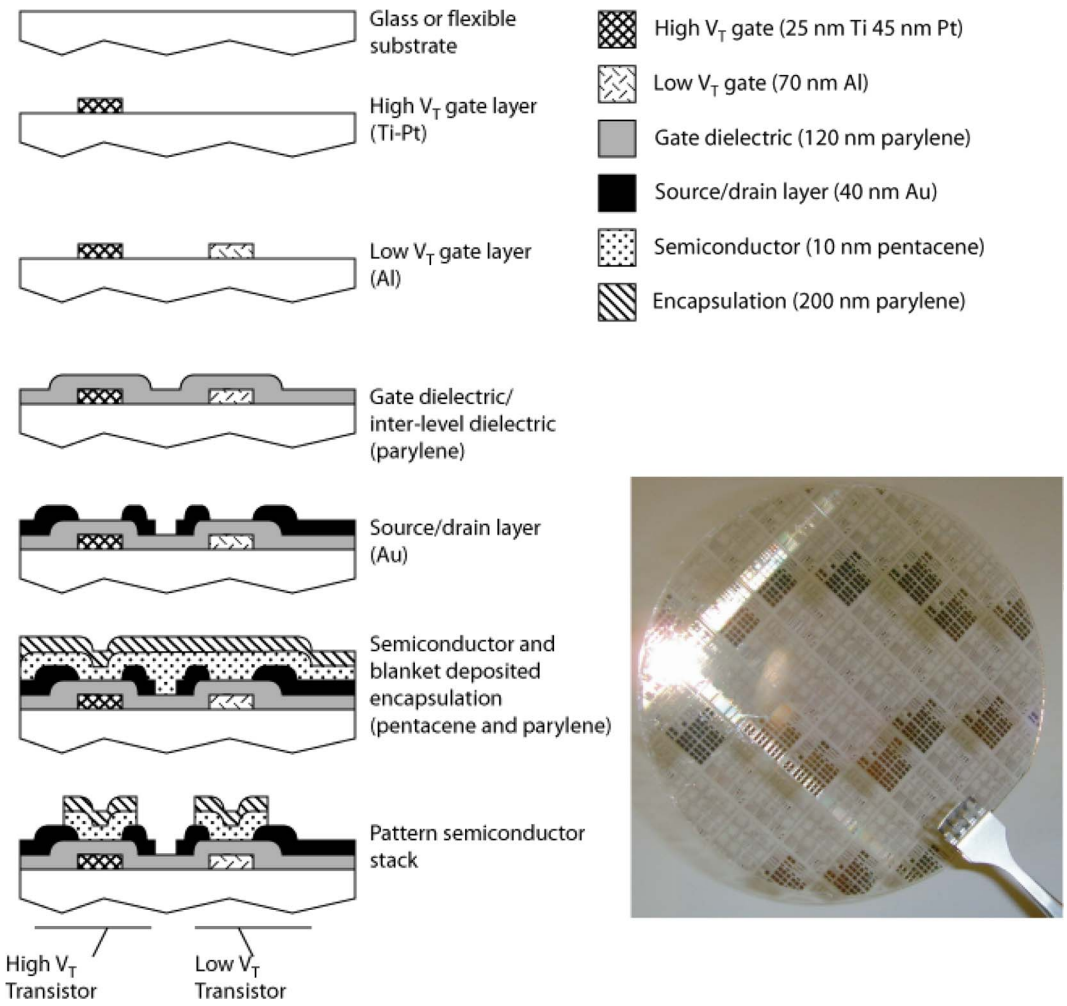

Fig. 1. Process flow for integrated dual V_T OTFTs and photograph of a finished 100-mm wafer.

OTFT technology, photolithographically processed or not [4], [7]–[10].

II. Dual V_T Process Flow

A near-room-temperature (≤ 95 °C) photolithographic process is used to fabricate integrated bottom-gate bottom-contact dual V_T OTFTs. The process is implemented using glass substrates, but its low temperature allows the use of flexible substrates. The process flow is depicted in Fig. 1, along with a photograph of a finished wafer.

All fabrication steps are done in a class 100 clean room. Float glass wafers (100 mm) are first cleaned in a 3:1 H_2O_2 : H_2SO_4 (piranha) solution for 10 min. The high-V_T (more depletion-like) gate pattern is transferred by image reversal photolithography, followed by a descum for 10 min in a barrel asher. Ti (25 nm) followed by Pt (45 nm) is electron-beam evaporated. The wafers are immersed in acetone and left overnight. A sonication in fresh acetone completes the liftoff process. Image reversal photolithography is next done for the low-V_T gate (more enhancement-like) in the same manner. After descum, 70 nm of Al is electron-beam evaporated. Liftoff is done in the same way as the Pt gate. After removal from acetone, the wafers are rinsed in deionized (DI) water, blown dry with nitrogen, and immediately loaded for dielectric deposition.

Parylene-C, an organic polymer, is used as the gate dielectric. Parylene (130 nm) (Galaxyl) is deposited by hot filament chemical vapor deposition while the substrate remains at room temperature. The run-to-run variation of the gate dielectric thickness is about 5%. We have not concentrated on optimizing this yet.

Via holes are patterned by photolithography and a reactive ion etch in oxygen plasma. Photoresist is stripped by immersion in a solvent photoresist stripper (Microstrip 2001), followed by a DI wafer rinse and nitrogen blow dry.

Au (40 nm) is deposited by electron-beam evaporation and patterned by standard photolithography. Since the process is not self-aligned, a gate–source and gate–drain overlap of 5 μm is included. The gold layer is wet etched in a solution of 5 : 1 H2O:Transene TFA gold etchant (KI/I_2). The photoresist is removed with Microstrip, and the wafers are rinsed in DI water and blown dry. Pentacene (10 nm) is thermally evaporated at 0.5 nm/min. Since the dielectric and the semiconductor of the two V_T devices are processed at the same time, we expect nominally identical dielectric–semiconductor interfaces for both devices. The pentacene deposition is immediately followed by a 200-nm blanket deposition of parylene-C. The parylene serves

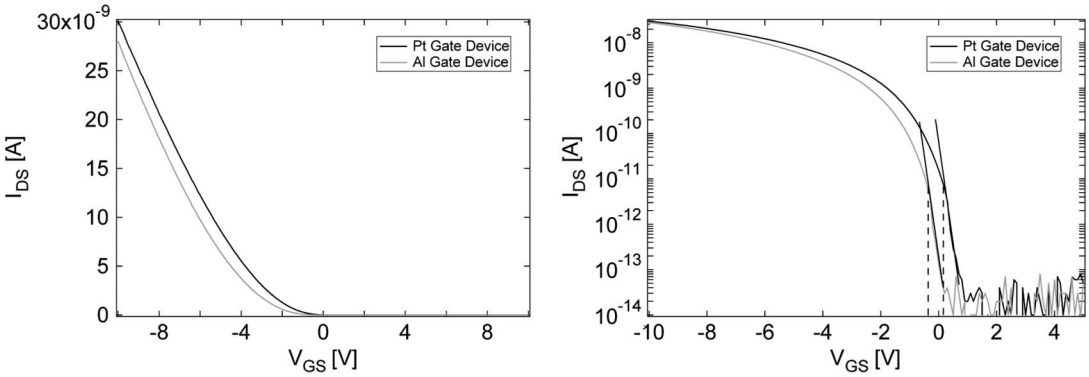

Fig. 2. (a) Measured linear transfer curves for adjacent $W/L = 200\ \mu\text{m}/15\ \mu\text{m}$ sized Al and Pt OTFTs at $V_{\rm DS} = -1$ V. (b) Measured semilogarithmic transfer curves for the same 200 μm/15 μm OTFTs at $V_{\rm DS} = -1$ V. The V_T is extracted by drawing a straight line fit in the subthreshold region and taking the voltage at which it pulls away. In this case, $V_{T,\rm Al} = -0.5$ V, $V_{T,\rm Pt} = 0.1$ V. The Pt device conducts 100$\times$ more current at $V_{\rm GS} = 0$ than the Al device.

as an encapsulant and prevents pentacene from exposure to subsequent solvent processing [11]. The pentacene–parylene stack is patterned photolithographically and etched in oxygen plasma, thereby defining the active region for each OTFT.

III. Dual V_T Device Performance

The fabricated devices are electrically characterized using an Agilent 4156C semiconductor parameter analyzer. Current–voltage and capacitance–voltage measurements are taken to extract device parameters such as $C_{\rm ox}$, subthreshold slope, contact resistance, and mobility. The $C_{\rm ox}$ is 22.3 nF/cm^2, and at a $V_{\rm SG}$ of 3 V, we measure a typical mobility of $\sim$0.01 cm^2/Vs [12]. We observe no difference in these parameters compared with the standard single V_T photolithographic process previously reported [13]. In addition, no difference in these parameters is observed between the Al and Pt gate devices. We observe a variation between the as-drawn and measured device width of 2 μm. Therefore, we choose 20 μm as the minimum device width in circuit designs. The channel length is patterned via a different wet chemical etch, and optical microscopy indicates that the fabricated channel length differs from the as-drawn by 100 nm or less.

Fig. 2(a) plots the linear and semi-log transfer characteristics for typical dual V_T devices. The threshold voltage is extracted by applying a linear fit to the subthreshold regime in the semi-log curve and noting the $V_{\rm GS}$ at which the I–V pulls away from the line. This process is shown in Fig. 2(b). The current–voltage curves are nominally identical, except shifted by an amount we call ΔV_T. A consistent ΔV_T of 0.6 V is observed over multiple wafers and lots. In each die, we extract the V_T of the Al and Pt gate devices and the shift in V_T between them ΔV_T. Table I shows the mean and standard deviation of the threshold voltages and ΔV_T.

The flatband condition for the TFT is written as

$$V_T = (\Phi_{\rm Gate} - \Phi_{\rm Pentacene}) - \frac{Q_f}{C_{\rm Gate}} \qquad (1)$$

where Q_f is the fixed charge (in coulombs per square centimeter) at the pentacene–parylene interface [6]. Since these devices operate in accumulation, we have referred to this voltage as V_T to be consistent with OTFT literature. The work function values are referenced to the vacuum level.

TABLE I
Statistics of V_T and ΔV_T Across Three Wafers. V_T Extracted as Shown in Fig. 2. Four to Five Dies Measured per Wafer

Parameter	Wafer 1	Wafer 2	Wafer 3
Mean V_T Al-Gate	-0.43 V	-0.46 V	-0.72 V
Std. Dev. V_T Al- Gate	0.10	0.09	0.15
Mean V_T Pt-Gate	+0.23 V	+0.08 V	-0.16 V
Std. Dev. V_T Pt- Gate	0.10	0.08	0.15
Intra-die Mean ΔV_T	+0.65 V	+0.54 V	+0.56 V
Intra-die Std. Dev. ΔV_T	0.06	0.05	0.09

By writing (1) for both metal gate devices, inserting the work functions of platinum and aluminum, and taking the difference, one can calculate the expected V_T difference between the two devices. Assuming uniform pentacene potential and parylene thickness across the wafer and no variation in fixed charge, the difference in flatband voltages should be proportional to the difference in metal work functions. Using work functions of 5.65 and 4.28 eV for platinum and aluminum, respectively, one would expect a difference in V_T between devices to be around 1.3 V [14].

We suggest two reasons for the difference in expected and observed threshold voltages. It is known that the presence of water on a metal surface will change the surface potential [15], [16]. Contamination of the metal surfaces through processing or residual water layers on the gates may lead to the effective work function difference of 0.6 V.

IV. Inverter Design and Characteristics

Conventional OTFT technologies are resistorless and contain a single V_T p-channel device. The lack of a high-output-resistance load makes designing inverters and amplifiers

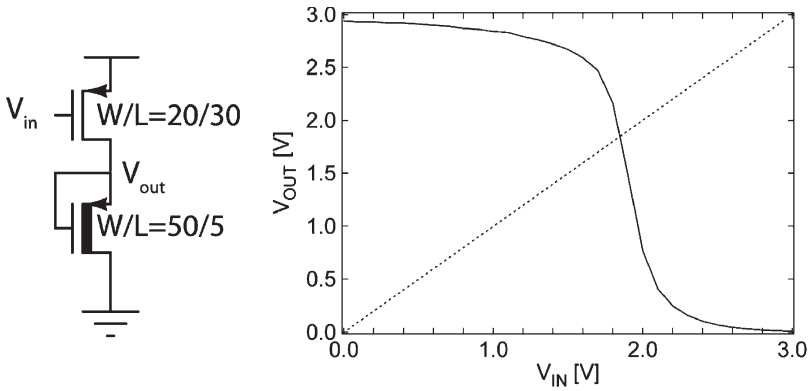

Fig. 3. (a) Dual V_T inverter with low V_T driver and high V_T zero-$V_{\rm GS}$ load. (b) Measured transfer characteristics $V_{\rm DD} = 3$ V. Noise margin high $({\rm NM}_H) = 0.3$ V, noise margin low $({\rm NM}_L) = 1.3$ V, $V_{\rm DD} = 3$ V.

difficult. In a p-channel-only process, there are two approaches one could take: use 1) a diode-connected OTFT load or 2) a zero-$V_{\rm GS}$ load [17].

Diode-load inverters have asymmetric transfer characteristics and low gain, making it difficult to achieve positive noise margins [7]. The zero-$V_{\rm GS}$ load provides a higher output resistance and thus higher gain, while allowing the inverter to be designed to trip near $V_{\rm DD}/2$. Given the gate-voltage-dependent mobility in OTFTs, the zero-$V_{\rm GS}$ load must be significantly wider than the driver to achieve positive noise margins [12], [18]. Not only does this make the area of the inverter large, it also increases the $C_{\rm GD}$ of the load transistor, decreasing the inverter speed. A dual threshold voltage technology alleviates this problem by enabling area-efficient high-output-resistance zero-$V_{\rm GS}$ current sources. Since the Pt gate device sinks 100× more current than the Al device at $V_{\rm GS} = 0$, using the high V_T device as the load reduces its area by two orders of magnitude.

An area-minimized inverter schematic is shown in Fig. 3. Hand calculations were used to size the devices. The inverter was designed to maximize noise margins and trip at $V_{\rm DD}/2$ while also minimizing the area. The measured transfer curve is asymmetric, as are the noise margins, since the fabricated load device's V_T was 200 mV more negative than was used in the hand designs.

The dual V_T inverter uses 30× less area and reduces the load capacitance by 17× compared with a single V_T implementation, assuming the single V_T topology is sized such that $V_M = V_{\rm DD}/2$. The measured inverter characteristics are pictured in Fig. 3. The inverter was found to have a noise margin high of 0.3 V and a noise margin low of 1.3 V when powered by a 3-V supply [19]. The Pt gate device's V_T was slightly more negative than was used in hand calculations, causing the inverter to trip at 1.8 V instead of at 1.5 V. The load would need to be twice as wide ($W = 100$ μm, $L = 5$ μm) to trip at 1.5 V. The current at the trip point $V_{\rm IN} = V_{\rm OUT}$ was 8 pA. The off currents ($V_{\rm IN} = 0$ V, $V_{\rm IN} = V_{\rm DD}$) were 9 pA and 480 fA, respectively.

If the inverter was instead optimized for speed and not area, then we estimate that an inverter delay of 7.7 ms would be expected with a driver $W/L = 20$ μm/5 μm and load $W/L = 300$ μm/5 μm while sinking 48 pA at its trip point.

These results compare favorably to state-of-the-art shadow-masked organic complementary metal–oxide–semiconductor digital circuits. The dual V_T inverter presented here uses 40× less area, 10 000× less switching current, and 10–20× less static current ($V_{\rm IN} = 0$ V, $V_{\rm IN} = V_{\rm DD}$, respectively) compared with the complementary inverters reported in [4]. The dual V_T inverter's power-delay product is over 50× lower at 5.6×10^{-13} J compared with an estimated 3×10^{-11} J. The improved power-delay product is due to the small feature sizes enabled by using a photolithographic process.

It should be noted that integrating an n-channel device does not necessarily improve performance compared with the p-channel-only dual V_T process. In the dual V_T design, the load is sized with a W/L of 15× larger than the driver in order for the inverter to trip at $V_{\rm DD}/2$. If we were to replace the zero-$V_{\rm GS}$ load with an NMOS device, then assuming a symmetric V_T with the p-channel TFT, the NMOS would need to be sized Z times wider than that p-channel driver. Z is equal to the ratio of the PMOS hole mobility to the NMOS mobility $Z = \mu_h/\mu_e$. Therefore, an n-channel device would only be clearly superior to the zero-$V_{\rm GS}$ load if $Z < 15$.

V. Ring Oscillator

An 11-stage ring oscillator with output buffer is fabricated and tested using the dual V_T process. The inverter topology is the same design as shown in Fig. 3. The circuit schematic for the ring oscillator is shown in Fig. 4.

The ring oscillator is powered by a 3-V supply. Fig. 5 plots the measured 1.7-Hz waveform, which corresponds to an inverter propagation delay of 27 ms [20]. In comparison, the inverter propagation delay reported in [3] is 2.3 ms, and 700 μs in [10]. Despite our small feature size, the gate delay is larger in the dual V_T implementation due to the low mobility. This is a result of the unoptimized pentacene deposition and poorer charge transport compared with other films reported [1]–[3]. This is in part due to our bottom-contact device architecture, which is necessary to ensure compatibility with standard photolithography. In addition, it has been widely reported that the vertical electric field increases mobility, and these devices operate at lower vertical fields than other reports [3], [10].

The ring oscillator output swings from 0.05 to 2.85 V. Although other OTFT ring oscillators have been published,

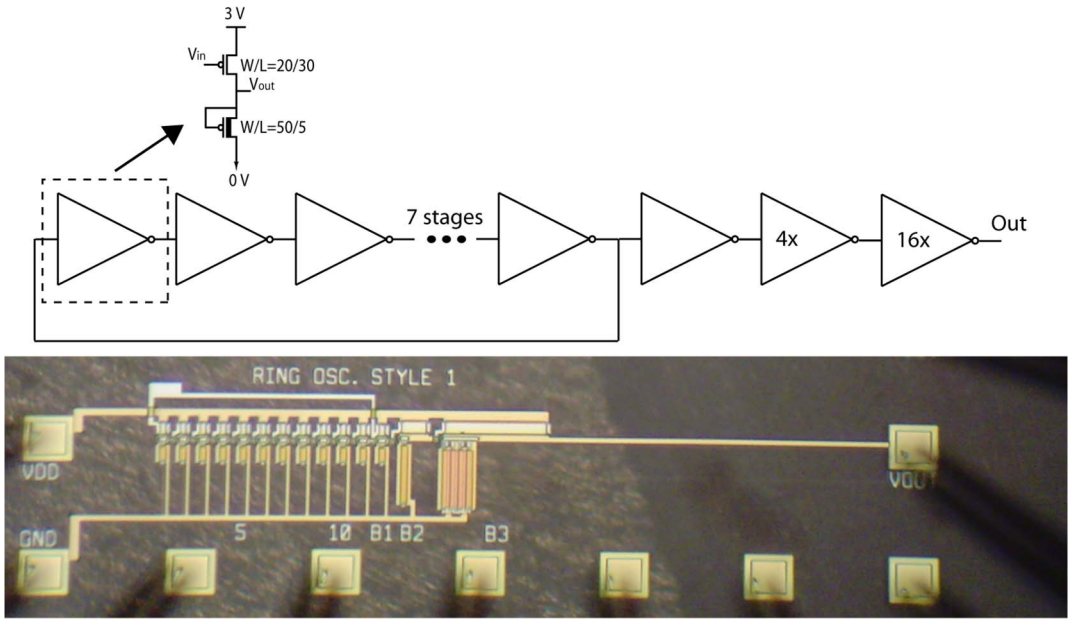

Fig. 4. Schematic and die photo of 11-stage dual V_T ring oscillator with output buffer.

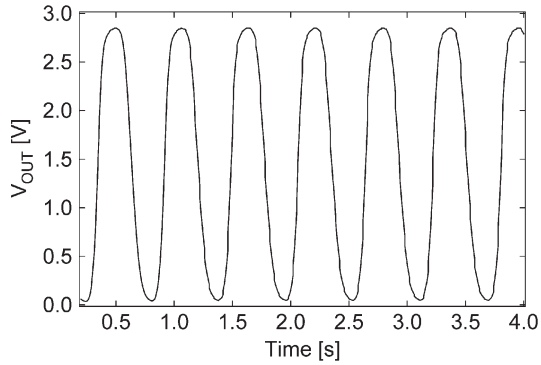

Fig. 5. Measured 1.7-Hz ring oscillator output, corresponding to an inverter delay of 27 ms. $V_{\rm DD} = 3$ V.

many do not swing near rail-to-rail and thus are not an accurate measure of the inverter propagation delay.

VI. Conclusion

A near-room-temperature process with two gate metals for integrated dual V_T OTFTs has been introduced. Devices are electrically characterized and are found to be nominally identical but shifted by $\Delta V_T = 0.6$ V.

An area-minimized integrated dual V_T inverter is fabricated and characterized, offering 30× area savings over a single V_T topology. The inverter has $\mathrm{NM}_H = 0.3$ V and $\mathrm{NM}_L = 1.3$ V and uses ∼24 pW of power with a 3-V supply.

An 11-stage ring oscillator using the inverter design is fabricated and tested, demonstrating rail-to-rail operation and an inverter delay of 27 ms.

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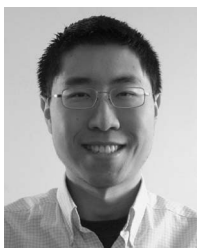

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