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Research Article

DVCCCTA-Based Implementation of Mutually Coupled Circuit

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This paper presents implementation of mutually coupled circuit using differential voltage current-controlled conveyor transconductance amplifier (DVCCCTA). It employs only two DVCCCTAs, one grounded resistor, and two grounded capacitors. The primary, secondary, and mutual inductances of the circuit can be independently controlled and tuned electronically. The effect of non-ideal behaviour of DVCCCTA on the proposed circuit is analyzed. The functionality of the proposed circuit is verified through SPICE simulation using 0.25 μm TSMC CMOS technology parameters.

1. Introduction

Since the beginning of current-mode circuit concept, a lot of research has been directed towards the development of active inductance and immittance simulator circuits. A limited literature is available on active realizations (simulators) of mutually coupled circuit (MCC). The MCC is characterized by primary inductance, secondary inductance, mutual inductance, and the coupling factor. The MCC simulators can be integrated easily and have reduced possibility of magnetic interference due to absence of inductive components. Also, there exists a possibility of tunability of inductance values along with the coupling coefficient. Considering this, some MCC simulators have recently been reported in literature that uses different active building blocks [1–8]. The study of MCC simulators [1–8] shows that the circuits reported in [1, 2, 7] are based on operational transconductance amplifier (OTA), [2–4] that uses second-generation current conveyors (CCII), [5, 6] employ second-generation current-controlled conveyors (CCCII), [7] uses differential voltage current conveyors (DVCC) and CCIIs, [8] and utilizes current-controlled current backward transconductance amplifier (CC-CBTA). Some of these implementations [1–7] realize grounded MCC whereas a floating MCC realization is reported in [8]. The OTA-based MCC [1, 2] employs eight OTAs and two grounded capacitors. The CCII-based structures [2–4] use four to eight active elements, four to six resistors, and two to four capacitors. The CCCII-based MCC [5] employs four CCCIIs, five resistors, and two capacitors [5]. Reference [6] reports another CCCII-based MCC that uses five CCCIIs, two capacitors, and an inductor. Two circuits are reported in [7], the first circuit uses four OTAs, two resistors, and two capacitors whereas the second circuit makes use of two DVCCs; two CCIIs, six resistors, and two capacitors. The recently reported MCC [8] uses three CC-CBTAs and three capacitors. The circuits reported in [1, 5–8] are electronically tunable MCC parameters.

In this paper, a new DVCCCTA- [9] based MCC is proposed that uses Gorski Popiel Technique [10]. It is floating in nature and uses only two DVCCCTAs, one resistor, and two grounded capacitors. The primary inductance (L_1), secondary inductance (L_2), and mutual inductance (M) can be electronically and independently controlled. The effect of nonideal behaviour of DVCCCTA on the proposed circuit is discussed. The functionality of the proposed circuit is tested under open-circuit condition. Its performance is exhibited by connecting it as a double-tuned band pass filter by using two additional resistors and two capacitors. The theoretical proposition has been verified with SPICE simulations using the parameters of 0.25 μm TSMC CMOS Technology.

2. Circuit Description

2.1. DVCCCTA. The DVCCCTA [9] is based on differential voltage current conveyor transconductance amplifier (DVCCTA) [11] and consists of differential amplifier, translinear

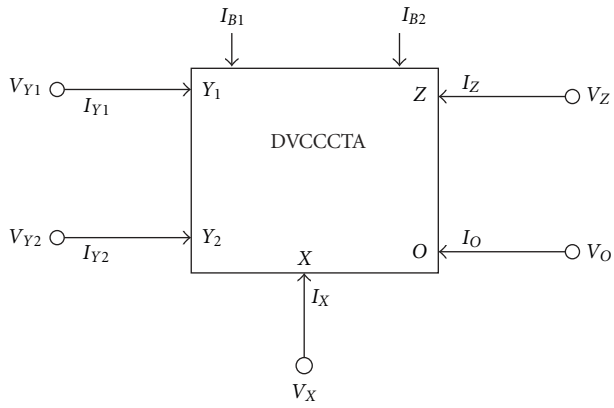

Figure 1: Circuit symbol of DVCCCTA.

loop and transconductance amplifier. The port relationships of the DVCCCTA as shown in Figure 1 can be characterized by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_X & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix}, \tag{1}$$

where R_X is the intrinsic resistance at X terminal and g_m is the transconductance from Z terminal to O terminal of the DVCCCTA.

The CMOS-based internal circuit of DVCCCTA [9] in CMOS is depicted in Figure 2. The values of R_X and g_m depend on bias currents I_{B1} and I_{B2}, respectively, which may be expressed as

$$R_X = \frac{1}{\left(\sqrt{2\mu_n C_{ox}(W/L)_{18,19} I_{B1}} + \sqrt{2\mu_p C_{ox}(W/L)_{16,17} I_{B1}}\right)}, \tag{2}$$

$$g_m = \sqrt{\mu_n C_{ox}(W/L)_{24,25} I_{B2}}. \tag{3}$$

2.2. DVCCCTA-Based Floating Mutually Coupled Circuit. In this section, firstly the port equations for a floating MCC are stated. Then, Gorski Popiel technique is outlined which is followed by realieation of the proposed DVCCCTA-based floating mutually coupled circuit.

2.2.1. Floating Mutually Coupled Circuit. A floating MCC is shown in Figure 3(a) and is functionally represented as

$$\begin{aligned} V_{1F} &= sL_P I_1 + sM_{12} I_2 + V_{3F}, \\ V_{2F} &= sM_{21} I_1 + sL_S I_2 + V_{3F}, \end{aligned} \tag{4}$$

where $L_P = L_1 + M_{11}$ and $L_S = L_2 + M_{22}$, and M_{12} and M_{21} represent mutual inductances of MCC.

Alternately, (4) can be represented as

$$\begin{aligned} V_{1F} - V_{3F} &= s(L_1 + M_{11}) I_1 + sM_{12} I_2, \\ V_{2F} - V_{3F} &= sM_{21} I_1 + s(L_2 + M_{22}) I_2. \end{aligned} \tag{5}$$

Representing the voltages $V_{1F} - V_{3F}$ and $V_{2F} - V_{3F}$ as V_{1D} and V_{2D}, respectively, (5) reduces to

$$\begin{aligned} V_{1D} &= s(L_1 + M_{11}) I_1 + sM_{12} I_2, \\ V_{2D} &= sM_{21} I_1 + s(L_2 + M_{22}) I_2. \end{aligned} \tag{6}$$

Equation (6) can be represented pictorially in Figure 3(b) which can be realized using Gorski Popiel technique [10] described in the following section.

2.2.2. Gorski Popiel Technique [10]. This technique is generalization of inductor simulation method and uses generalized impedance converter (GIC). The GICs are circuits whose input impedance can be changed by appropriate selection of components and load. A simplified pictorial representation of GIC is shown in Figure 4. The characteristic equation of GIC may be written as

$$\begin{aligned} V_1 &= V_2, \\ I_2 &= sTI_1, \end{aligned} \tag{7}$$

where T represents time constant of GIC. In Figure 5, a GIC connected to a resistor in input branch makes the input impedance inductive. The value of the inductance would be TR.

This technique implies that a resistive network embedded in GICs appears like an inductive network of same topology with the inductance matrix $L_i = TR_i$. Thus it allows replacement of complete inductor networks by similar resistive networks rather than treating each inductor separately. Thus, this technique can be easily applied to T-shaped resistive network to get the mutually coupled circuit as shown in Figure 6.

2.2.3. Proposed Floating Mutually Coupled Circuit. The method outlined in preceding section can be used for floating MCC realization if the voltages V_1 and V_2 (Figure 6) represent differential voltage as shown in Figure 7. The DVCCCTA, being capable of processing differential inputs through Y_1 and Y_2 terminals, can be used to implement floating mutually coupled circuit.

The proposed floating MCC circuit is shown in Figure 8 where each DVCCCTA realizes GIC block ($sT : 1$) and a series resistance. Thus the circuit uses X-port resistances of 1st and 2nd DVCCCTA for realization of inductances L_1 and L_2 whereas resistance R_M provides mutual coupling. The analysis of the circuit in Figure 8 gives

$$\begin{aligned} V_{1D} &= \frac{sC_1(R_{X1} + R_M)}{g_{m1}} I_1 + \frac{sC_2 R_M}{g_{m2}} I_2, \\ V_{2D} &= \frac{sC_1 R_M}{g_{m1}} I_1 + \frac{sC_2(R_{X2} + R_M)}{g_{m2}} I_2, \end{aligned} \tag{8}$$

where $V_{1D} = V_{1F} - V_{3F}$, $V_{2D} = V_{2F} - V_{3F}$, R_{Xi} and g_{mi} represent intrinsic X-port resistance and transconductance of ith DVCCCTA.

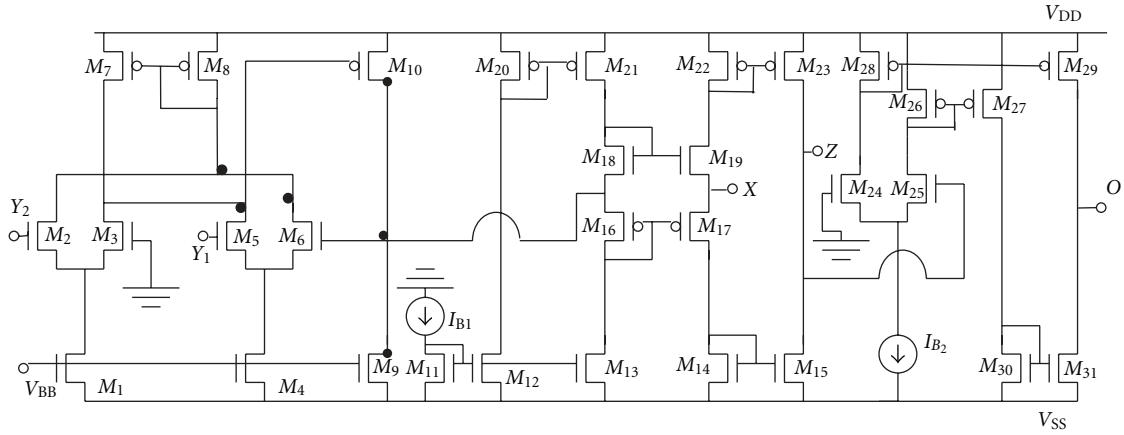

Figure 2: CMOS implementation of DVCCCTA [9].

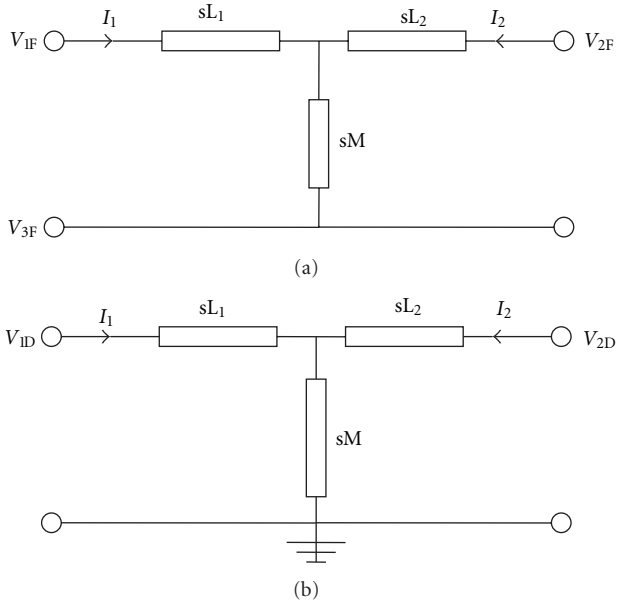

Figure 3: Pictorial representation of floating MCC.

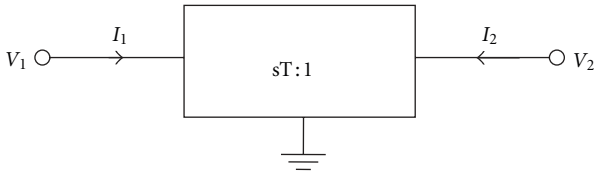

Figure 4: Symbolic Representation of GIC.

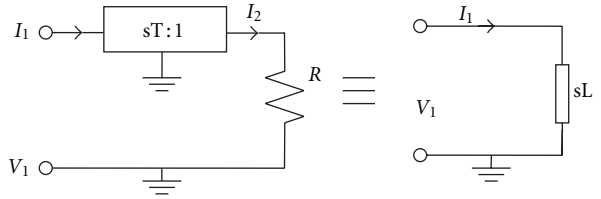

Figure 5: Inductance simulation using Gorski Popiel Technique.

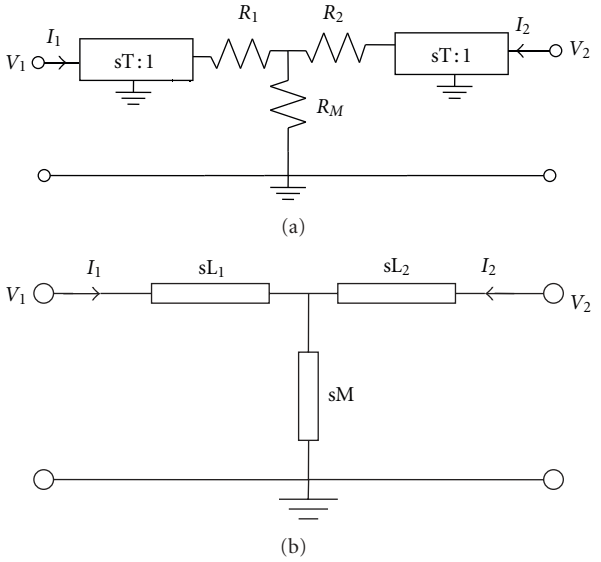

Figure 6: MCC implementation using Gorski Popiel Technique. (a) Resistive network with GIC, (b) its equivalent network.

Using (3) and (6), the values of various inductances L_1, L_2, M_{11}, M_{22}, M_{12}, and M_{21} can be computed as

$$L_1 = \frac{C_1 R_{X1}}{g_{m1}}, \qquad L_2 = \frac{C_2 R_{X2}}{g_{m2}},$$
$$M_{11} = \frac{C_1 R_M}{g_{m1}}, \qquad M_{12} = \frac{C_2 R_M}{g_{m2}}, \tag{9}$$
$$M_{21} = \frac{C_1 R_M}{g_{m1}}, \qquad M_{22} = \frac{C_2 R_M}{g_{m2}}.$$

For symmetrical coupling, $M_{12} = M_{21} = M$. Assuming $g_{m1} = g_{m2} = g_m$, and $C_1 = C_2 = C$, the inductances become

$$L_1 = \frac{CR_{X1}}{g_m}, \qquad L_2 = \frac{CR_{X2}}{g_m},$$
$$M = \frac{CR_M}{g_m}. \tag{10}$$

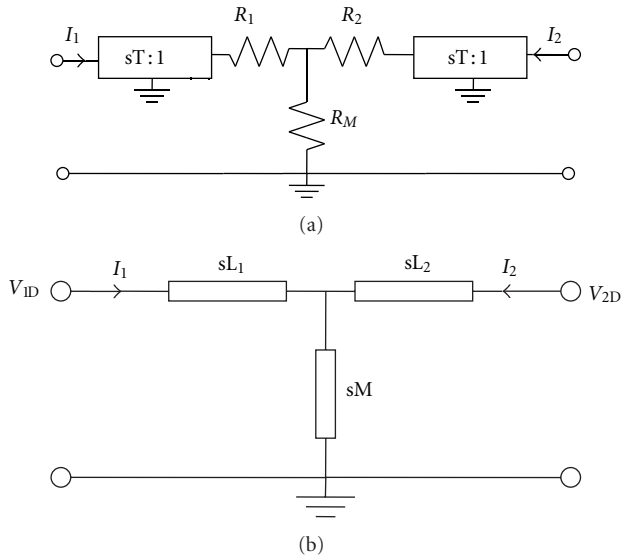

Figure 7: Floating MCC implementation using Gorski Popiel Technique.

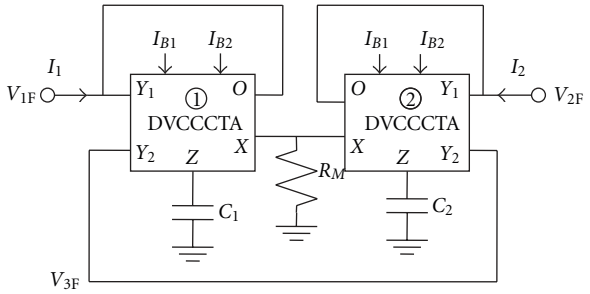

Figure 8: Proposed floating MCC circuit.

The coefficient of coupling (k) can be computed as

$$k = \frac{R_M}{\sqrt{(R_{X1} + R_M)(R_{X2} + R_M)}}. \tag{11}$$

The resistance R_M being grounded can easily be implemented with MOS transistor [12]. Thus, the inductances of MCC as well as coefficient of coupling can be electronically tuned.

2.3. Non-Ideal Analysis. The frequency performance of the proposed MCC may deviate from the ideal one due to nonidealities. The DVCCCTA nonidealities may be categorized in two groups. The first comes from nonunity internal current and voltage transfers in DVCCCTA. The modified port relationships may be written in matrix form as follows:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & R_X & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 \\ 0 & 0 & 0 & \gamma g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix}, \tag{12}$$

where the voltage transfer functions $\beta_1 = 1 - \varepsilon_{v1}$ and $\beta_2 = 1 - \varepsilon_{v2}$. The ε_{v1} and ε_{v2} denote voltage tracking errors from Y_1 and Y_2 terminals to X terminal, respectively. The current transfer function $\alpha = 1 - \varepsilon_i$, where ε_i denote current tracking error from X to Z terminal. The coefficient γ denotes current transfer function from Z terminal to O terminals. Considering these deviations in the voltage and current transfers, (9) modifies to

$$L_1 = \frac{CR_{X1}}{(\alpha\beta\gamma g_m)}, \qquad L_2 = \frac{CR_{X2}}{(\alpha\beta\gamma g_m)},$$
$$M_{11} = M_{12} = M_{21} = M_{22} = \frac{CR_M}{(\alpha\beta\gamma g_m)}, \tag{13}$$

where equal values of α, β, and γ are assumed for both DVCCCTAs. Equation (9) clearly indicates that the nonunity voltage and current transfer functions of DVCCCTA affect various inductances. Apart from having non-unity values, the current and voltage transfer functions also have poles at high frequencies. Their effect on proposed MCC performance can however be ignored if the operating frequencies are chosen sufficiently smaller than voltage and current transfer pole frequencies of the DVCCCTA.

The second group of nonidealities comes from parasitics of DVCCCTA comprising of resistances and capacitances connected in parallel at terminals $Y1$, $Y2$, Z, and O (i.e., R_{Y1}, C_{Y1}, R_{Y2}, C_{Y2}, R_Z, C_Z, R_O, C_O). The effects of these parasitics on filter response depend strongly on circuit topology. In the proposed structure, the external capacitor appears in parallel to the parasitic capacitor, the effect of these may be accommodated by preadjusting the external capacitor value.

Table 1: Aspect ratios of CMOS transistors in DVCCCTA.

Transistors	Aspect ratio (W (μm)/L (μm))
M_1, M_4, M_9, M_{11}–M_{15}, M_{30}-M_{31}	3/0.25
M_2, M_3, M_5, M_6	1/0.25
M_7-M_8, M_{20}–M_{23}, M_{26}, M_{28}-M_{29}	5/0.25
M_{10}	12.5/0.25
M_{16}-M_{17}	8/0.25
M_{18}-M_{19}	5/0.25
M_{24}-M_{25}	5/0.25
M_{27}	4.35/0.25

3. Simulation Results

To verify the functionality of the proposed DVCCCTA-based MCC, SPICE simulations have been carried out using TSMC 0.25 μm CMOS process model parameters and power supplies of $V_{DD} = -V_{SS} = 1.25$ V and $V_{BB} = 0.8$ V. The aspect ratios of various transistors of DVCCCTA (Figure 2) are listed in Table 1. Firstly, the proposed circuit is tested under the open-circuit condition, that is, $I_2 = 0$, so the ratio between the secondary and the primary voltage can be expressed as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_M}{R_M + R_{X1}}. \tag{14}$$

Equation (14) clearly shows that under the open-circuit condition the ratio between the output and input voltages

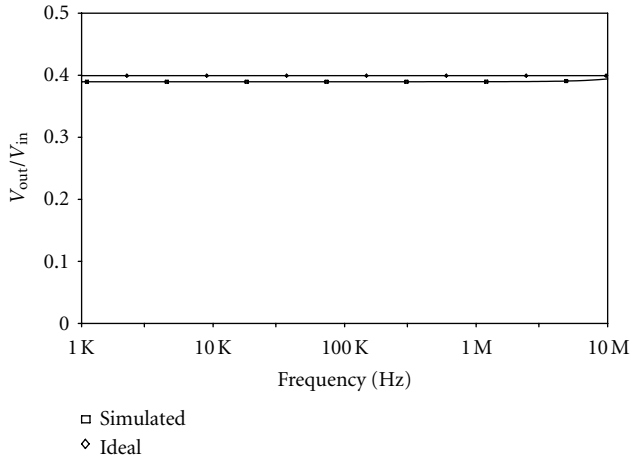

Figure 9: Simulated response of proposed MCC under open-circuit condition.

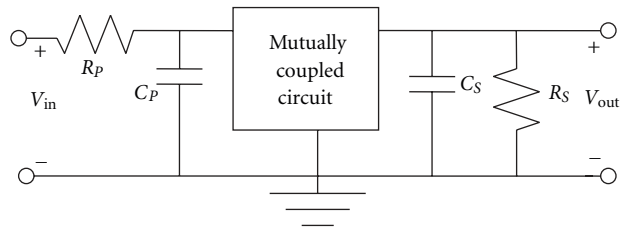

Figure 10: Double-tuned circuit.

will be frequency independent. The open circuit is tested for bias currents I_{B1} and I_{B2} taken as 10 μA and 160 μA, respectively, for both DVCCCTA. The values of C_1, C_2, and R_M are 10 pF, 10 pF, and 1.33 kΩ, respectively. The simulation result as shown in Figure 9 confirms the relation between V_{out} and V_{in}.

To illustrate an application of proposed mutually coupled circuit, a double-tuned circuit is constructed as shown in Figure 10. The primary and secondary side resonance frequencies (f_P and f_S) and quality factors (Q_P and Q_S) can be obtained as

$$f_P = \frac{1}{\left(2\pi\sqrt{C_P(L_1+M)}\right)}, \qquad f_S = \frac{1}{\left(2\pi\sqrt{C_S(L_2+M)}\right)},$$
$$Q_P = 2\pi f_P R_P C_P, \qquad Q_S = 2\pi f_S R_S C_S. \tag{15}$$

The performance of the double-tuned circuit is tested with following component values: $R_P = R_S = 11$ kΩ; $C_P = C_S = 20$ pF; for proposed MCC: $R_M = 1.33$ kΩ, $C_1 = C_2 = 10$ pF. The bias current I_{B1} and I_{B2} are selected as 10 μA and 160 μA, respectively, so as to provide $R_{X1} = R_{X2}$ as 2 kΩ and $1/g_{m1} = 1/g_{m2}$ as 1.5 kΩ. The resulting values of inductances are $L_1 = L_2 = 30\,\mu$H and $M_{11} = M_{12} = M_{21} = M_{22} = 19.95\,\mu$H. This selection results in $f_P = f_S = 5.035$ MHz and $Q_p = Q_s = 6.952$. The ideal and simulated responses of a double-tuned circuit are shown in Figure 11. There is a close agreement between the ideal and simulated values. The

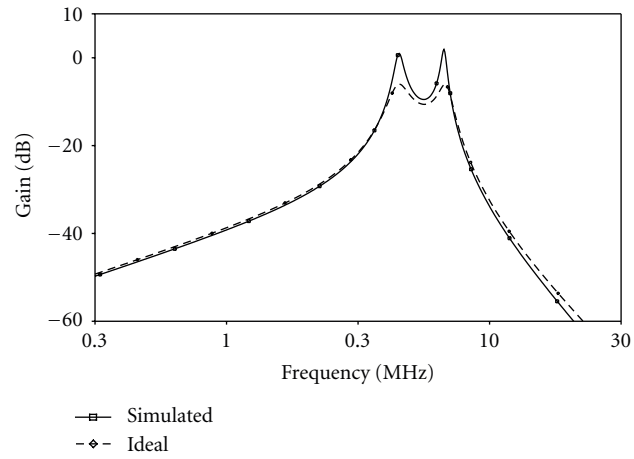

Figure 11: Simulated and ideal response of double-tuned circuit.

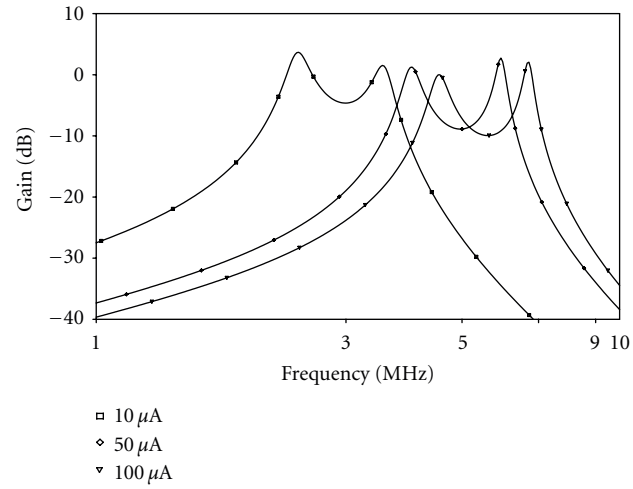

Figure 12: Simulated filter response with varying bias current I_{B2}.

electronic tunability is demonstrated by varying bias current I_{B2} of both the DVCCCTAs from 10 μA to 250 μA and the simulation results are shown in Figure 12.

To study the time domain behaviour of the double-tuned circuit (Figure 10), a sinusoidal signal of 300 mV amplitude and frequency of 5.035 MHz is applied as input. The transient response is depicted in Figure 13 which shows that ideal and simulated responses are in close approximation. The power consumption of the circuit was 2.77 mW. The double-tuned circuit is also tested to judge the level of harmonic distortion at the output of the signal. The %THD result is shown in Figure 14 which shows that the output distortion is low and within 3% up to about 800 mV.

4. Conclusion

In this paper, DVCCCTA-based circuit for simulation of floating mutually coupled circuit has been presented. The proposed circuit uses only two DVCCCTAs, one grounded resistor, and two grounded capacitors. The primary and

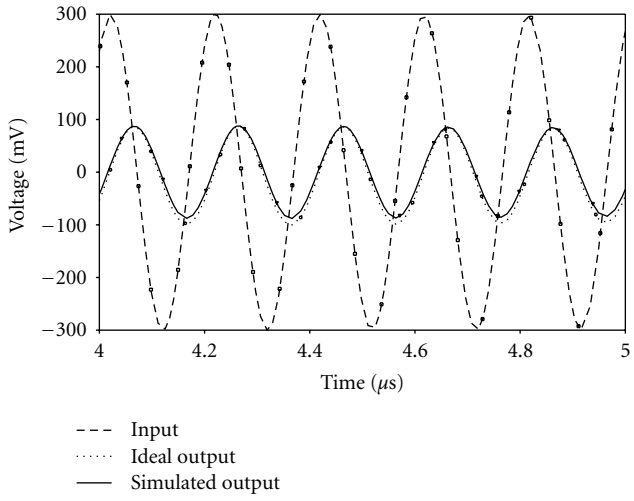

Figure 13: Transient response of double-tuned circuit of Figure 10.

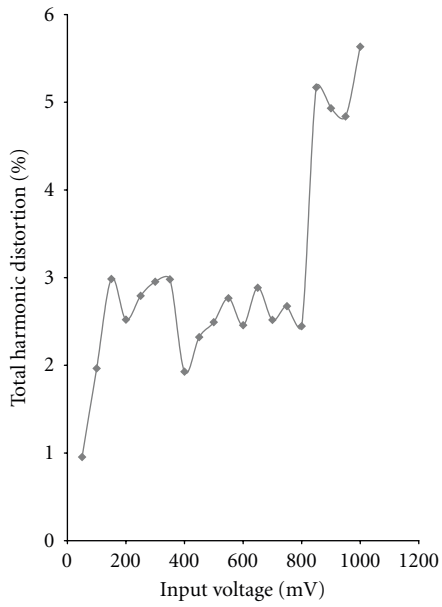

Figure 14: Variation of %THD with respect to input signal amplitude.

secondary inductances of the circuit can be independently controlled and tuned electronically via bias currents of DVCCCTAs whereas mutual coupling can be adjusted via grounded resistor. This resistor can be realized with MOS transistors. The nonideal analysis of circuit is included and as an application a double-tuned circuit is simulated.

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