Dynamic and Static Behavior of Packaged Silicon Carbide MOSFETs in Paralleled Applications

Gangyao Wang, John Mookken, Julius Rice, Marcelo Schupbach
Power Application Engineering
Cree Inc.
Durham, NC, USA

***Abstract*—There is little work done to study the nuances related to paralleling the higher speed SiC Mosfet devices when compared to Si devices. This paper deals with the parallel operation of packaged silicon carbide (SiC) MOSFETs. The parameters that affect the static and dynamic current sharing behavior of the devices have been studied. We also investigate the sensitivity of those parameters to the junction temperature of the devices. The case temperature difference for paralleled MOSFETs has been experimentally measured on a SEPIC converter for different gate driver resistance and different switching frequency, the results show the current and temperature can be well balanced for the latest generation of SiC MOSFETs with low gate driver resistance.**

***Index Terms*—Silicon Carbine (SiC), MOSFET, Parallel Operation**

I. INTRODUCTION

The paralleling of Si MOSFETs and IGBTs is done routinely and is well understood in several different applications [1-3], but not much information is available for SiC MOSFTs. Since SiC MOSFTs are relatively new and mostly available in lower current ratings, there is a great desire to parallel devices to use them for higher power applications. Comparing with commercial available SiC MOSFET module [4], the benefits of paralleling discrete parts include: (i) Heat generated by more paralleled discrete devices can be distributed evenly on the heatsink which reduces the overall peak temperatures and lowers the temperature difference between junction and ambient. (ii) The designer has the flexibility to parallel two or more devices as determined by any specific application (iii) A more cost effective solution since the high volume discrete part can be manufactured at a lower cost compared with the low volume customized part.

When paralleling two or more SiC MOSFETs, their current may not be balanced due to the Rds(on) and threshold voltage (Vth) variance from sample to sample. Fig .1 and Fig.2 shows the Rdson and Vth distribution for 30 random samples of 10A 1200V generation two (Gen-II) SiC MOSFET C2M0160120D [5] under room temperature. The maximum Rds(on) is about 1.2 times of the minimum Rds(on) for those the 30 samples, while the maximum threshold voltage is 3.08V versus minimum threshold voltage 2.48V. For the operation of the paralleled MOSFETs, the variations in Rds(on) will determine the static current sharing between the paralleled MOSFETs, while the threshold gate voltage (Vth) variances will affect the dynamic switching transient. The MOSFET with the lower Vth will switch on earlier and switch off later than the others with higher Vth. When considering parallel operation of MOSFETs, Rds(on) and Vth are critical parameters and we need to investigate their sensitivity to other devices parameters like junction temperature.

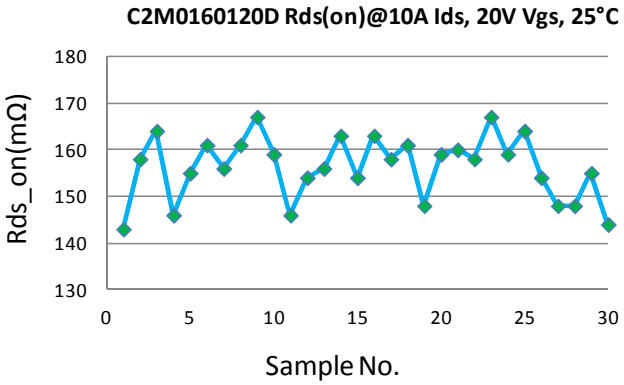


Fig. 1 On-state resistance variances

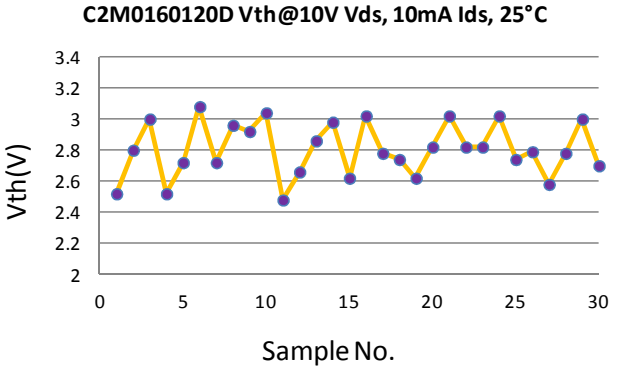


Fig. 2 Gate threshold voltage variances

In previous work [7] [8], solutions have be proposed for balancing the current during the switching transient by adding an extra feedback. These solutions will bring more cost to the customer and cannot be applied for paralleling more than two parts. The objective of this paper is to experimentally study the SiC MOSFET's self-balancing capability without adding any sensing or control circuit. The only adjustable parameters will be gate drive voltage and resistance.

The sample parts selected for this study, are the commercially available 10A 1200V first generation (Gen-I) SiC MOSFET CMF10120D [5] and Gen-II SiC MOSFET C2M0160120D [6], with similar rating, from Cree Inc. For each generation, two samples out of 30 samples with the

largest Vth variance have been chosen as the worse case for the analysis and experiment.

II. RDS(ON) CONSIDERATION FOR THE STATIC CURRENT SHARING

It is well understood that positive temperature coefficient (PTC) of the silicon MOSFET on-state resistance helps with current sharing during parallel operation and can help avoid a thermal runaway condition for all MOSFETs. Considering two MOSFETs in parallel as in Fig.3, the current flowing through each device will be:

$$I_{d1} = \frac{R_{ds(on)2}(T_{j2})}{R_{ds(on)1}(T_{j1}) + R_{ds(on)2}(T_{j2})} \cdot I_d \qquad \text{.....(1)}$$

$$I_{d2} = \frac{R_{ds(on)1}(T_{j1})}{R_{ds(on)1}(T_{j1}) + R_{ds(on)2}(T_{j2})} \cdot I_d \qquad \text{.....(2)}$$

The MOSFET with higher Rds(on) will have lower current.

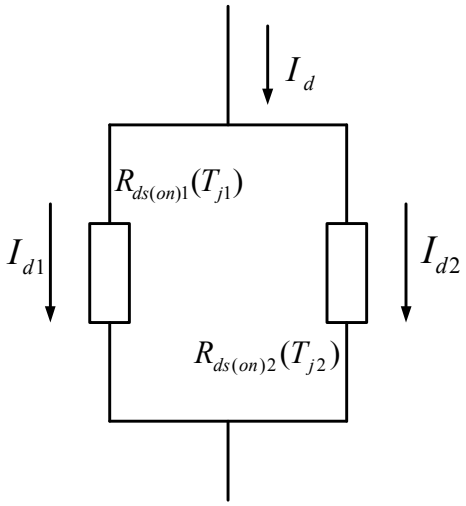


Fig. 3 Static Current Sharing

Like Si MOSFET, SiC MOSFET Rds(on) also have the PTC characteristic (Fig.4, Fig.5), the one with higher junction temperature will have less of the shared current for paralleled parts, a thermal equilibrium will be reached in the end. However, for the SiC MOSFET, such temperature dependency for the Rds(on) is not as strong as Si MOSFET. As reported in [9], the Rds(on) under 150 °C is 2.6 times of the Rds(on) under 25 °C for typical 600V Si CoolMOS, but for SiC MOSFET, it is only 1.2 times for CMF10120D and about 1.5 times for C2M0160120D. Moreover, the SiC MOSFET on-state resistance is highly dependent on the Vgs as shown in Fig.4, the on-state resistance even shows a negative temperature coefficient (NTC) with 16V gate source bias for CMF10120D. This is because the MOSFET Rds(on) is mainly made up of three components: channel resistance (Rch) which has an NTC, JFET region resistance (Rjeft) has a PTC, and drift region resistance (Rdrift) also has a PTC. The Rch will become dominant for low Vgs, so the overall Rds(on) will show an NTC characteristic.

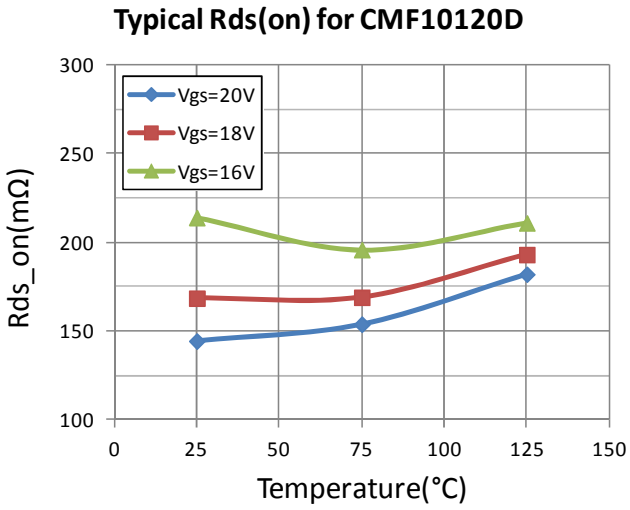


Fig. 4 Typical Rds(on) for CMF10120D

The C2M0160120D shows stronger Rds(on) temperature dependency due to the improved channel resistance(Fig.5). It is desired to use higher turn-on voltage to ensure current sharing in parallel operation as well as reducing conduction loss.

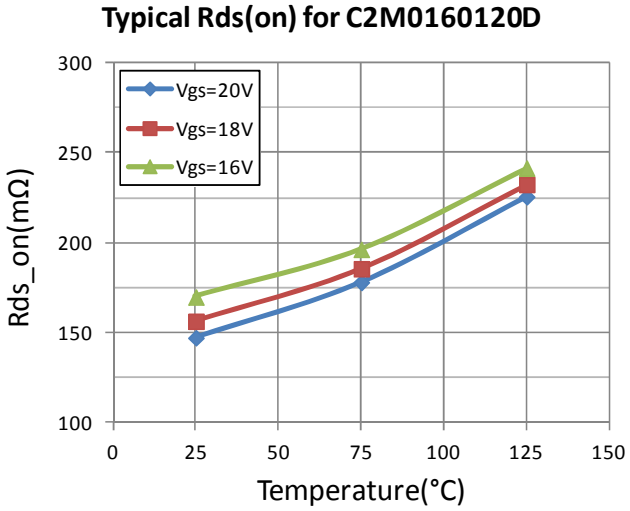


Fig. 5 Typical Rds(on) for C2M0160120D

III. VTH CONSIDERATION FOR THE DYNAMIC CURRENT SHARING

Without considering switching loss, the paralleled SiC MOSFET current and temperature can be balanced through the PTC characteristic of the Rds(on), unfortunately the switching loss cannot always be equal if the threshold voltage is different for the two paralleled MOSFETs. Two samples with minimum (sample A) and maximum (sample B) Vth from 30 samples have been chosen separately for both Gen I and Gen II MOSFETs, their parameters under room temperature are listed in Table I.

Table I Threshold voltage and on-resistance

Sample	Vth(V)	Rdson(mΩ)
CMF10120D-A	2.74	133
CMF10120D-B	3.50	144
C2M0160120D-A	2.48	146
C2M0160120D-B	3.08	161

Considering the test case for two Gen-I MOSFET in parallel with the conditions: Vds=600V, 41Ω gate driver resistance (Rg) for each device and with an average total Ids=20A. Fig.7 (a) and (b) shows the turn on and turn off waveforms separately. It can be seen that the sample A with lower Vth turns on earlier than sample B and takes more current during the switching transient, its turn on loss is 252.5uJ compared with 165.2uJ for sample B. While during the turn off transient, sample A will turn off later and consequently has more turn off loss at 296.7uJ versus 81.2uJ for sample B. The switching loss difference will be converted to junction temperature difference. The junction to case temperature rise Tjc can be calculated as:

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} \qquad \text{.....(3)}$$

$$T_{jc} = (P_{sw} + P_{con}) \cdot R_{th(jc)} \qquad \text{.....(4)}$$

Sample A will have a higher junction temperature if the conduction loss and heatsink temperature are the same for both samples. Due to the NTC characteristic of Vth (Fig.6), the Vth will decrease for higher junction temperature, the switching loss difference will increase and then a positive feedback has been formed. Fortunately the PTC characteristics of the Rds(on) will help to compensate such temperature difference to some extent. It is desired and important to have less switching loss difference caused by threshold voltage variance. A smaller Rg will speed up the switching transient and reduce the switching loss, Fig.7 (c) and (d) shows the turn on and turn off waveforms for the above two Gen-I samples with 5.1 Ω Rg. Both the switching loss and its difference has been reduced less than half of the previous case with 41Ω Rg.

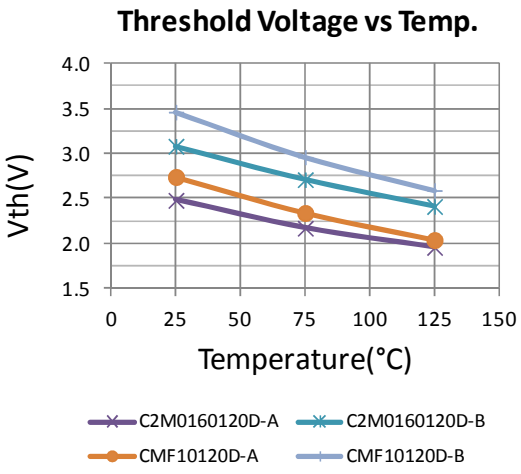
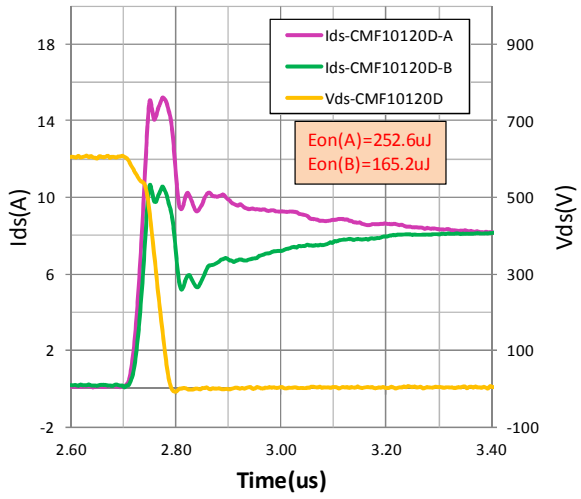
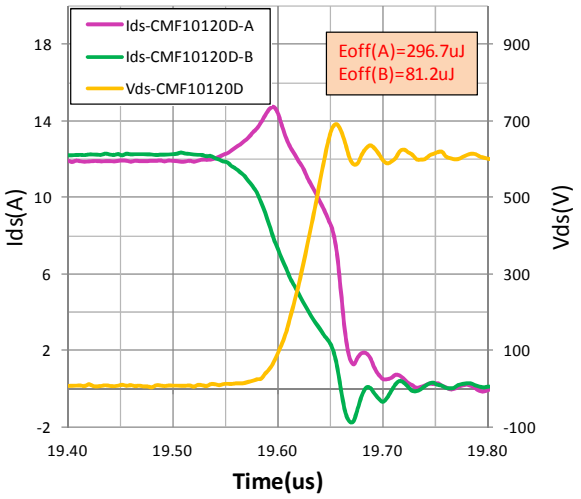


Fig. 6 Threshold voltage for different temperature



(a)



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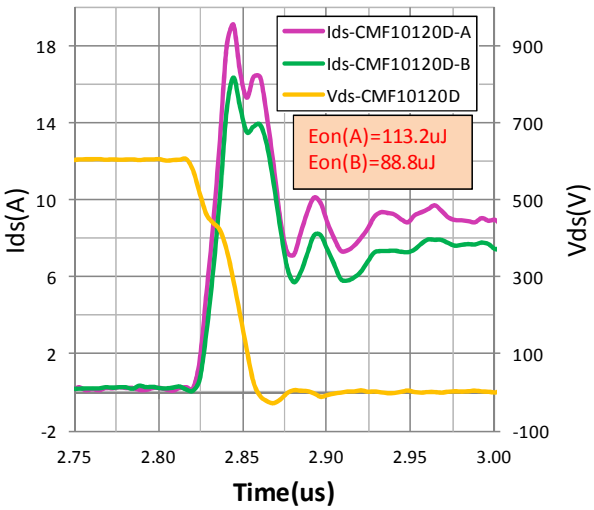

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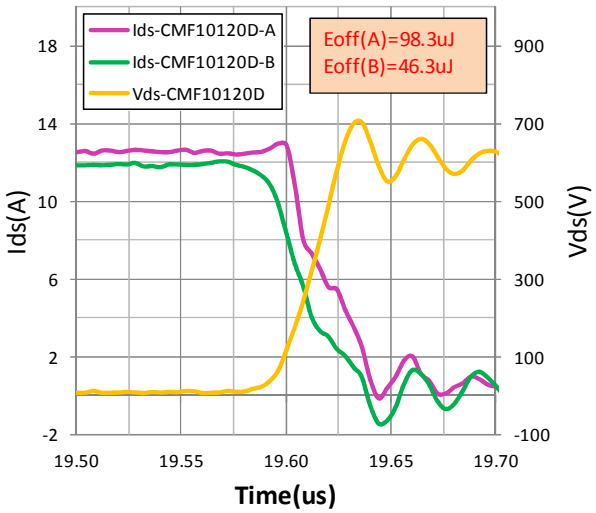
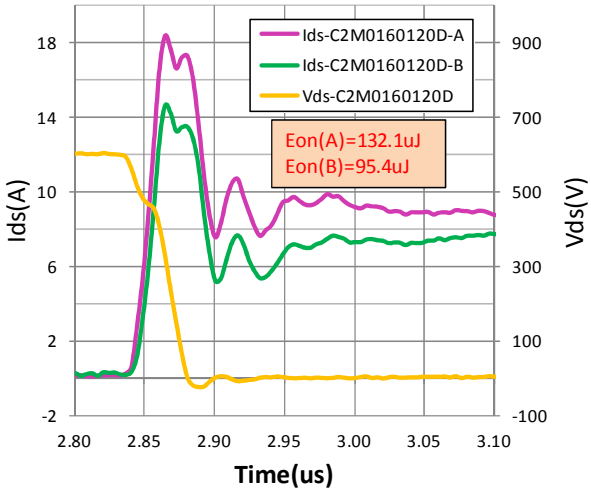


(d)

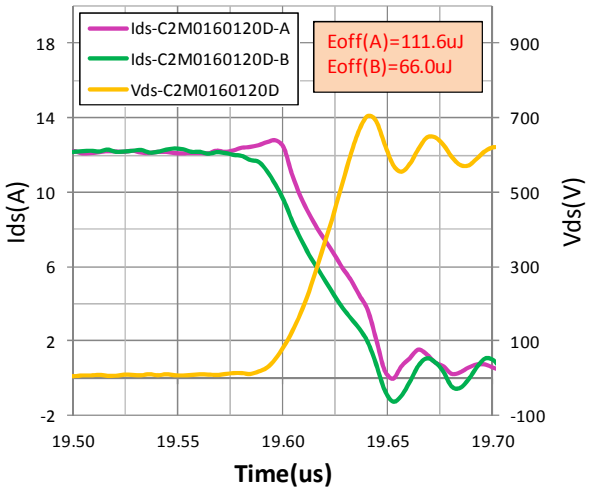
Fig. 7 Paralleled Gen-I SiC MOSFETs switching waveforms: (a) turn on with Rg=41Ω; (b) turn off with Rg=41Ω; (c) turn on with Rg=5.1Ω; (d) turn off with Rg=5.1Ω.

The same experiments have been carried for Gen-2 MOSFETs (Fig.8) which shows much lower switching loss and less loss difference. The reason is that Gen-2 MOSFETs have smaller chip area and lower Qgd, it can be switched faster than the Gen-I MOSFET with the same Rg value. With the faster switching transient, the impact of the Vth mismatch will be less significant.

Based on the previous analysis, it is clear that Gen-II SiC MOSFETs have two clear advantages for paralleling operation compared with the Gen-I SiC MOSFET. On one side, it has lower switching loss difference caused by Vth variance due to its faster switching; on the other side, the stronger PTC dependency for its on-resistance will help balance the junction temperature difference caused by the switching loss.



(a)



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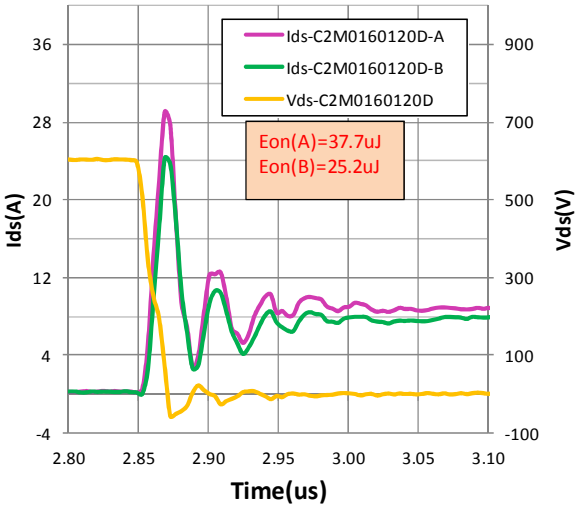

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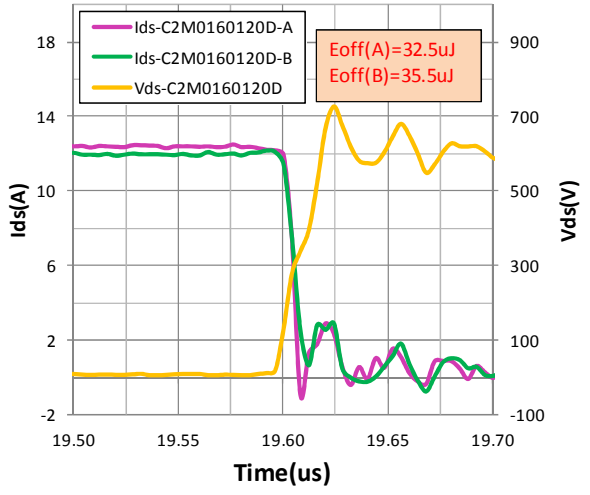

(d)

Fig. 8 Paralleled Gen-II SiC MOSFETs switching waveforms: (a) turn on with Rg=41Ω; (b) turn off with Rg=41Ω; (c) turn on with Rg=5.1Ω; (d) turn off with Rg=5.1Ω.

IV. Experimental Study of the Paralleled MOSFETS Operation for A SEPIC Converter

For the safe operation of the paralleled MOSFET, the objective is to maintain the junction temperatures for both parts as close to each other as possible. The samples with large threshold voltage mentioned in the previous sections have been put into a SEPIC converter (Fig.9) to evaluate their temperature difference for different gate driver resistance and different switching frequency. The SEPIC has a fixed 50% duty cycle. The output voltage will be equal to the input voltage according to equation (5):

$$V_{out} = \frac{D}{1-D} \cdot V_{in} \quad \cdots\cdots\cdots (5)$$

In this case the output is fed back to the input terminal of the SEPIC covnerter, the energy will be recirculated and thus limit the power demanded from the extenal power supply to the losses of the converter.

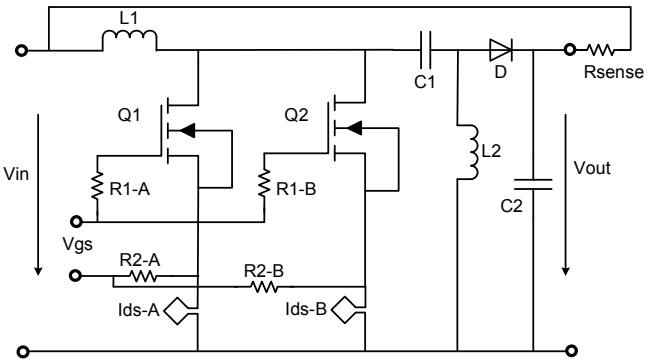

Fig. 9 SEPIC converter topology

There are two gate driver resistors R1 and R2 for each MOSFET, one has been connected to the gate terminal, the other one has been connected to the source terminal. Such an arragement is needed to ensure all drain current for each device goes through its souce terminal to the ground where a current sensing resistor has been inserted, so the current for each MOSFET can be measured seperately. Fig.10 shows the SEPIC converter hardware, the case temperaure is measured through a thermocouple for each device under test.

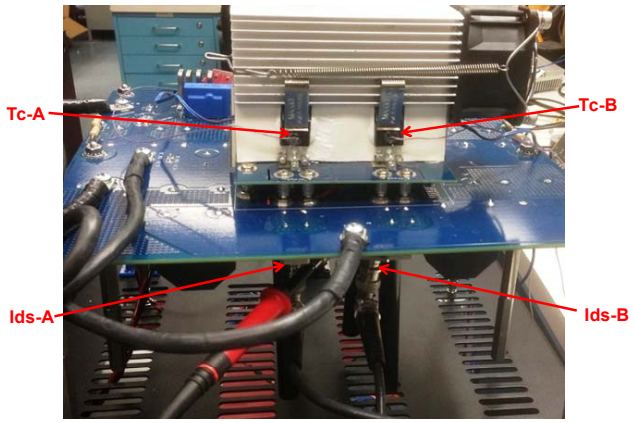

Fig. 10 SEPIC converter hardware

The voltage has been set of 600V and the circulating current is 10A which gives 6 kW power for all the experiments. For each generation MOSFET, four test cases has been tested which includes: (1) Rg=41Ω, f=30 kHz; (2) Rg=41Ω, f=100 kHz; (3) Rg=5.1Ω, f=30 kHz; (4) Rg=5.1Ω, f=100 kHz. The above Rg value includes both R1 and R2 resistance. The switching loss and case temperature has been recorded and listed in Table II. The switching transient waveforms for 30 kHz cases have been included in section III.

Table II. MOSFET Switching loss and case temperature for different test cases

	Rg (Ω)	fsw (kHz)	Psw-A (W)	Psw-B (W)	Tc-A (°C)	Tc-B (°C)	ΔTc (°C)
CMF10120D	41	30	16.5	7.4	63.0	41.9	21.1
		100	57.9	24.2	119	67.7	51.3
	5.1	30	6.3	4.1	43.7	37.5	6.2
		100	21.4	14.0	64.5	51.5	13.0
C2M0160120D	41	30	7.3	4.8	49.2	41.6	7.6
		100	23.9	16.3	72.1	58.4	13.7
	5.1	30	2.1	1.8	44.0	38.3	5.7
		100	6.8	6.1	55.6	46.6	9.0

It can be observed from Table II that: 1) Choosing smaller Rg or lower switching frequency, the switching loss and case temperature difference will be less for sample A and sample B; 2) Gen-II 10A 1200V MOSFET has lower case temperature difference compared with Gen-I 10A 1200V MOSFET under the same test conditions. 3) It is generally safe to parallel SiC MOSFET directly without adding extra balancing circuit by using a lower Rg value.

The Fig.11 and Fig. 12 shows the waveforms for the two Gen-II SiC MOSFETs under 100kHz with 41Ω and 5Ω gate driver resistance separately. The larger static current difference in Fig. 11 is caused by the higher junction temperature difference.

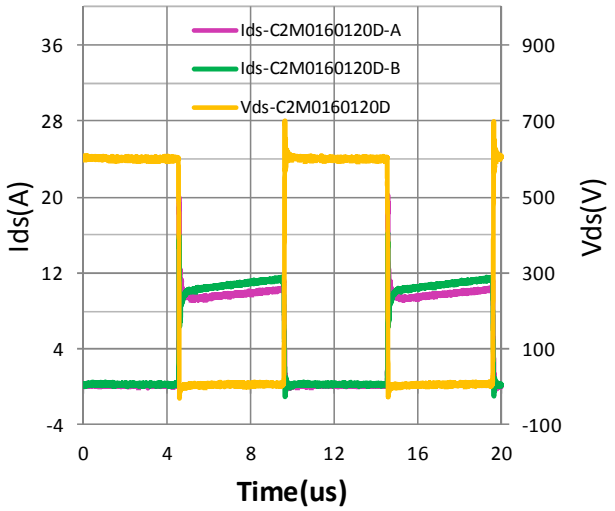

Fig. 11 Gen-II MOSFET Current sharing for Rg=41Ω, f=100 kHz

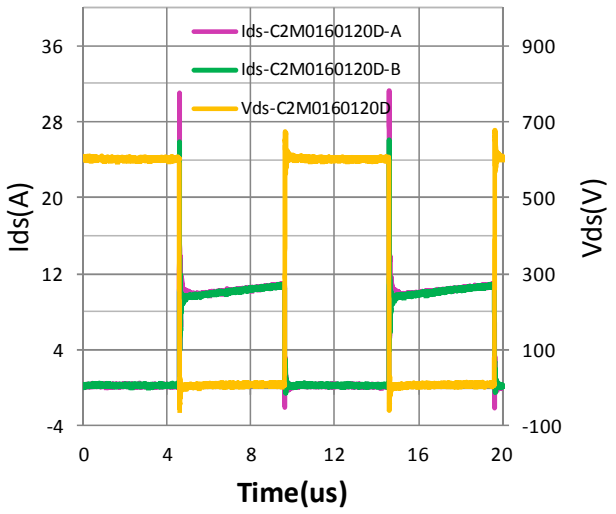

Fig. 12 Gen-II MOSFET
Current sharing for Rg=5.1Ω, f=100 kHz

V. CONCLUSION

Based on the above analysis of paralleled SiC MOSFETs operation, it can be concluded that 1) Rds(on) and Vth are two parameters that determines the static and dynamic current sharing separately for the paralleled MOSFETs; 2) high turn on gate driver voltage can reduce conduction loss; 3)lower gate driver resistance can improve dynamic current sharing and reduce switching loss difference; 4) Gen-II SiC MOSFET is more suitable for paralleling compared with Gen-I SiC MOSFET with the same current rating. For the experiment setup discussed in this paper, the PCB traces for connecting the two paralleled SiC MOSFETs are exactly symmetric and have minimized stray inductance. However, it may be difficult to have symmetric layout for some applications which means the two paralleled SiC MOSFET will have different loop stray inductance. It would be interesting to study how such inductance mismatch affects the SiC MOSFET switching behavior in continued future work.

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