Dynamic Behavior Model for High-k MOSFETs

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ABSTRACT

The use of high-k dielectrics introduces new dynamic behavior into the transistor operation. In this work, an analytical model is derived to capture the dynamic behavior of a high-k transistor through the modeling of fast transient charging effects. WKB theory is used to determine the rate of charging/discharging of the traps. The model is verified against experimental data from literature. A sub-circuit adaptation of the model is developed to implement it in a general compact model framework. The sub-circuit is solved alongside the core transistor to capture the dynamic behavior of the transistor.

Keywords: High-k, fast charging transient effects, compact model, MOSFETs.

1 INTRODUCTION

The continuous scaling of the channel length of transistor demands a simultaneous reduction in gate-oxide thickness to maintain a strong electrostatic control by the gate electrode [1]. The 2003 ITRS roadmap demands gate dielectrics with equivalent oxide thickness (EOT) less than 1nm [2]. At the same time, power constraints require gate dielectrics with a minimum physical thickness to control the gate tunneling current. High-k dielectrics with larger physical thickness for the same effective capacitance have emerged as a possible solution to this scaling problem [3].

The use of high-k dielectrics introduces new behavior into the MOSFET operation [4]. Pulsed measurements show hysteresis in drain current, threshold voltage instability and drain current degradation as shown in Fig. 1 [5]. In order to design and verify circuits with high-k transistors, the device models should be able to capture the new physics associated with the high-k transistors. In this work, an analytical model is derived to account for the fast transient charging effects. The dynamic behavior is captured through a corresponding change in the threshold voltage of the high-k transistor. SRH trapping/de-trapping rate formulation within the WKB approximation forms the basis of the model. The model is verified against experimental data from literature.

In order to adopt the high-k model into a general compact model framework, sub-circuit architecture is conceived. The sub-circuit is solved in parallel with the transistor causing the threshold voltage to change with time and hence capturing the dynamic electrical behavior of the transistor.

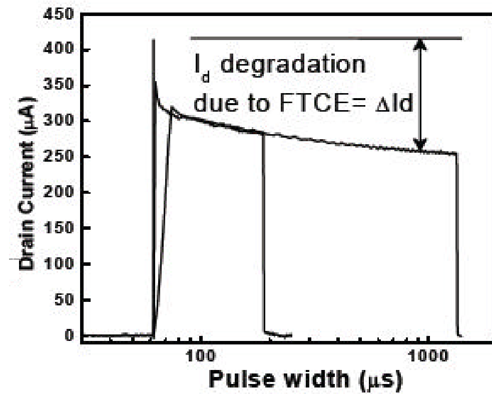


Figure 1: Drain current degradation: A sign of dynamic behavior in high-k transistors [5].

2 THEORY

The traps in the high-k gate stacks are responsible for the dynamic behavior. Trapping/de-trapping of mobile carriers into the traps changes the threshold voltage (V_{th}) of the device [6], [7].

$$\Delta V_{th} \propto n_T(t) \tag{1}$$

where, $n_T(t)$ is the filled trap density which can vary with time t. The traps could be located at the interface (interfacial traps) or inside the high-k layer (bulk traps).

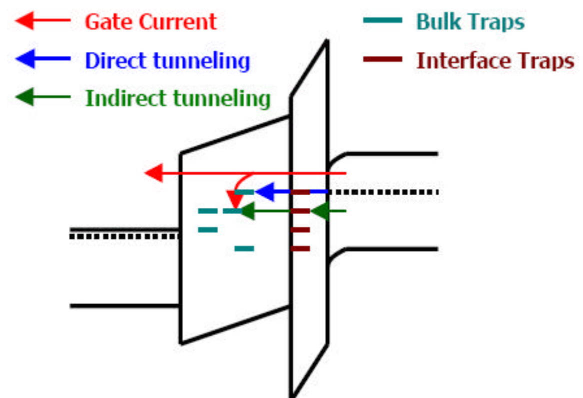


Figure 2: Possible trapping/de-trapping mechanisms of mobile carriers in high-K gate stacks.

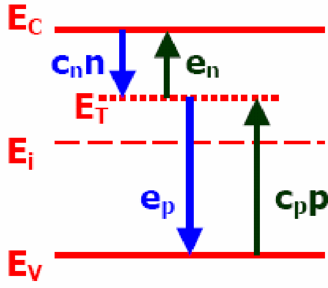


Figure 3: SRH trap/de-trap process, where E_T is the trap energy level.

Source of the carriers entering the gate stack can be the gate current, direct tunneling of carriers into the trap sites or indirect tunneling from the interfacial traps. Fig. 2 illustrates these possible trapping/de-trapping mechanisms.

2.1 Trap/ De-trap Rate Equation

The kinetics of all these mechanisms can be formulated using Shockley-Read-Hall (SRH) statistics [8]. The rate of change of filled traps can be expressed as (Fig. 3)

$$\frac{dn_T}{dt} = (c_n n + e_p)(N_T - n_T) - (c_p p + e_n)n_T \tag{2}$$

where, N_T is the available trap density, n and p are electron and hole densities, c_n and c_p are electron and hole capture constants and e_n and e_p are electron and hole emission constants. The rate equation can be further simplified under the assumption of moderate and strong inversion, where density of one carrier is dominant over the other carrier. For example, in case of N-MOSFET, we can simplify Eq. (2) to

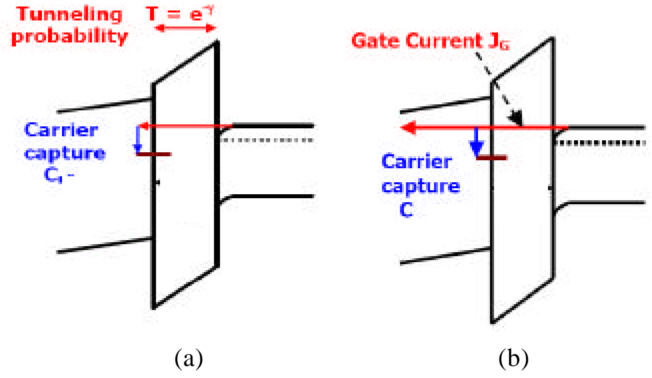
$$\frac{dn_T}{dt} = c_n n(N_T - n_T) - e_n n_T \tag{3}$$

At equilibrium, the rate of change of filled traps is zero, which allows us to express e_n, the emission constant, in terms of c_n, the capture constant.

$$e_n = c_n n \exp\left(\frac{E_T - E_F}{kT}\right) = c_n nA \tag{4}$$

Using, Eq. (4) in Eq. (3), the final rate equation governing trap/de-trap process is derived in terms of capture constant c_n, and trap energy level E_T.

$$\frac{dn_T}{dt} = c_n n(N_T - (1 + A) \cdot n_T) \tag{5}$$



(a) (b)

Figure 4: Trap filling through (a) direct tunneling and (b) gate current mechanisms

2.2 Capture Constant

The capture constant c_n is trapping process dependent. For a thin interface layer, direct tunneling of the carrier into the trap is the main source of carriers. It can be viewed as a two step process (Fig. 4a). First, the carriers tunnel from the inversion layer to the trap site with a tunneling probability T. Then they get trapped at the site with probability C. Assuming the trap is located at the bottom interface of high-k layer, using WKB approximation, the capture constant c_n can be expressed as

$$c_n = C \cdot \frac{4}{3\hbar} \frac{t_{ox}}{V_{ox}} \sqrt{2m^* q}\left(\phi_B^{3/2} - (\phi_B - V_{ox})^{3/2}\right) \tag{6}$$

where m^* is carrier effective mass, ϕ_B is barrier height, V_{ox} is voltage drop across oxide and t_{ox} is the physical thickness of the high-k dielectric.

If the dominant source of carriers for trapping is gate current (Fig. 4b), c_n is proportional to the gate current. Since, gate current is exponentially dependent on the voltage across the high-k layer and insulator thickness, the functional form of capture constant is similar to Eq. (6). Indirect tunneling of carriers from interfacial traps will also have similar exponential dependency through the tunneling probability term.

2.3 Dynamic behavior Model

The analysis so far assumed one trap site with a specific energy level and location inside the high-k gate. In reality, traps exist at different energy levels and different physical locations. Trapping of carriers could occur through several trapping mechanisms at the same time. In order for the rate equation (Eq. 5) to work under such a generalized situation, introduce fitting parameters into A and $c_n.n$ while retaining the important dependencies on physical and electrical parameters.

$$A = A1 \cdot V_g + A2 \cdot V_g^{\,2} \tag{7}$$

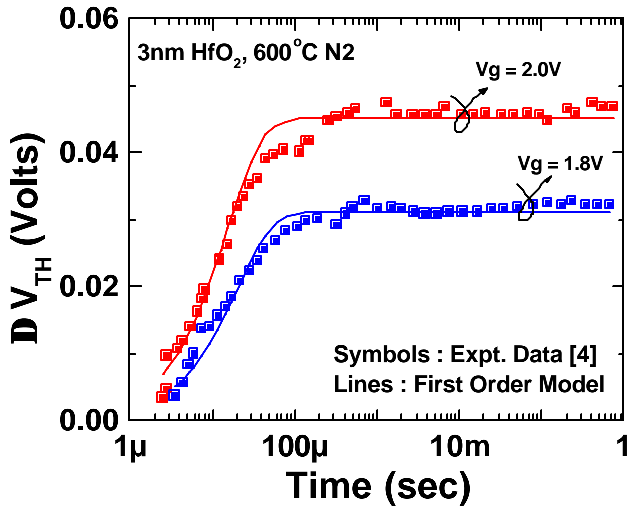


Figure 5: Verification of the first order approximation to the model for smaller V_{th} shifts.

$$c_n n = C1 \cdot (1 + C2 \cdot V_{ox}) \cdot \exp\left(-t_{oxe}\left(1 - C3 \cdot V_{ox} - C4 \cdot V_{ox}^{2}\right)\right) \quad (8)$$

where *A1*, *A2*, *C1*, *C2*, *C3* and *C4* are the model fitting parameters.

3 RESULTS AND DISCUSSION

The model is verified against the measured change in threshold voltage as a function of time for a high-k transistor. Solution to the rate equation (Eq. 5) yields filled trap density, n_T, as a function of time and the threshold voltage change is simply proportional to n_T (Eq. 1).

If the change in n_T as a function of time is small, threshold voltage shift is small. For small V_{th} shifts, the capture constant c_n and carrier density n can be assumed constant with time. This will make the rate equation a simple first order differential equation whose solution is given by

$$n_T(t) = \frac{N_T}{1 + A} \cdot \left(1 - \exp\left(-(1 + A) \cdot c_n n \cdot t\right)\right) \quad (9)$$

The first order model is verified against experimentally measured smaller V_{th} shifts [4]. Fig. 5 shows that the first order model fits the measured V_{th} shifts very well when change in V_{th} is small.

If the change in V_{th} is large, the capture constant and carrier density in the rate equation (Eq. 5) change with time. The equation is no longer a first order differential equation and must be solved numerically. Since differential equations can be solved using the numerical engine of any circuit simulator, the rate equation (Eq. 5) is implemented in the form of a sub-circuit. The sub-circuit is solved in parallel with the transistor during circuit simulation.

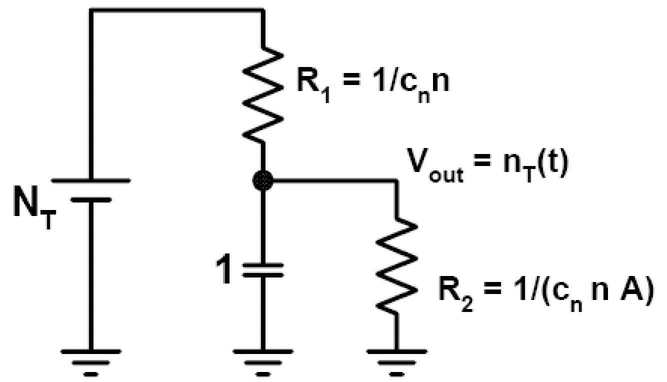


Figure 6: Sub-circuit for implementing the high-k dynamic behavior model in a general compact model framework. Two additional nodes are introduced into transistor model.

Fig. 6 shows the sub-circuit implementation of the rate equation. The magnitude of the voltage source is equal to the total density of traps. The resistor *R1* determines the carrier trapping rate and the resistor *R2* determines the de-trapping rate. Voltage across the capacitor with a capacitance of 1F yields the filled trap density $n_T(t)$. The filled trap density is then used inside the core transistor model to correct the threshold voltage dynamically and hence capture the observed dynamic effects in the high-k transistor.

Fig. 7 shows the model verification for larger V_{th} shifts. The first-order differential equation (Eq. 9) cannot match the experimental data for large V_{th} shifts. The complete model, Eq. 5, is used to fit the experimental data with the use of fitting parameters introduced in Eq. 7 and Eq. 8. Good fit is achieved to the experimental data, thus validating the model.

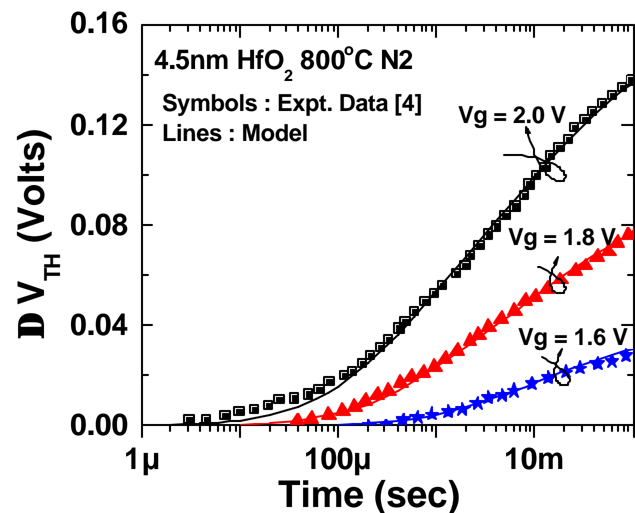


Figure 7: Verification of the complete model for larger V_{th} shifts. Rate equation is no longer a first-order differential equation and needs to be solved numerically.

4 CONCLUSION

An analytical model has been developed to capture the fast transient charging effects in high-k transistors. The model calculates the filled trap density as a function of time and uses it to correct the threshold voltage of the transistor. For small threshold voltage shifts, the model assumes the form of a simple first-order differential equation. For larger threshold voltage shifts, the model needs to be solved numerically. The model shows good fits to experimentally measured threshold voltage shifts for both small and large shifts. An efficient inclusion of the model in a compact model framework is through a sub-circuit implementation. Sub-circuit architecture for the model has been developed which when solved in parallel to the transistor, captures the fast transient charging effects.

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