

# Dynamic Internal Testing of CMOS Circuits Using Hot Luminescence

J. A. Kash, *Senior Member* and J. C. Tsang, *Senior Member*

**Abstract**—Subnanosecond pulses of hot electron luminescence are shown to be generated coincident with logic state switching of individual devices in CMOS circuits. These pulses are used to directly observe 90 ps gate delays in a ring oscillator as well as the logic switching and gate delays of a counter. By use of a detector with both space- and time-resolution, the dynamics of all the gates of the circuit are simultaneously measured. This noninvasive technique can be extended to smaller device size, as well as probing from the backside of the wafer. The optical emission may provide an alternative to electron beam testing for measuring the dynamics of high-speed CMOS circuits.

## I. INTRODUCTION

TECHNOLOGICAL advances in CMOS circuits will cause present internal test methods using electron beams to become ineffective [1]. Therefore, alternative methods to probe the operation of integrated circuits at the device level are urgently needed. We show that hot electron light emission is generated as a subnanosecond pulse coincident with the normal logic state switching of CMOS circuits. This emission can be readily observed and used to directly measure the propagation of high-speed signals through the individual gates in fully-functional CMOS circuits. As model circuits, we use CMOS ring oscillators and countdown circuits fabricated with an effective gate length of 0.6  $\mu\text{m}$ . A 90 ps internal switching delay from one state of the ring to the next is observed. Electrical waveforms circulating through the circuit can be reconstructed from the optical data, providing a detailed description of the circuit at the device level. Our results suggest that this optical emission can provide a powerful alternative to conventional electron beam techniques [2] in measuring the dynamics of advanced high-speed CMOS circuits. In addition to superior time resolution, the optical technique has the ability to simultaneously measure thousands of gates. Since the emission is intrinsic to the operation of the devices, our technique is totally noninvasive and requires no contacts or probes beyond those needed for the normal operation of the circuit.

The generation of light from normally-operating high-speed CMOS circuits is the same as that seen in MOSFET's operated in saturation [3]. The emission arises from intraband transitions of hot carriers, although controversy remains as to whether the hot carriers couple to light through scattering from phonons or impurities [4]. In a CMOS circuit under static conditions,

almost no current is drawn and there is no observable optical emission. However, when a CMOS gate switches state, a transient current does flow, and both n- and p-MOSFET's are briefly in saturation. This current consists of a portion that is needed to charge or discharge the downstream gate capacitances, as well as a parasitic portion that flows from  $V_{DD}$  to ground as the conductances of the FET's are modulated. The duration of the switching transient for our devices is typically of order 100 ps, and the hot carrier emission is coincident with the transients.

## II. EXPERIMENTAL SYSTEM

To collect time-resolved optical images, the device under test was mounted and energized on a conventional probe station. A 20X, 0.42 N.A. microscope objective imaged the circuit onto a thermoelectrically cooled microchannelplate photomultiplier (MCP) with a position sensitive resistive anode [5]. The photocathode of the MCP is multialkali with useable response (quantum efficiency  $>0.01$ ) out to about 870 nm. The MCP shows a dark count over the 25-mm diameter photocathode of 200 counts/s and a spatial resolution of better than 400 line pairs, resulting in a dark count per effective pixel of about 0.001/s. Photon timing with 100 ps resolution can also be obtained from this detector. So, using the output of the ring oscillator countdown stage as a trigger, a conventional time-correlated photon counting technique [6] allows reconstruction of the time dependence of the optical emission. (This photon timing method is effectively a sampling technique and requires a repetitive waveform.) The x- y- and time-outputs are analyzed in a coincidence mode by a three parameter multichannel analyzer, with image analysis performed on a conventional PC. After integration over several million detected photons, the three-dimensional histogram represents the complete spatial and temporal record of the emission from the circuit. The integration time depends on circuit details such as the size and type of gates and the supply voltage, and ranges from several minutes to many hours. With a photocathode better matched to the infrared spectrum of the hot luminescence, integration times would be drastically reduced.

The results presented here were obtained on a 47-stage ring oscillator fabricated from CMOS inverters with an effective gate length of 0.6  $\mu\text{m}$ . Similar results have been obtained from 29-stage ring oscillators consisting of three-way NOR or three-way NAND gates fabricated from the same CMOS technology. For  $V_{DD} = 3.5$  V (the normal operating voltage

Manuscript received November 8, 1996; revised March 3, 1997.

The authors are with IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

Publisher Item Identifier S 0741-3106(97)05082-9.

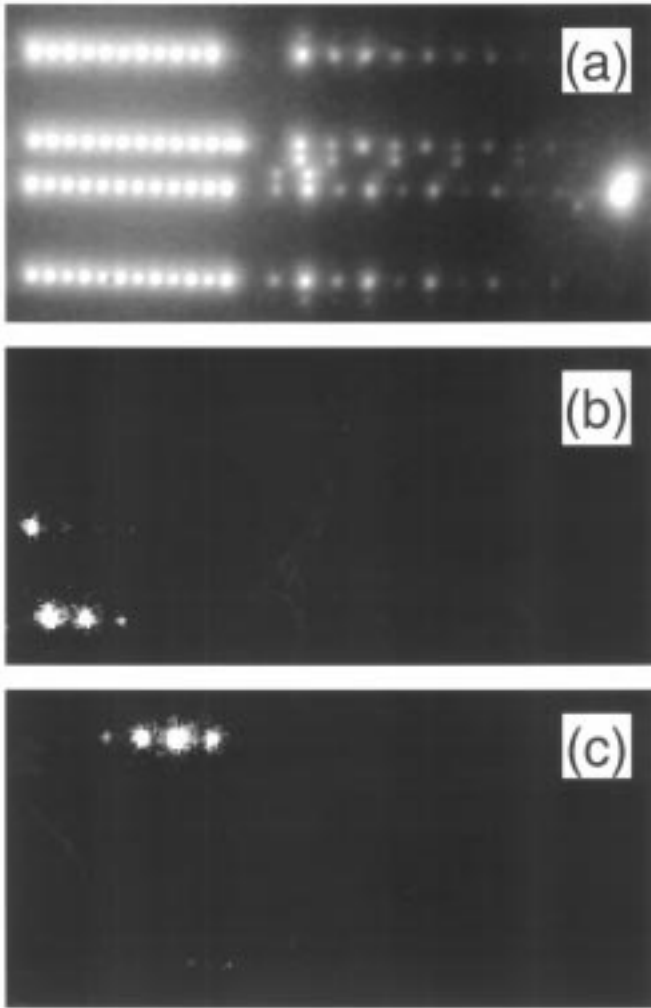


Fig. 1. (a) Time-integrated emission pattern from the circuit, taken during a 5 h acquisition with the imaging microchannelplate photomultiplier. The circuit was operated at its normal design voltage  $V_{DD} = 3.5$  V, resulting in a ring frequency of 118 MHz. The displayed image consists of 104 pixels vertically  $\times$  208 pixels horizontally ( $160 \mu\text{m} \times 320 \mu\text{m}$ ), with about seven million detected photons, of which about 200 000 are dark noise. (b) and (c) are time slices of the emission corresponding to 136 ps out of the full 271.2 ns period of the divide-by-32 countdown stage. (b) is at 3.33 ns relative to the countdown trigger, while (c) is at 4.63 ns. The grayscale for all images is logarithmic in the number of counts.

for these circuits), the ring oscillator frequency of the inverter circuit is 118 MHz, i.e., the average delay per stage is 90 ps. Attached to the ring oscillator is a five-stage (divide by 32) binary countdown circuit which produces a 100 mV output trigger into 50 ohms at 3.69 MHz.

### III. SPACE- AND TIME-RESOLVED EMISSION

Fig. 1(a) shows the time-integrated light emission from the circuit for  $V_{DD} = 3.5$  V. The four rows of light on the left side of the image are due to emission from the n-MOSFET's of the CMOS inverters. Emission from the p-MOSFET's is about 100 times weaker, and is difficult to observe against the background from the strong n-MOSFET emission. The bright spot on the far right of the figure is due to the output amplifier. The spots in the right half of the image which

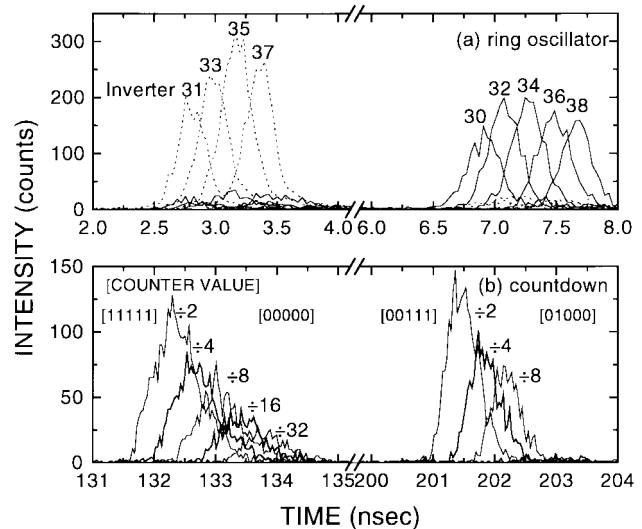


Fig. 2. (a) Time-resolved emission from the n-MOSFET's of nine of the 47 sequential inverters of the ring, corresponding to inverters at the lower left of Fig. 1(a). For clarity, all even-numbered inverters are shown as solid lines, while odd-numbered inverters are shown as dashed lines. Each data point corresponds to a 34 ps time interval. The delay between inverters 30 and 38 is 748 ps, consistent with the 90 ps delay per inverter obtained from the output frequency of the countdown stage. (b) Time-resolved emission from the time interval from the right half of Fig. 1(a) are similar; the bottom row has been selected here. The left set of peaks corresponds to changing the logic state from all ones (i.e.,  $V_{DD}$ ) to all zeroes, so each stage of the countdown emits a pulse. The right set of peaks corresponds to the counter value changing from 7 to 8, with the divide-by-2, -4, and -8 counters all switching to zero, while the divide-by-16 switches up to  $V_{DD}$ . The small pulse produced by this counter cannot be seen on this scale, but is observable. The divide-by-32 counter does not switch and hence produces no pulse in the time interval from 200 to 204 ns. The propagation delay in the countdown portion of the circuit is 400 ps per stage, which is considerably longer than that for the ring.

decrease in intensity from left to right come from the gates of the countdown circuit. The decrease roughly follows the decreasing switching rate of the countdown circuit.

Because each detected photon is labeled with arrival time in addition to x-y position, it is possible to create time-resolved images of the emission for various times. Such images are shown in Fig. 1(b) and (c) for times delayed by 3.33 and 4.63 ns relative to the output trigger. Other inverters, as well as the various gates of the countdown circuit emit light in other time slices. By arranging a series of such time slices in chronological order, a "movie" showing the relative timing of a complex circuit has been assembled. For the ring, the movie appears as a spot of light moving sequentially around the ring (skipping every other inverter as explained in the next paragraph), with the countdown chain incrementing each time the spot makes two circuits of the ring.

As an alternative means of presenting the data, Fig. 2 gives the detailed temporal dependence of the light emission shown in Fig. 1. These results were obtained by defining small rectangular regions in the image of Fig. 1(a) and plotting the time-histogram of all photons detected within that region. The traces in Fig. 2(a) represent the intensity of the light emission from the n-MOSFET's of nine sequential inverters in the ring. The emission from each gate is repeated with a period of 8.48 ns in agreement with the 3.69 MHz output of the countdown

circuit. In each full period of the ring, every inverter goes through a positive and a negative logic swing, separated by 4.24 ns. A simulation [7] of the switching of such inverters shows that the current through the n-MOSFET is far larger for the  $V_{DD}$  to ground transition at the inverter output than it is for the reverse transition. Thus, the large optical pulse for each inverter is identified as the  $V_{DD}$  to ground transition, while the small pulse is for ground to  $V_{DD}$ . The asymmetry between the positive- and negative-going transitions means that inverters immediately adjacent to the brightest inverter in Fig. 1(b) and (c) are much less bright than the next-nearest-neighbor inverters. The results in Fig. 2(a) demonstrate the ability to measure switching speeds in excess of 10 GHz. Fig. 2(b), which focuses on the emission from the countdown portion of the circuit, demonstrates the ability of the technique to generate the timing diagram for logic circuits.

#### IV. DISCUSSION

The above results have all been taken from the front side of the circuit. With the increasing complexity of CMOS circuits, a technique which can probe devices from the back side of the substrate will become essential. The hot luminescence detected here is considerably more intense at lower photon energies, including energies near and below the 1.12 eV bandgap of silicon, than it is at energies greater than 1.43 eV, where the present detector operates. We have used a photon counting silicon avalanche photodiode (APD) to detect the emission near the silicon bandgap with 300 ps time resolution. Since the APD has no spatial resolution, a 50- $\mu\text{m}$  core multimode fiber was placed in proximity to the circuit so as to detect emission from only a small area of the circuit. The light collected by the fiber was passed to the detector. To roughly simulate the effect of backside detection, a 250- $\mu\text{m}$  thick, double-side polished silicon wafer was placed in the optical path between the fiber and the APD. Because the bandgap of silicon is indirect, some photons with wavelengths between 1 and 1.1  $\mu\text{m}$  are passed by the wafer and detected by the APD. Although the signal is reduced about twenty-fold by the silicon wafer, the APD can still measure the time variation of the waveform traveling around the ring oscillator. This demonstrates that the light emission can be used to obtain detailed information about switching in CMOS circuits through the backside of the device wafer.

As CMOS devices are scaled, the gate length of the MOSFET's is shrinking faster than the supply voltage, so that the electric field in the channel is increasing. The hot luminescence intensity depends on electric field, so that smaller MOSFET's actually emit more detectable light per electron through the channel. We have verified this scaling by comparing the relative emission of photons with energy greater than about

1 eV between the (0.6  $\mu\text{m}$ , 3.5 V) devices measured in this letter and smaller (0.25  $\mu\text{m}$ , 2.5 V) devices [8]. These results show that our optical technique will be usable even as feature sizes continue to shrink.

Our results show that time-resolved optical emission microscopy has potential as a powerful tool for the characterization of dynamic processes in high-speed integrated circuits. In contrast to electron beam techniques, the optical method is capable of measuring the switching dynamics of hundreds of devices simultaneously. In addition, where electron beam testing measures the voltage on accessible circuit wiring, the optical technique is sensitive to the actual device switching. The optical technique is also fully noninvasive, and needs no vacuum. Because the hot electron luminescence is strongest below the bandgap of silicon, time-resolved measurements of this luminescence may be a practical method of obtaining circuit waveforms in integrated circuits, even where the front surface is not experimentally accessible.

#### ACKNOWLEDGMENT

The authors thank D. Vallet for providing the wafer studied here, R. W. Oldrey for equipment, and M. V. Fischetti, S. E. Laux, J. J. Welser, and J. C. McGroddy for valuable discussions.

#### REFERENCES

- [1] S. M. Kudva, R. Clark, D. Vallett, D. Ross, T. Hasegawa, G. Gilfeather, M. Thayer, S. Pabbisetty, R. Shreeve, B. Ash, J. Serpiello, K. Huffman, L. Wagner, and S. Kazmi, "The SEMATECH failure analysis roadmap," in *Int. Symp. Testing and Failure Anal.*, Santa Clara, CA, Nov. 6–10, 1995, pp. 1–5.
- [2] J. T. L. Thong, *Electron Beam Testing Technology*. New York: Plenum, 1993.
- [3] S. Tam and C. Hu, "Hot-electron-induced photon and photocarrier generation in silicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1264–1273, Sept. 1984; and Y. Uraoka, N. Tsutsu, T. Morii, and K. Tsuji, "Hot carrier evaluation of MOSFET's in ULSI circuits using the photon emission method," *IEEE Trans. Electron Devices*, vol. 40, pp. 1426–1431, Aug. 1993.
- [4] S. Villa, A. L. Lacaita, and A. Pacelli, "Photon emission from hot electrons in silicon," *Phys. Rev.*, vol. 52, no. 15, pp. 10992–10999, Oct. 1995.
- [5] C. Firmani, E. Ruiz, C. W. Carlson, M. Lampton, and F. Paresce, "High-resolution imaging with a two-dimensional resistive anode photon counter," *Rev. Sci. Instrum.*, vol. 53, no. 5, pp. 570–574, May 1982; and J. C. Tsang, "Multichannel detection and raman spectroscopy of surface layers and interfaces," in *Light Scattering in Solids V*, M. Cardona and G. Guntherodt, Eds. Berlin: Springer-Verlag, 1988, ch. 6, pp. 233–284.
- [6] S. Charbonneau, L. B. Allard, Jeff F. Young, D. Dyck, and B. J. Kyle, "Two-dimensional time-resolved imaging with 100-ps resolution using a resistive anode photomultiplier tube," *Rev. Sci. Instrum.*, vol. 63, no. 11, pp. 5315–5319, Nov. 1992.
- [7] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, 2nd ed. Reading, MA: Addison-Wesley, 1993, pp. 233–236.
- [8] J. C. Tsang and J. A. Kash, "Picosecond hot electron emission from submicron complementary metal oxide semiconductor circuits," *Appl. Phys. Lett.*, vol. 70, no. 7, pp. 889–891, Feb. 1997.