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Dynamic modeling of DC-DC converters with peak current control in double-stage photovoltaic grid-connected inverters

ABSTRACT

In photovoltaic (PV) double-stage grid-connected inverters a high frequency DC-DC isolation and voltage step-up stage is commonly used between the panel and the grid-connected inverter. This paper is focused on the modeling and control design of DC-DC converters with Peak Current mode Control (PCC) and an external control loop of the PV panel voltage, which works following a voltage reference provided by a maximum power point tracking (MPPT) algorithm. In the proposed overall control structure the output voltage of the DC-DC converter is regulated by the grid-connected inverter. Therefore, the inverter may be considered as a constant voltage load for the development of the small-signal model of the DC-DC converter, whereas the PV panel is considered as a negative resistance. The sensitivity of the control loops to variations of the power extracted from the PV panel and of its voltage is studied.

The theoretical analysis is corroborated by frequency response measurements on a *230W* experimental inverter working from a single PV panel. The inverter is based on a Flyback DC-DC converter operating in discontinuous conduction mode (DCM) followed by a PWM full-bridge single-phase inverter. The time response of the whole system (DC-DC + inverter) is also shown to validate the concept.

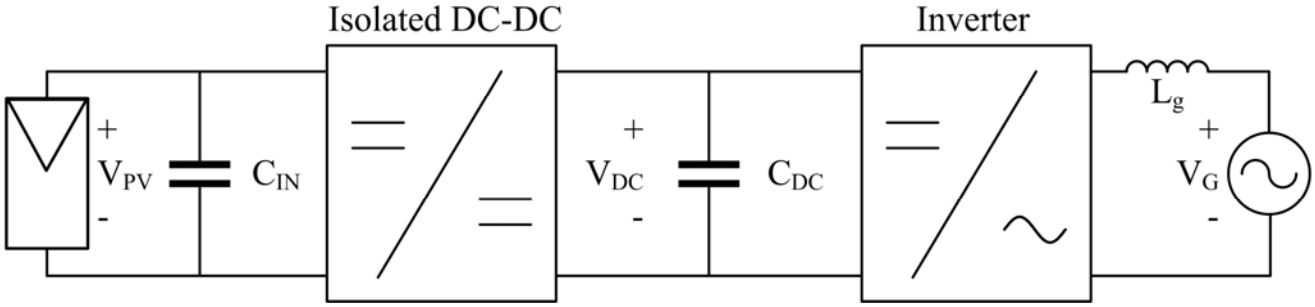
KEYWORDS

PHOTOVOLTAIC POWER SYSTEMS, DC-DC POWER CONVERSION, CURRENT MODE CONTROL, MODELING, INVERTERS.

1. INTRODUCTION

Grid-connected photovoltaic (PV) inverters may be divided into two major categories: PV inverters with a DC-DC converter and PV inverters without DC-DC converter [1]. A key factor for the choice of the power conversion topology is the need of galvanic isolation. In some countries as Great Britain or Spain isolation is mandatory at any power level. In the USA isolation is normally required because of the need of grounding of one of the PV panel outputs. References [1] and [2] provide very useful information about the current framework and state-of-the-art regarding PV grid-connected systems.

If isolation is mandatory, two options are possible: low frequency isolation by means of a bulky low frequency (LF) transformer between the inverter and the grid, and high frequency (HF) isolation by means of an isolated DC-DC converter between the PV panels and the grid-connected inverter. According to the review found in [2], one of the possibilities of the latter power conversion structure applied to PV inverters is the double-stage conversion structure with a DC-link, as depicted by Fig. 1.



[Fig.1. Double-stage power conversion structure with a DC-link for PV grid-connected inverters.]

That general topology is composed by an isolated DC-DC converter with an HF transformer and a maximum power point tracking algorithm (MPPT), followed by a grid-tied inverter. The energy decoupling between both converters is very good because of the bulk DC-link capacitance, C_{DC}, that links both stages. The energy stored in C_{DC} per volume is high, because its DC voltage is higher than the grid peak voltage, so that an overall compact design results. Due to the good energy decoupling, the controls of both power conversion stages are almost mutually independent: the DC-DC converter can be controlled to perfectly track the maximum power point (MPP) of the PV panel, whereas the inverter is controlled to produce a grid injected current in phase with the grid voltage, with a very small distortion and almost unity power factor.

In order to avoid the overcurrents associated to an eventual saturation of the HF transformer of the DC-DC converter, Peak Current Mode Control (PCC) [3] based on the measurement of current through the power transistor(s) is proposed in this work. As it is explained in section 2 high currents can be delivered to the DC-DC converter by its input capacitors, C_{IN}, placed in parallel to the panel, see Fig. 1.

PCC is an efficient method for protecting both the HF transformer and the power transistor(s), improving the PV inverter robustness.

In the proposed control structure the MPPT algorithm does not provide directly the duty cycle of the DC-DC converter as in [4], but it produces the reference voltage for the PV panel voltage as in [5] to [7]. The error between the actual PV panel voltage and its reference is the input of a panel voltage regulator which provides the peak value reference (or control voltage) of the sensed power transistor(s) current for implementation of PCC.

For the validation of the proposed control structure a Flyback DC-DC converter has been chosen. The Flyback pulse-width modulated (PWM) DC–DC power converter and its derivatives are one of the most popular converters in industry for low-power applications [8]-[12]. This converter is a common and low cost option for supplying a high output voltage from a low input voltage with a low components count and galvanic isolation. This is the case of low power (*<250 W*) double-stage inverters working from a single PV module, where the input voltage of the DC-DC converter (e.g. *30 V* at the MPP) is much lower than its output voltage (e.g. *380 V*), and the output current is relatively low (less than *1 A*). Therefore, a candidate for the DC-DC stage is the Flyback converter [2], which integrates the energy storage inductor in the high-frequency transformer magnetizing inductance, as proposed in [13].

Flyback converters are often designed to work in discontinuous conduction mode (DCM), because the value of the transformer magnetizing inductance becomes smaller, usually resulting in a reduction of the HF transformer physical size [14].

A further advantage of DCM operation is the reduction of reverse recovery problems of the output diode [15]. Besides, the dynamic control of the Flyback converter in DCM becomes simpler [16]. The main disadvantage of DCM operation is that it causes a higher RMS current in the primary switch and in the output capacitors.

It is concluded in [15] that DCM operation is usually recommended for high output voltage and low output current applications, whereas continuous conduction mode (CCM) is preferred for low output voltage and high output current converters. Therefore, DCM operation of the DC-DC Flyback converter is studied in this work, but the study can be extended to other DC-DC PWM converters operating either in DCM or in CCM. Note that the paper is focused on the control structure, and not on the converter topology. The concept can be extended to many other topologies of the DC-DC converter and to higher power levels, where the Flyback is not a good option.

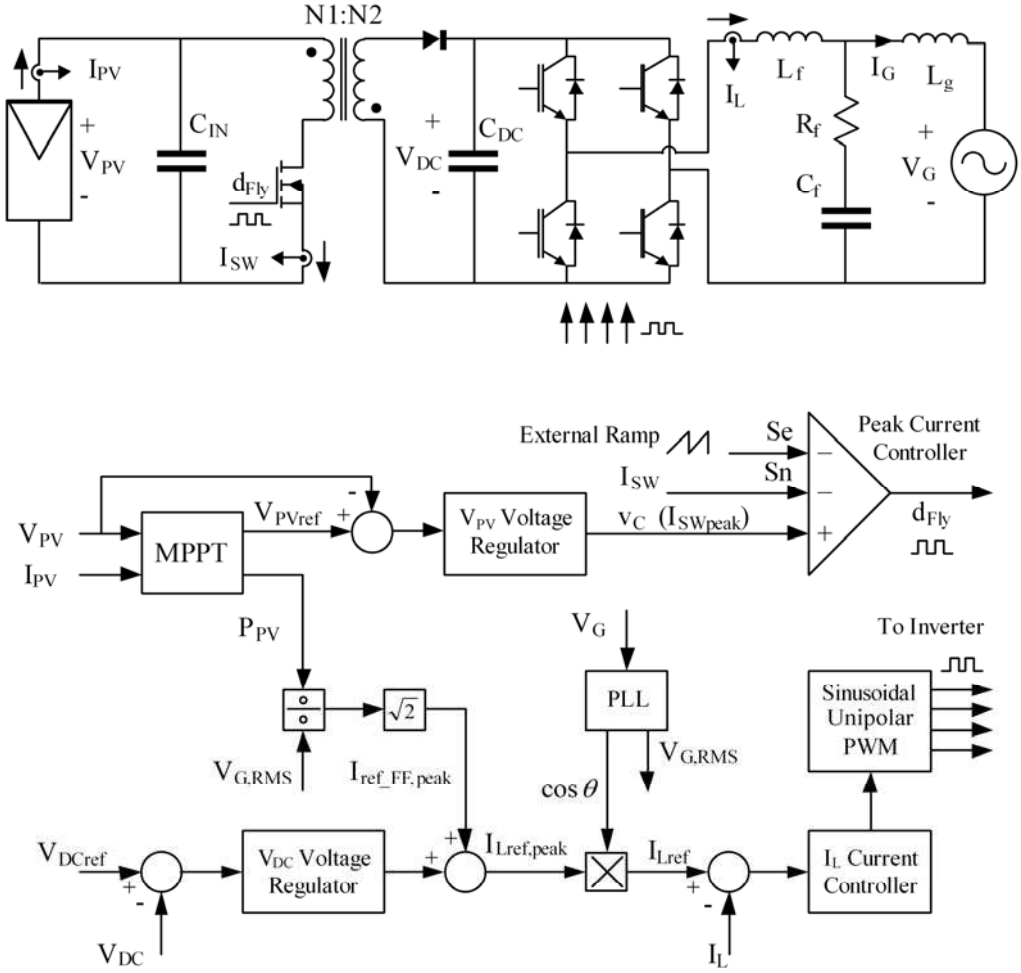
This paper is focused on the modeling and control design of the DCM Flyback converter with PCC and control of the PV panel voltage (i.e. its input voltage), which in this work follows a voltage reference provided by a Perturb&Observe (P&O) MPPT algorithm [4] [17]. Other MPPT algorithms could be valid for this application, being the study of the MPPT algorithm beyond the scope of this work.

A state-space representation of the Flyback converter small-signal model in DCM working from a PV panel is provided, from which the most important transfer functions are derived. Based on that model, the sensitivity of the PCC control loops to variations of the power extracted from the PV panel and of its voltage is studied.

Finally, experimental results of the whole inverter system, along with frequency response measurements of the Flyback converter control loops are shown, in order to validate the study.

2. DESCRIPTION OF THE PV INVERTER CONTROL STRUCTURE

Fig 2. shows the overall control structure of the proposed PV inverter system. Its most important parameters are summarized in Table I.



[Fig. 2. Proposed overall control structure of the PV inverter.]

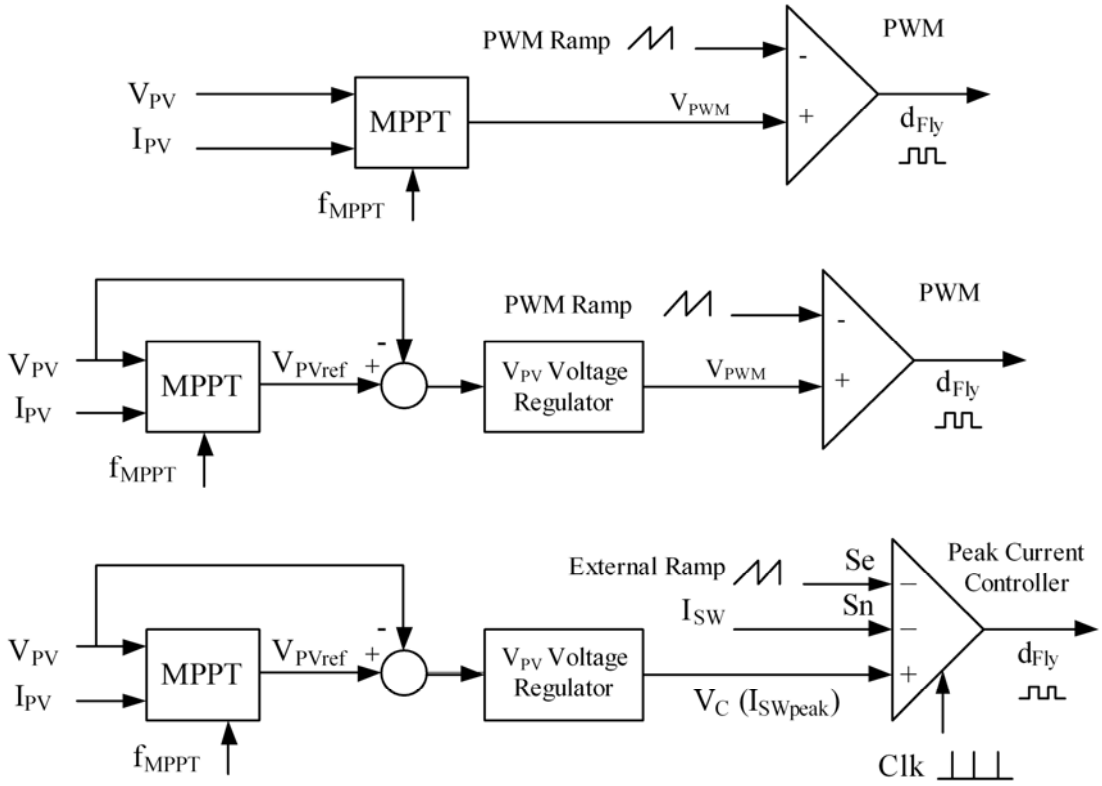
The novelty of the proposed control can be understood by observing Fig. 3, which depicts three options for the control of the DC-DC converter that provides a high enough DC voltage, V_{DC}, to the grid-tied inverter. The upper and middle schemes are the direct duty cycle control of the DC-DC converter [4] and the Voltage Mode Control [5]-[7] of V_{PV}, respectively. None of these control structures provides an overcurrent protection of the current through the active switch(es), I_{SW}.

It is worth pointing out that the PV module has an inherent overcurrent protection due to its I-V characteristic, so that the current I_{PV} in Fig. 2 is naturally limited by the value of the panel shortcircuit current. Nevertheless, the input capacitance, C_{IN}, of the DC-DC converter can be considerably high (around several miliFarads) [2] in order to deliver the input current ripple absorbed by the DC-DC converter with an acceptable switching ripple at the input voltage, V_{PV}, see Figures 1 and 2. Therefore, this input capacitance can deliver dangerous overcurrents (I_{SW}) that can damage the active switch(es) of the DC-DC converter. Those overcurrents are typical when either the HF transformer or the output inductor (if any) of the DC-DC converter saturates. The lower scheme of Fig. 3 depicts the proposed solution for the control of the DC-DC converter, which is based on Voltage Mode Control (VMC) of V_{PV} with Peak Current Control. This control

method provides an efficient cycle-by-cycle overcurrent protection. A further advantage of PCC is that the transfer function to be compensated by the voltage regulator becomes basically first order [3], avoiding the need of a complex integrator+2 poles+2 zeroes regulator, typical from VMC. Note that the concept can be extended to many topologies of the DC-DC converter.

A. Flyback DC-DC Converter operating in DCM

It is general practice to design a DCM Flyback converter to operate at the boundary between CCM and DCM for the minimum input voltage and maximum permissible load, i.e. for the maximum allowed short circuit peak primary current, I_{SCpri}, [14] [15]. In order to avoid high peak currents and voltages, the transformer turns ratio, $N=N1/N2$, is chosen in order to have a duty cycle around $D=0.5$ at the mode boundary [14].



[Fig. 3. Options for the control of the DC-DC converter. Up: Direct duty cycle control. Middle: Voltage Mode Control of V_{PV}. Down: Voltage Mode Control of V_{PV} with Peak Current Control]

In this work a short circuit peak primary current corresponding to 120% of the rated power for the minimum input voltage at the MPP ($24\ V$) and $D=0.498$ is considered, yielding the values of N and L_m shown in table I, and a short circuit peak primary current $I_{SCpri}=49.11\ A$. For a smaller load power, including rated power, the converter works in DCM with smaller values of both the duty cycle and the primary peak current.

Fig. 4 depicts a detail of the implementation of the Flyback converter with PCC control, which is composed by an inner current loop and a digital outer voltage loop. Note that the DC-link has been represented as a constant voltage source, because V_{DC} is regulated by the grid-connected inverter.

In the inner loop the instantaneous current through the Flyback switch, I_{SW}, is measured by means of a current sensor with gain R_i, and added to an external stabilization ramp [3] with slope S_e. The resulting signal, V_{Sn+Se}, is compared with the control signal, v_c, provided by the outer voltage controller. The value of v_c limits the peak value of V_{Sn+Se} performing the reset of a flip-flop and driving low the Flyback switch

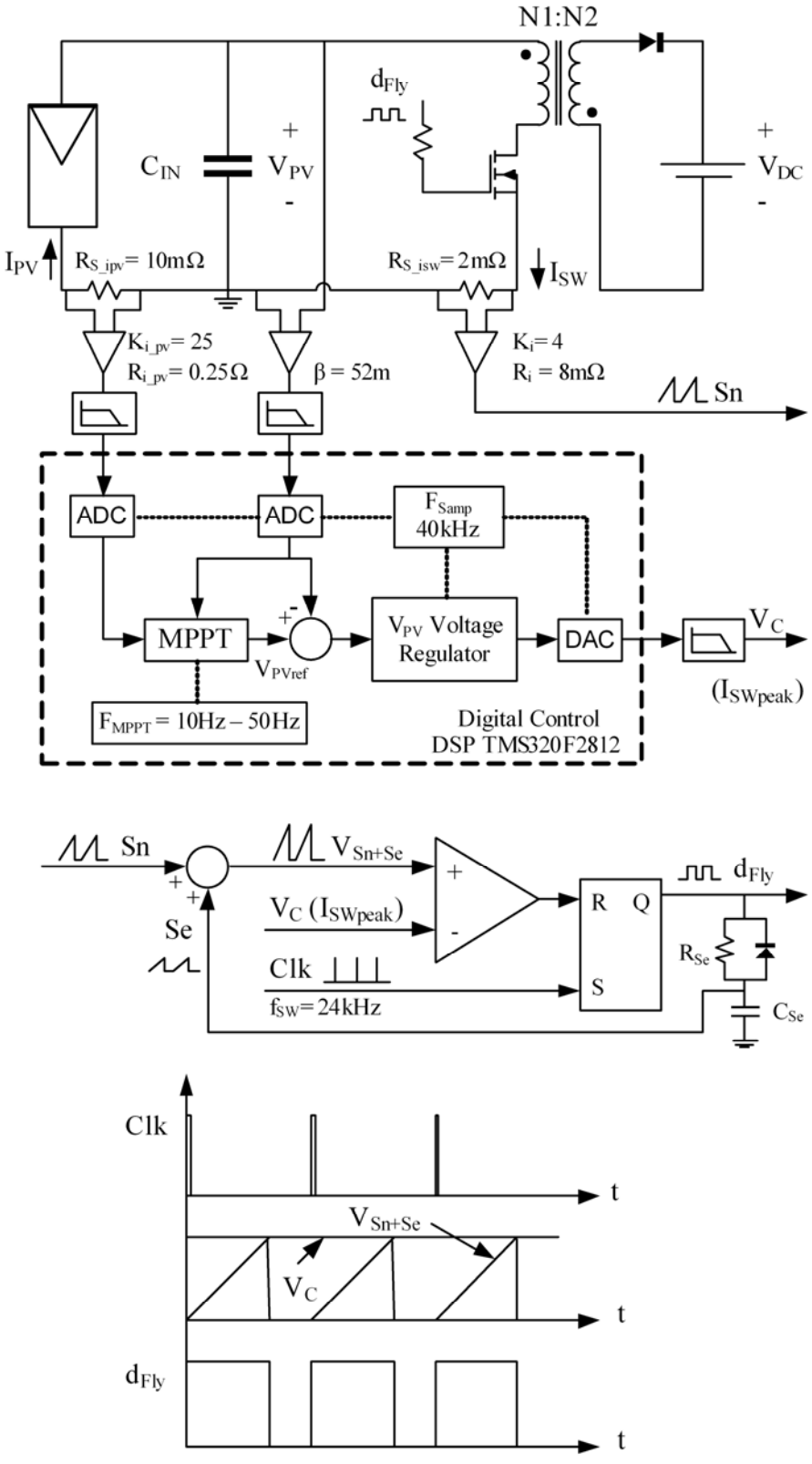
driving signal. This signal is driven high at the constant switching frequency by an external clock. Note that overcurrents in the sensed current are limited in a cycle-by-cycle basis, making PCC a very effective and fast overcurrent protection.

The slope of the sensed switch current, S_n, is added to S_e, determining the gain, F_M, of the PWM modulator with PCC. Equations (1) and (2) show the expressions of S_n and F_M, respectively, where $T_{SW}=1/f_{SW}$ is the switching period.

In (2) $m_c=1+S_e/S_n$ stands for the modulation index of PCC [3]. That parameter gives an idea about the amount of external ramp, S_e, which is necessary to stabilize the current loop. If $m_c=1$, no external ramp is used, but stability problems might arise. A high value of m_c stabilizes the current loop, but the external ramp is dominant over the sensed current ramp, S_n, reducing the advantages of current mode control. In section 3 the influence of the choice of m_c (i.e. of S_e) in the stability of the current loop will be highlighted.

$$S_n = R_i \cdot \frac{V_{PV}}{L_m} \tag{1}$$

$$F_M - \frac{1}{(S_n + S_e) \cdot T_{SW}} - \frac{1}{m_c \cdot S_n \cdot T_{SW}} \tag{2}$$



[Fig. 4. Detailed implementation of the Flyback converter with PCC control.]

In the proposed control structure a digital outer voltage loop regulates the input voltage of the Flyback converter (i.e. the PV panel voltage) instead of its output voltage, which is the common practice in

conventional DC-DC converters.

A digitally implemented P&O MPPT algorithm provides the reference for the PV panel voltage, V_{PVref}, to the voltage loop. The panel voltage, V_{PV}, is sensed with a gain β, and the voltage error acts on the PI voltage regulator, $G_V(s)$, whose output is the control voltage of the current loop.

It is worth pointing out that the PCC current loop requires instantaneous information of the sensed current for overcurrent protection, so that its digital implementation would require an extremely high sampling frequency. Therefore, its implementation has been performed in the experimental prototype with some analog circuits. As it can be observed from Fig. 4, the PCC function can be implemented by means of a clock generator, an RS flip-flop and a comparator. For the digital control of both the DC-DC and the inverter stage a development board of the Texas Instruments TMS320F2812 digital signal processor has been used.

B. Full-Bridge PWM inverter

The grid-connected inverter is a conventional Full-Bridge with sinusoidal unipolar PWM modulation [18]. The DC-link capacitance value, C_{DC}, has been chosen to have a $2 \cdot f_{grid}=100\ Hz$ ripple of $\Delta V_{DC\_100Hz}=4\ V$ at full power, i.e. around 1% of V_{DC}.

In Fig. 2 it can be observed that L_f, C_f, R_f along with the grid inductance L_g make up an LCL filter for attenuation of the switching harmonics of the current injected to the grid. The design of the LCL filter has been performed following the guidelines of [19] and [20].

In [21], it was demonstrated that the robustness of a grid connected PV inverter improves if the inverter current control loops are closed by sensing the current in the inverter side (current through L_f) instead of sensing the current in the grid side (current through L_g). Therefore, the first solution has been adopted for implementing the inverter inner current loop, as it is shown in Fig. 2.

The inverter control structure depicted in Fig. 2 is based on that of [22]. The current controller is a P+Resonant one [20] [23]. The resonant part is centered at *50Hz* and is provided with some damping as proposed in [24]. Having chosen a current sensor for I_L with a gain $K_{iL}=0.7$, the transfer function of the current controller is expressed by (3). The resulting gain crossover frequency of the current loop is $f_{Ci}=1.16\ kHz$ with a phase margin of $MF_i=50^0$.

$$G_i(s) = K_p + K_1 \cdot \frac{B_1 \cdot s}{s^2 + B_1 \cdot s + \omega_1^2} = 0.5 + 100 \cdot \frac{2 \cdot \pi \cdot 1 \cdot s}{s^2 + 2 \cdot \pi \cdot 1 \cdot s + (2 \cdot \pi \cdot 50)^2} \tag{3}$$

As it is found in Fig. 2, a Phase Locked Loop (PLL) provides the phase information ($cos\theta$) of the grid voltage in order to synthesize the reference for the current loop, I_{Lref}. In this case a single phase PLL in the synchronous reference frame (SRF-PLL) [22] has been devised following the guidelines explained in [25].

Following Fig. 2, the peak value of the current reference, $I_{Lref,peak}$, is the sum of a feedforward term $I_{ref\ FF,peak}$, and the output of the DC-link voltage regulator. The feedforward term is calculated starting from the measured PV panel power and the RMS value of the grid voltage calculated by the SRF-PLL.

Regarding the PI DC-link voltage regulator, its expression is shown by (4). Taking into account that the DC-link voltage sensor has a gain of $K_{Vdc}=6 \cdot 10^{-3}$, the resulting gain crossover frequency of the voltage loop is $f_{Cv}=12\ Hz$ with a phase margin of $MF_v=87^0$.

$$G_{v\_inv}(s) = -\left(K_p + \frac{K_i}{s}\right) = -\left(4.8 + \frac{3}{s}\right) \tag{4}$$

The control of the inverter has been fully digitally implemented with a sampling frequency of $f_{sampling}=2 \cdot f_{SW\_inv}=20\ kHz$, by using the Tustin (or bilinear transform) discretization method of the current and voltage controllers. Therefore, a conservative delay (PWM + calculation delay) of one switching period has been taken into account for the calculation of the stability margin of the fast loop, i.e. the current loop.

Further issues about the stability of full-bridge PWM inverters are addressed in [26].

3. MODELING AND CONTROL OF THE FLYBACK CONVERTER WITH PCC AND CONTROL OF ITS INPUT VOLTAGE

As depicted in Figures 2 and 4, the PCC of the Flyback converter is performed for controlling its input voltage by means of an outer voltage loop. Besides, the load is represented as a constant voltage source, because it is regulated by the grid-connected inverter. The PV panel can be dynamically modeled as a negative resistance [4].

A. Small-Signal Model

The small-signal model of the Flyback converter may be found by perturbing the averaged variables around an operating point, as expressed by (5). In (5), X and $\hat{x}$ denote the operating point value and the small-signal term of the averaged variable, x, respectively.

$$x = X + \hat{x} \tag{5}$$

A PV panel can be modeled by the linearization of the curves ipv = ipv(vpv) around an operation point close to the MPP of the panel. Indeed, at any operation point the PV panel power can be represented as (6), where the nonlinear term $\hat{v}_{pv} \cdot \hat{\imath}_{pv}$ has been neglected

$$\begin{aligned} p_{pv} = P_{pv} + \hat{p}_{pv} = v_{pv} \cdot i_{pv} = \left(V_{pv} + \hat{v}_{pv}\right) \cdot \left(I_{pv} + \hat{\imath}_{pv}\right) \\ = V_{pv} \cdot I_{pv} + V_{pv} \cdot \hat{\imath}_{pv} + \hat{v}_{pv} \cdot I_{pv} + \hat{v}_{pv} \cdot \hat{\imath}_{pv} \approx V_{pv} \cdot I_{pv} + V_{pv} \cdot \hat{\imath}_{pv} + \hat{v}_{pv} \cdot I_{pv} \end{aligned} \tag{6}$$

From (6) the operation point terms and small-signal terms of the PV panel power can be identified, following (7) and (8), respectively.

$$P_{pv} = V_{pv} \cdot I_{pv} \tag{7}$$

$$\hat{p}_{pv} = V_{pv} \cdot \hat{\imath}_{pv} + \hat{v}_{pv} \cdot I_{pv} \tag{8}$$

From (8), taking into account that $\hat{p}_{pv} = 0$ in an operating point close to the MPP, the PV panel dynamic resistance at the MPP results negative ($-R_{PV}$), as represented by (9), where $R_{pv}=V_{pv}/I_{pv}=V_{pv}^2/P_{pv}$ at the MPP.

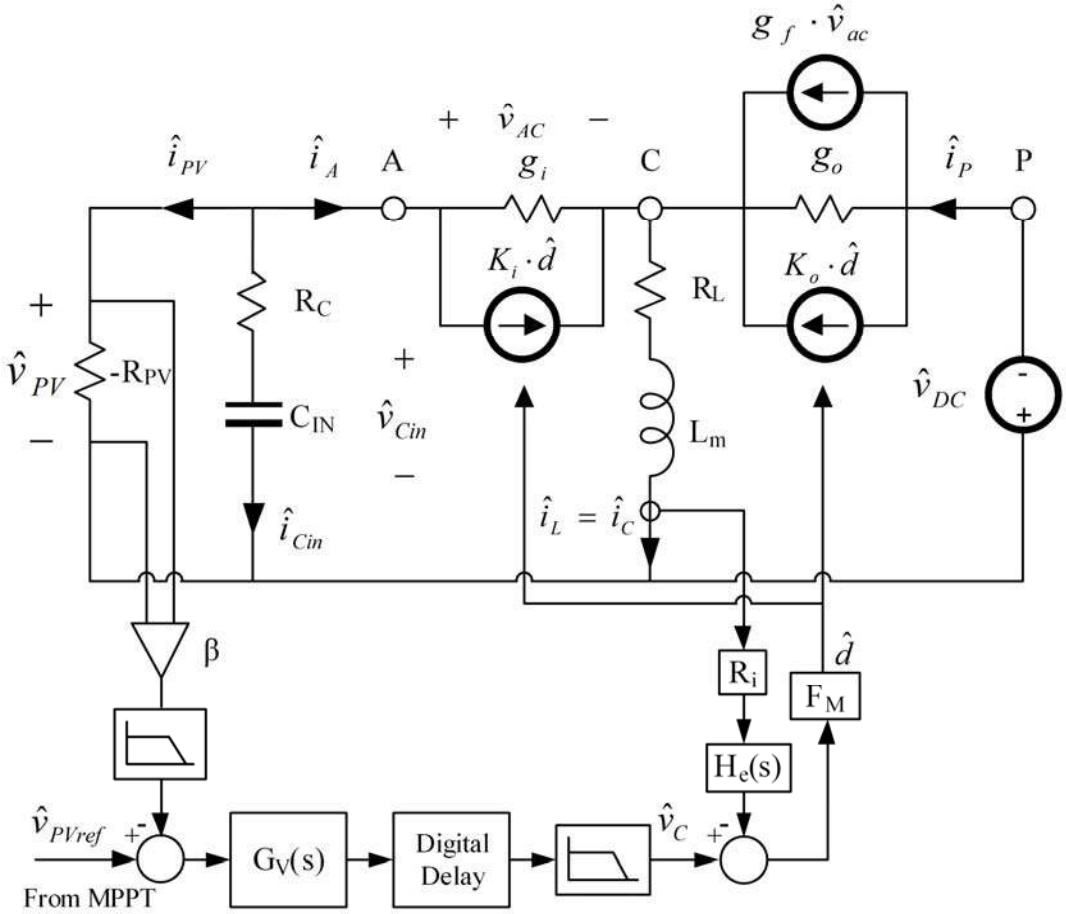
$$\left.\frac{\hat{v}_{pv}}{\hat{\imath}_{pv}}\right|_{MPP} = -\left.\frac{V_{pv}}{I_{pv}}\right|_{MPP} = -R_{pv} \tag{9}$$

Fig. 5 shows the small-signal model of the Flyback converter in DCM with PCC, obtained by using the model of the PWM switch in DCM [27] and the PCC modeling explained in [3].

Besides [27], other small-signal models for DCM DC-DC converters are valid for the dynamic study. For instance, the model of [28] could be easily adapted to Flyback converters by taking into account the transformer turns ratio. In the case of a Boost DC-DC converter, the model explained in [29] could be used. Boost DC-DC converters are common in both grid-connected and in isolated photovoltaic applications [30]. Buck-derived isolated DC-DC converters, like the soft-switching Forward converter described in [31], are also an option for this kind of applications.

In Fig. 5 the PV panel has been considered as a negative resistance, $-R_{pv}$, whereas the load is modeled as a disturbance, $\hat{v}_{dc}$, that represents the ripple at $2 \cdot f_{grid}=100\ Hz$ at the inverter DC-link voltage. The voltage

loop for the control of the PV panel voltage has been included.



[Fig. 5. Equivalent continuous small-signal model of the Flyback converter with PCC and control of the PV panel voltage.]

Note that, as it was shown in Fig. 4, the voltage loop has been implemented digitally. In the experimental prototype a TMS320F2812 Digital Signal Processor (DSP) performs the inverter control (at $f_{sampling}$=*20 kHz*), the MPPT at f_{MPPT}=*10 Hz* to *50 Hz*, and the control of the PV panel voltage at $f_{sampling}$=*40 kHz*. Therefore, 3 additional blocks have been considered when modeling the equivalent analog voltage loop of the Flyback converter:

1) The low-pass filter for the acquisition of V_{PV}. It is a second order Butterworth low-pass filter with a corner frequency of 4.5 *kHz*.
2) A delay of one sampling period ($f_{sampling}$=*40 kHz*) representing all the digital delays.
3) The low-pass smoothing filter after the digital to analog converter (DAC) providing the control voltage, v_c, to the current loop. Its characteristics are the same as those of the filter applied for the acquisition of V_{PV}.

In the current loop of Fig. 5 the PWM gain, F_M, as defined by (2), can be observed. The block, $H_e(s)$, stands for the `sampling gain' [3], a pair of complex conjugated zeroes at half the switching frequency located at the complex right half plane (RHP), i.e. non-minimum phase zeroes, whose transfer function is shown by (10).

$$H_e(s) = \frac{s \cdot T_{SW}}{e^{s \cdot T_{SW}} - 1} \approx 1 + \frac{s}{\omega_z \cdot Q_z} + \frac{s^2}{\omega_z^2} \qquad (10)$$

$$\omega_z = \frac{\pi}{T_{sw}} \quad ; \quad Q_z = -\frac{2}{\pi}$$

The small-signal model of Fig. 5 has been devised by reflecting the circuit of the transformer secondary to the primary, obtaining an equivalent Buck-Boost converter in DCM. Three 'effective' converter values seen from the primary are defined:

- Effective output voltage: $V_{DCeff} = \frac{N1}{N2} \cdot V_{DC}$
- Effective output current: $I_{Oeff} = \frac{N2}{N1} \cdot I_O$
- Effective voltage conversion ratio: $M_{eff} = \frac{V_{DCeff}}{V_{PV}}$

By applying the averaged model of the PWM switch in DCM [27]to the equivalent Buck-Boost converter, the operation point values of the small-signal model parameters are obtained. Their expressions are summarized in Table II.

From the small signal circuit of Fig. 5 an accurate small-signal state-space representation of the Flyback converter in DCM can be derived, following (11) to (21).

$$\frac{d}{dt}\mathbf{X} = \mathbf{A}\cdot\mathbf{X} + \mathbf{B}\cdot\mathbf{U} \quad ; \quad \mathbf{Y} = \mathbf{C}\cdot\mathbf{X} + \mathbf{D}\cdot\mathbf{U}$$
$$\mathbf{X} = \left[\hat{\imath}_L \;\; \hat{v}_{Cin}\right]^T \; ; \quad \mathbf{U} = \left[\hat{d} \;\; \hat{v}_{dc}\right]^T \; ; \quad \mathbf{Y} = \left[\hat{\imath}_L \;\; \hat{v}_{pv}\right]^T \tag{11}$$

$$g_{den}^2 \equiv \left(\frac{1}{R_C} - \frac{1}{R_{pv}}\right)\cdot(g_i + g_o + g_f) + g_i \cdot g_o \tag{12}$$

$$\mathbf{A} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} ; \mathbf{B} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix}$$
$$\mathbf{C} = \begin{bmatrix} 1 & 0 \\ C_{21} & C_{22} \end{bmatrix} ; \mathbf{D} = \begin{bmatrix} 0 & 0 \\ D_{21} & D_{22} \end{bmatrix} \tag{13}$$

$$A_{11} = -\frac{R_L}{L_m} - \frac{\frac{1}{R_C} - \frac{1}{R_{pv}} + g_i}{L_m \cdot g_{den}^2} \tag{14}$$

$$A_{12} = \frac{1}{R_C \cdot g_i \cdot L_m} \cdot \left[\frac{\left(\frac{1}{R_C} - \frac{1}{R_{pv}} + g_i\right)\cdot(g_i + g_o + g_f)}{g_{den}^2} - 1\right] \tag{15}$$

$$A_{21} = \frac{-g_i}{R_C \cdot C_{in} \cdot g_{den}^2} \quad ; \quad A_{22} = \frac{1}{R_C \cdot C_{in}} \cdot \left[\frac{(g_i + g_o + g_f)}{R_C \cdot g_{den}^2} - 1\right] \tag{16}$$

$$B_{11} = \frac{1}{g_i \cdot L_m} \cdot \left[K_i + \frac{\left(\frac{1}{R_C} - \frac{1}{R_{pv}} + g_i\right) \cdot [K_o \cdot g_i - K_i \cdot (g_f + g_o)]}{g_{den}^2} \right] \quad (17)$$

$$B_{12} = \frac{-\left(\frac{1}{R_C} - \frac{1}{R_{pv}} + g_i\right) \cdot g_o}{L_m \cdot g_{den}^2} \quad (18)$$

$$B_{21} = \frac{K_o \cdot g_i - K_i \cdot (g_f + g_o)}{R_C \cdot C_{in} \cdot g_{den}^2} \quad ; \quad B_{22} = \frac{-g_i \cdot g_o}{R_C \cdot C_{in} \cdot g_{den}^2} \quad (19)$$

$$C_{21} = \frac{-g_i}{g_{den}^2} \quad ; \quad C_{22} = \frac{(g_i + g_o + g_f)}{R_C \cdot g_{den}^2} \quad (20)$$

$$D_{21} = \frac{K_o \cdot g_i - K_i \cdot (g_f + g_o)}{g_{den}^2} \quad ; \quad D_{22} = \frac{-g_i \cdot g_o}{g_{den}^2} \quad (21)$$

B. Control Design and Sensitivity Study

After closing the current loop, the small-signal model of the voltage loop can be represented by means of the block diagram of Fig. 6, where several transfer functions of interest, defined in Table III, can be identified.

[Fig. 6. Block level representation of the voltage loop]

The small-signal state-space representation of (11) to (21) has been introduced in MATLAB™ to represent the most important transfer functions.

During the design stage of the current loop the choice of S_e is a key issue for obtaining a stable transfer function $V_{PV\_VC}(s)$. The Bode plots of $V_{PV\_VC}(j\omega)$ at $P_{PV}=230W$ are depicted in Fig. 7 for different values of $V_{PV} \in [24, 30, 35\ V]$ and two values of S_e: $S_e=0$ (no external ramp) and $S_e=110\ V/ms$ (the selected slope of the external ramp). Figure 8 shows the Bode plots of $V_{PV\_VC}(j\omega)$ at $V_{PV}=30V$ as a function of $P_{PV} \in [20, 50, 100, 150, 230\ W]$ for the same two values of S_e.

In the case of no external ramp, in both figures a high frequency second order complex conjugated pole pair is noticed around $f_{SW}/2=12\ kHz$ due to the effect of $H_e(s)$. When $S_e=0$ the phase contribution of that pole pair is positive. That means that the pole pair is located at the complex RHP, yielding an unstable $V_{PV\_VC}(s)$ transfer function. Note that for $S_e=110\ V/ms$, the phase contribution of the complex pole pair is negative, yielding a stable $V_{PV\_VC}(s)$. From Figures 7(b) and 8(b) it is observed that $V_{PV\_VC}(s)$ is basically first order with a negative DC gain (see the phase plots of figures 7 and 8). This first order behavior, typical from PCC, eases the design of the voltage regulator, $G_V(s)$, resulting in a simple PI. Besides, due to the negative DC gain of $V_{PV\_VC}(s)$, $G_V(s)$ needs a negative DC gain (see Table III).

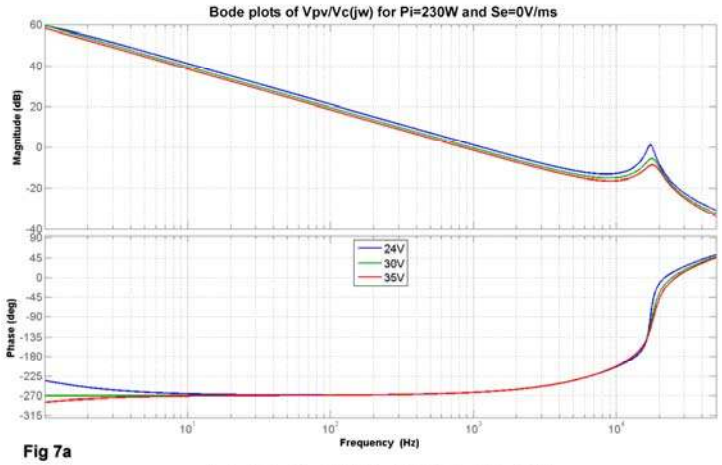


Fig 7a

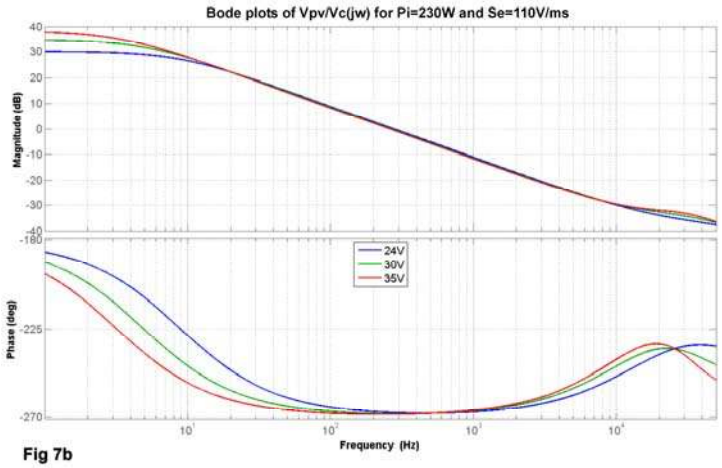


Fig 7b

[Fig. 7. Bode plots of $V_{PV\_VC}(jw)$ as a function of V_{PV} and S_e, $P_{PV}=230W$. (a) $S_e=0$, (b) $Se=110V/ms$.]

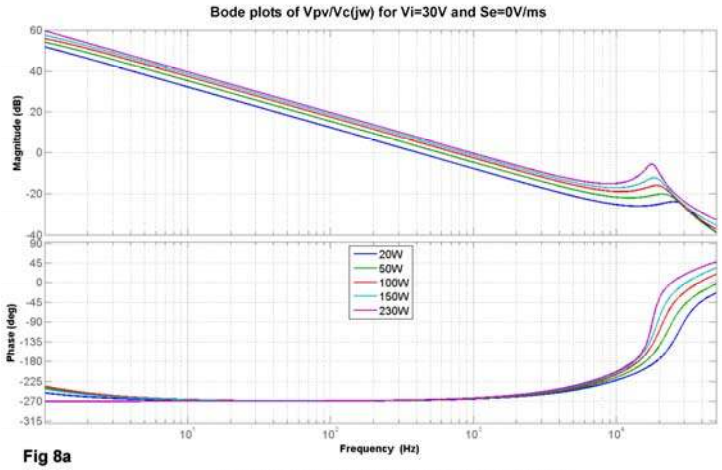


Fig 8a

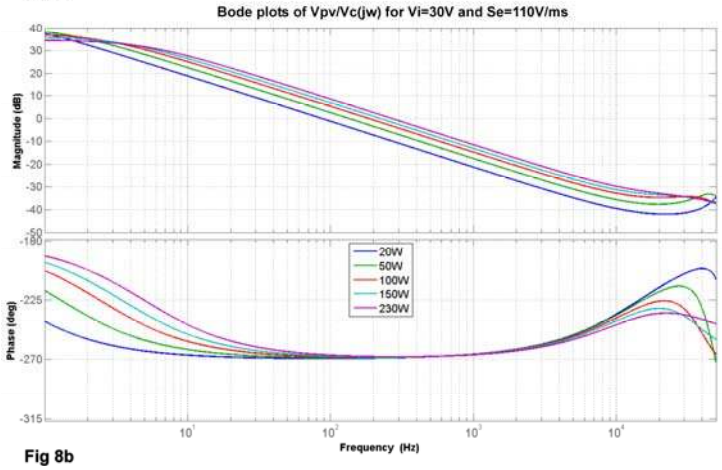


Fig 8b

[Fig. 8. Bode plots of $V_{PV\_VC}(jw)$ as a function of P_{PV} and S_e, V_{PV}=30V. (a) S_e=0, (b) Se=110V/ms.]

For the design of $G_V(s)$ two parameters of the MPPT algorithm have been considered: the refreshing frequency, f_{MPPT}, at which v_{PVref} is updated, and the incremental step of the panel voltage, Δv_{PV}, that is produced at each iteration of the MPPT algorithm. It is worth pointing out that the relationship between the incremental step in v_{PVref} produced by the MPPT algorithm, Δv_{PVref}, and the associated value of Δv_{PV} is defined by: $\Delta v_{PV}=\Delta v_{PVref}/\beta$. The adopted MPPT algorithm is a conventional P&O one acting on v_{PVref}, which can be briefly summarized by (22)

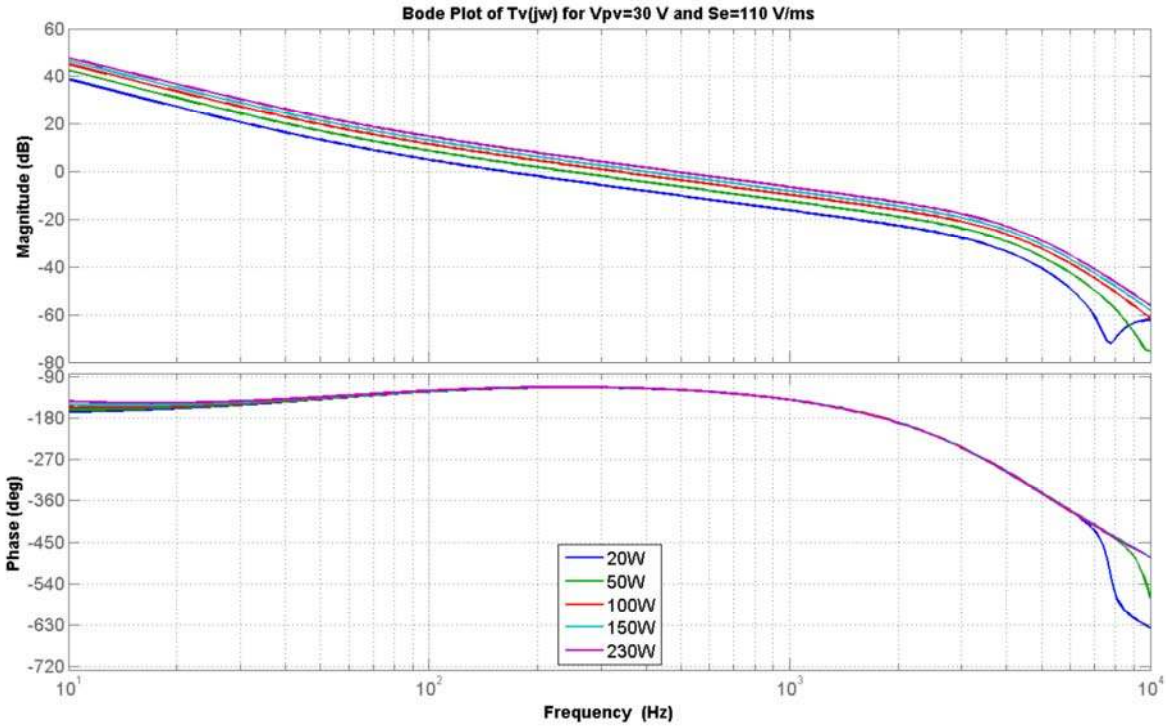
$$v_{PVref}(k+1) = v_{PVref}(k) + \Delta v_{PVref} \cdot sign[P_{PV}(k+1) - P_{PV}(k)] \quad (22)$$

, where variable k is the iteration index of the MPPT algorithm, and P_{PV} is the measured PV panel voltage at each iteration.

The design of $G_V(s)$ has been performed with two main goals. The first one is to achieve a crossover frequency, f_{Cv}, of the loop gain, $T_V(s)$, 'considerably' higher than f_{MPPT}, so that V_{PV} can follow v_{PVref}. This condition can be summarized as $f_{Cv}>n \cdot f_{MPPT}$, where n is an integer number that can be found empirically. Good results have been obtained with $n \geq 3$ if the step response of the closed loop transfer function $V_{PV\_VREF}(s)$ (Table III) is well enough damped. The second goal is to minimize the susceptibility of the control to the *100 Hz* ripple at the DC-link produced by the grid-connected inverter. Indeed, the *100 Hz* ripple at V_{PV}, ΔV_{PV_100Hz}, can be expressed as a function of the *100 Hz* ripple at V_{DC}, ΔV_{DC_100Hz}, and the gain of transfer function $A_{CL}(s)$ (Table III) at 100 Hz, following (23). As a result, the incremental step of the panel voltage, Δv_{PV}, produced by the MPPT algorithm must be higher than the highest possible value of ΔV_{PV_100Hz}, i.e. $\Delta v_{PV}=\Delta v_{PVref}/\beta>\Delta V_{PV\_100Hz}$.

$$\Delta V_{PV\_100Hz} = |A_{CL}(j\omega)|_{100Hz} \cdot \Delta V_{DC\_100Hz} \quad (23)$$

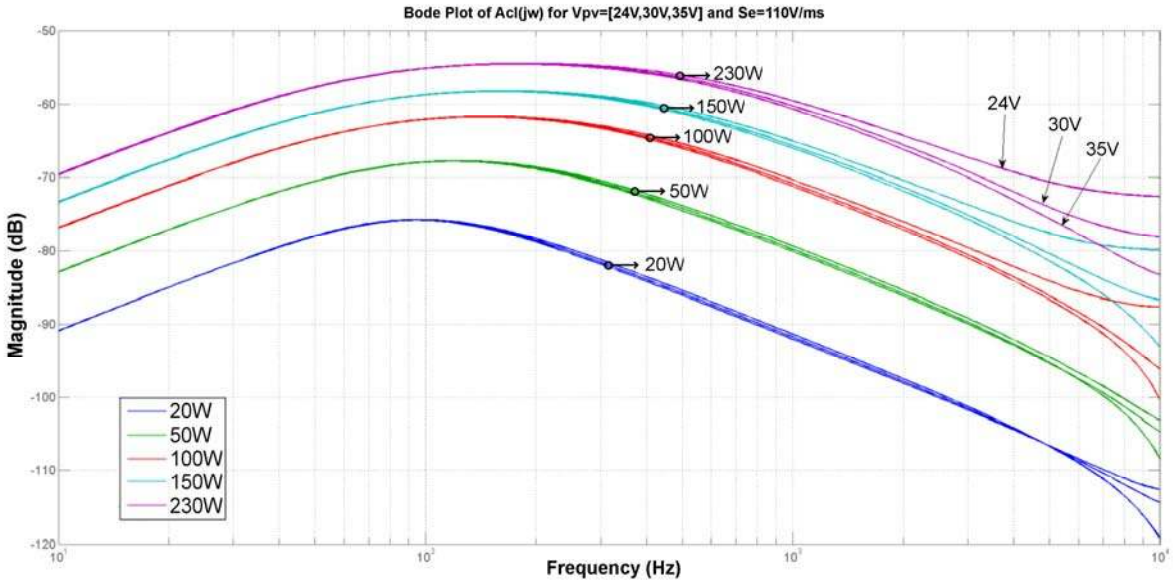
From Fig. 8(b) it can be observed that, for the chosen value of S_e, the transfer function $V_{PV\_VC}(s)$ is very sensitive to the value of P_{PV}, whereas and in the medium frequency range the sensitivity of $V_{PV\_VC}(s)$ to V_{PV} variations is very small, see Fig. 7(b). Therefore, the same effect can be noticed from the theoretical Bode plots of the loop gain $T_V(s)$, which depends on $V_{PV\_VC}(s)$ (see Table III). Fig. 9 shows the Bode plots of $T_V(j\omega)$ for V_{PV}=30V and $P_{PV}\in$[20, 50, 100, 150, 230 W]. It is observed that the crossover frequency increases with P_{PV}, ranging f_{Cv} from *162 Hz* (*20 W*) to *486 Hz* (*230 W*). The phase margin is in all cases higher than 60^0.



[Fig. 9. Bode plots of $T_V(j\omega)$ as a function of P_{PV}, for V_{PV}=30V and S_e=110V/ms]

In Fig. 10 the theoretical Bode plots of $|A_{CL}(j\omega)|$ *(dB)* have been depicted for $V_{PV}\in$[24, 30, 35 V] and $P_{PV}\in$[20, 50, 100, 150, 230 W]. It is observed that $|A_{CL}(j\omega)|$ *(dB)* increases with P_{PV}, ranging its value at 100Hz from -*75.64 dB (20 W)* to –*55 dB (230 W)*. On one hand, the maximum value of ΔV_{DC_100Hz} occurs at maximum power, taking a value of around *4V*. On the other hand, the maximum value of $|A_{CL}(j\omega)|$ *(dB)* at *100 Hz* is also obtained for maximum power, resulting –*55 dB*, i.e, $1.78 \cdot 10^{-3}$ in a linear scale. From (23) it can be calculated that the maximum expectable value of ΔV_{PV_100Hz} is: $4V \cdot 1.78 \cdot 10^{-3} = 7.12\ mV$. Therefore, the MPPT algorithm must produce a value $\Delta v_{PV} > 7.12\ mV$. In fact the minimum practical value of Δv_{PV} is usually much higher considering time-varying atmospheric conditions and the I-V curve of the PV panel [7].

It can be observed from Fig. 10 that the sensitivity of $A_{CL}(s)$ to V_{PV} variations is very small.



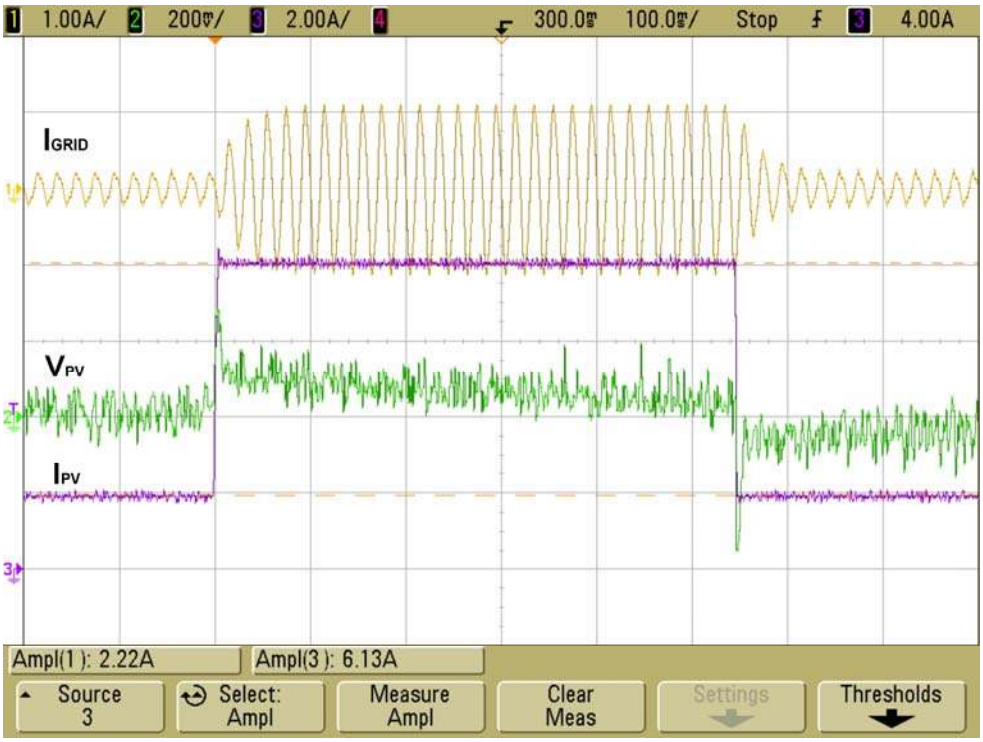
[Fig. 10. Bode plots of $|A_{CL}(j\omega)|(dB)$ as a function of P_{PV} and V_{PV}.]

4. EXPERIMENTAL RESULTS

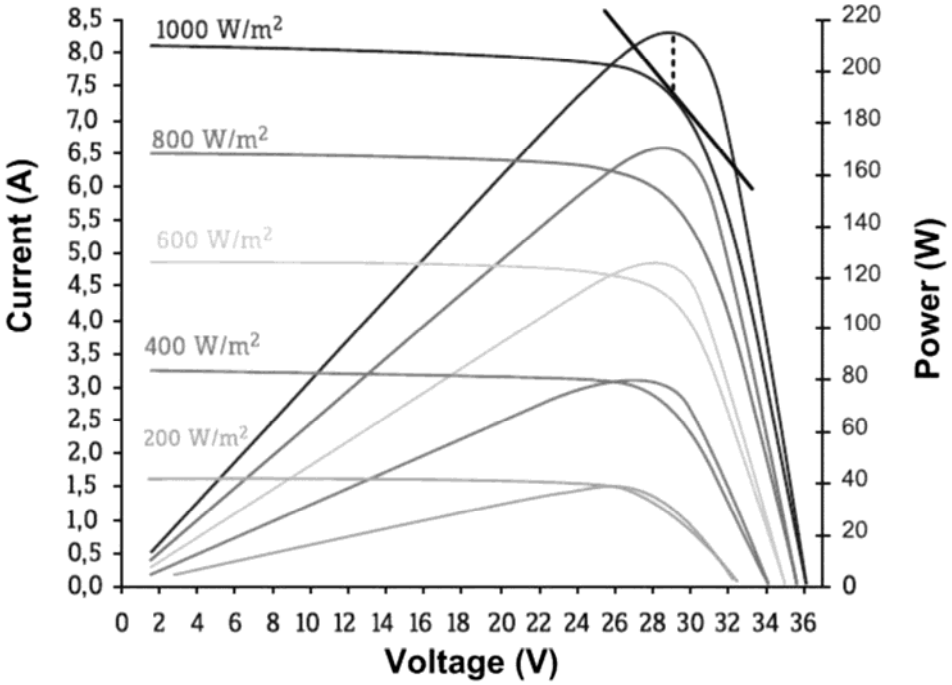
All the experimental results of this section have been performed with both stages (DC-DC and inverter) in operation, in order to validate the dynamics of the whole inverter system. The *230 W* prototype characteristics have been summarized in Table I, whereas the adjustment of the controllers has been described in previous sections. As depicted in Fig. 4, a TMS320F2812 Digital Signal Processor (DSP) performs the inverter control, the voltage controller of the Flyback converter and the MPPT.

A first large-signal stability test of the whole inverter has been performed by connecting it to a DC power supply configured as a current source that undergoes a sudden step in I_{PV} from *2 A* to *8 A* and back to *2 A*. The resulting waveforms are shown in Fig. 11. Note that this behavior of the input current does not correspond to a PV panel (it is too quick), because irradiance changes are usually slower. Nevertheless, the test is useful to demonstrate the robustness of the dynamics of the proposed control structure to fast transients. In Fig. 11 the voltage loop works from a constant reference voltage, adjusted to keep a constant value of V_{PV}=*29 V*. In this case the MPPT is disabled, because the input source does not correspond to the I-V curve of a PV panel. It can be observed from Fig. 11 that the dynamic response of both the grid injected current, I_{GRID}, and of V_{PV} is stable and well damped.

The rest of experimental results to be shown have been obtained by connecting a programmable DC power supply AMREL SPS800-12-D-013 to the PV inverter input. For these tests an I-V curve of a commercial PV panel SLK60P6L from the company *Siliken S.A.* has been programmed in the DC power supply. The MPP of the selected I-V curve is characterized by: V_{PV_MPP}=*29 V*, P_{PV_MPP}=*182 W*, Irradiance≈*900 W/m*^{2}. Fig. 12 shows the I-V curves of the commercial PV panel that has been emulated.



[Fig.11. Large-Signal Response of I_{GRID} (yellow, *1 A/div*) and V_{PV} (green, *0.2 V/div*, AC coupled) at a constant V_{PV} reference to an input current step I_{PV} (purple, *2 A/div*) from *2 A* to *8 A* and back to *2 A*. Time Scale=*100 ms/div*.]



[Fig.12. I-V and P-V curves of a photovoltaic panel SLK60P6L manufactured by Siliken S.A.]

A. Frequency Response Measurements of the voltage loop gain, $T_V(s)$, of the Flyback converter at the MPP.

The small-signal model of the Flyback converter with PCC and control of its input voltage has been

validated by means of measurements of the voltage loop gain, $T_V(s)$, at different power levels. The measurement has been performed by means of an NF Corporation FRA5097 frequency response analyzer following the procedure of [32], injecting a disturbance of *10mV* in the voltage loop, at the output of the DAC filter. For a clean measurement of the Bode plots the MPPT algorithm has been disabled, avoiding the typical small steps that the panel reference voltage undergoes around the MPP. In this case the voltage loop works from a constant reference voltage that achieves the MPP of the I-V curve of the PV panel that has been programmed in the input DC power supply that is emulating the panel. The reference voltage is adjusted inside the DSP to obtain a panel voltage: $V_{PV\_MPP}=29\ V$. Figure 13 depicts the experimental and theoretical Bode Plots of $T_V(s)$ at $V_{PV}=29\ V$ for two different values of P_{PV}: *50 W* and *150 W*.

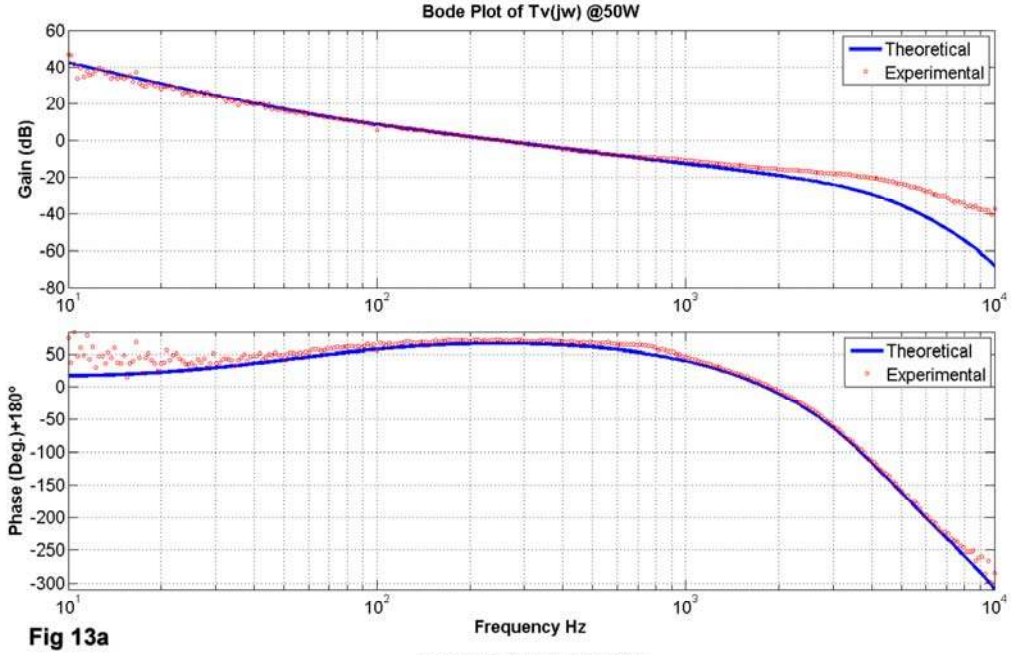


Fig 13a

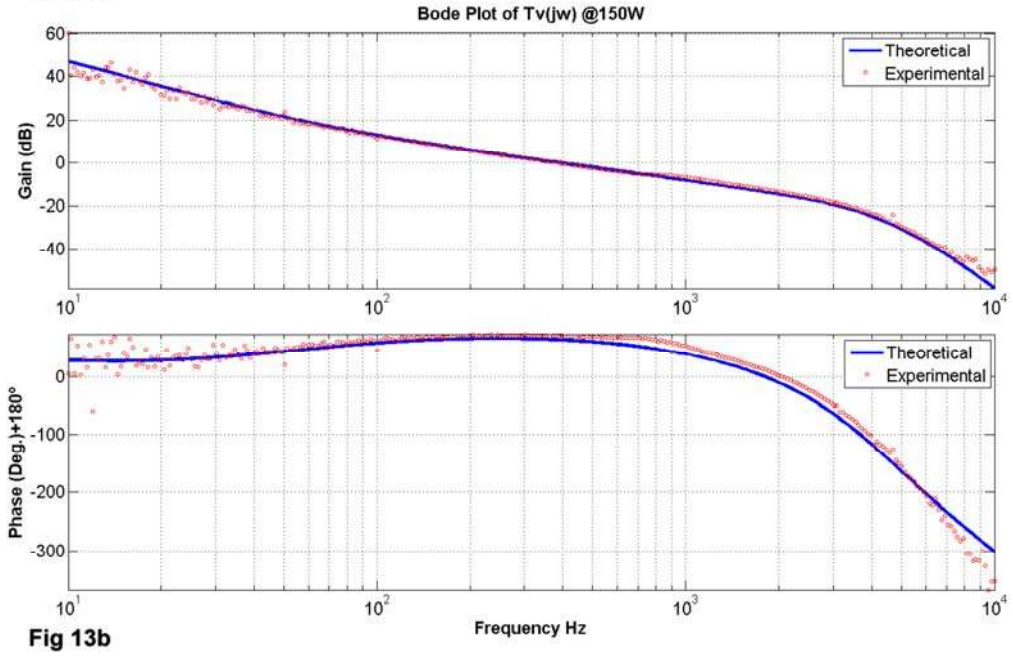


Fig 13b

[Fig. 13. Experimental and theoretical Bode plots of $T_V(j\omega)$ at $V_{PV}=29\ V$ for two values of P_{PV} : (a) $P_{PV}=50\ W$, (b) $P_{PV}=150\ W$.]

Note that due to the negative feedback of the voltage loop, the measured phase is that of $T_V(s)$ plus 180^0. Therefore, the phase margin can be read directly from the phase plots. It is worth pointing out that for properly comparing the experimental phase plots with the theoretical ones, a 180^0 positive phase shift has been added to the theoretical Bode plots in Fig. 13. It can be observed a very good agreement between the theoretical and experimental Bode plots. As expected, when the injected power increases, so does the experimental crossover frequency of $T_V(s)$: $f_{CV}=220\ Hz$ at $P_{PV}=50\ W$, and $f_{CV}=360\ Hz$ at $P_{PV}=150\ W$. The measured phase margin is in both cases higher than 60^0.

B. Response of the PV inverter to a reference voltage provided by a conventional P&O MPPT algorithm.

The experimental response of the whole PV inverter to a reference, v_{PVref}, provided by a conventional P&O MPPT algorithm is shown in this section.

The chosen MPPT algorithm update frequency for the tests is the maximum empirical one, $f_{MPPT\_max}=50\ Hz$. This value of f_{MPPT} is consistent to the crossover frequency of the voltage loop, ranging from *162 Hz* (*20 W*) to *486 Hz* (*230 W*). Two values of the incremental step of the panel voltage, Δv_{PV}, commanded at each iteration of the MPPT algorithm have been tested: $\Delta v_{PV}=600\ mV$ and $1V$. Figure 14 shows the start-up transient response of V_{PV}, I_{GRID} and V_{DC} when the DC power supply emulating the PV panel is connected to the inverter. The input capacitance C_{IN} is initially discharged. Therefore, the initial value of V_{PV} is zero. Note that the start-up transient exhibits no oscillations, reaching the MPP in steady-state ($V_{PV\_MPP}\approx 29\ V$, $P_{PV\_MPP}\approx 182\ W$). In steady-state V_{PV} follows the typical stepped reference of a P&O algorithm around the MPP.

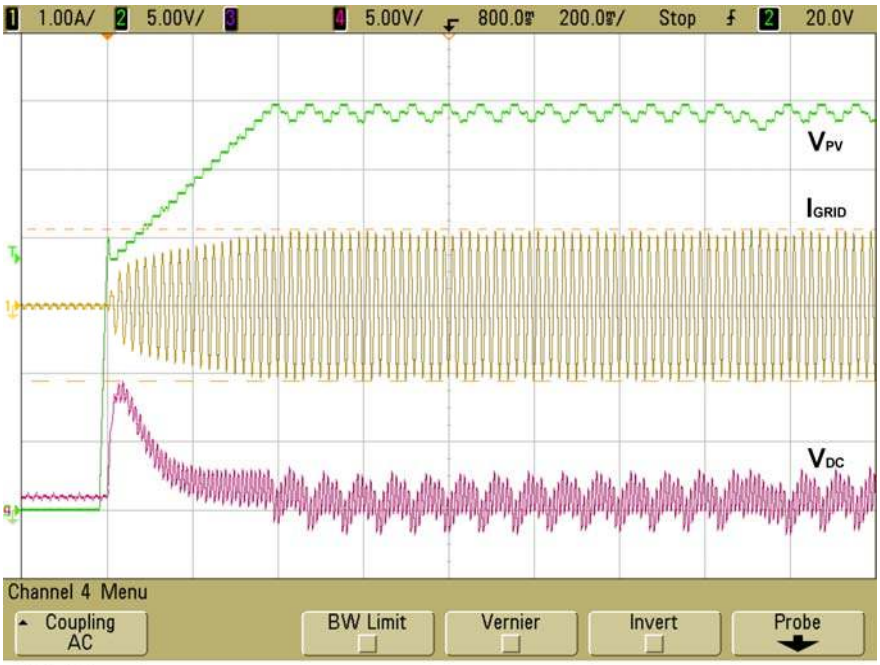


Fig 14a

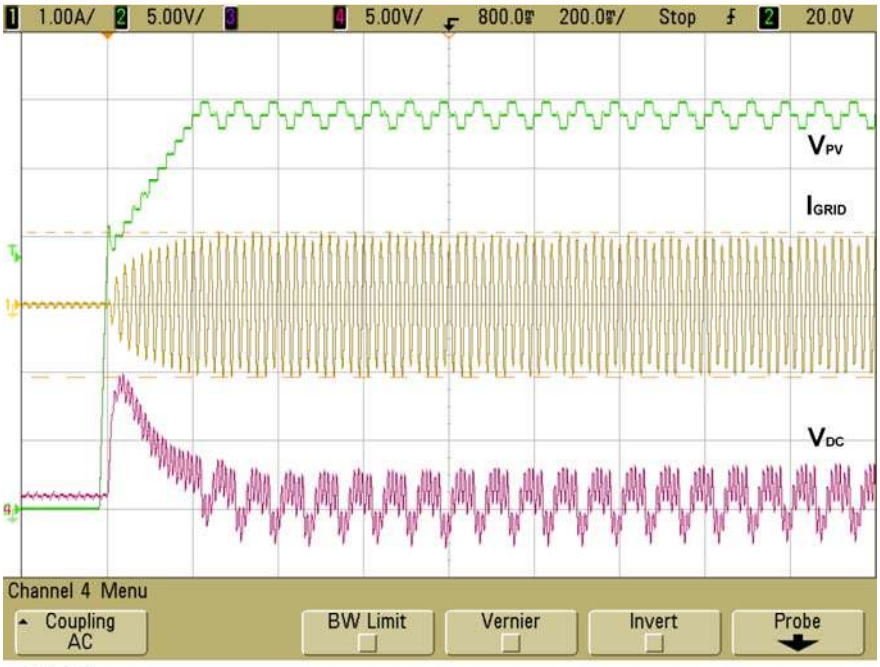


Fig 14b

[Fig. 14. Experimental response of the whole PV inverter to a reference, v_{PVref}, provided by a conventional P&O MPPT algorithm running at f_{MPPT}=50Hz, V_{PV_MPP}≈29 V, P_{PV_MPP}≈182 W and two values of Δv_{PV}. V_{PV} (up), I_{GRID} (middle) and V_{DC} (down). Horizontal Scale=200 ms/div. Vertical Scales: V_{PV}=5 V/div, I_{GRID}=1 A/div, V_{DC}=5 V/div (V_{DC} is AC coupled). (a) Δv_{PV}=600 mV. (b) Δv_{PV}=1V.]

Fig. 15 depicts a detail of the steady-state response of the PV inverter once the MPP of Fig. 14 has been reached: V_{PV_MPP}≈29 V, P_{PV_MPP}≈182 W. It can be observed that the voltage loop is fast enough to track the 50 Hz MPPT algorithm reference with both values of Δv_{PV} (600 mV and 1V).

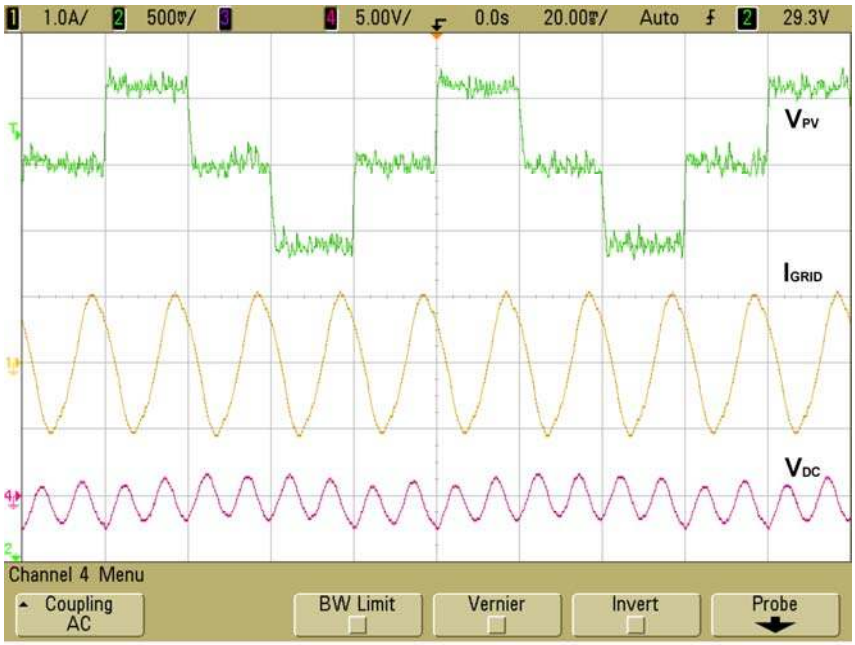


Fig 15a

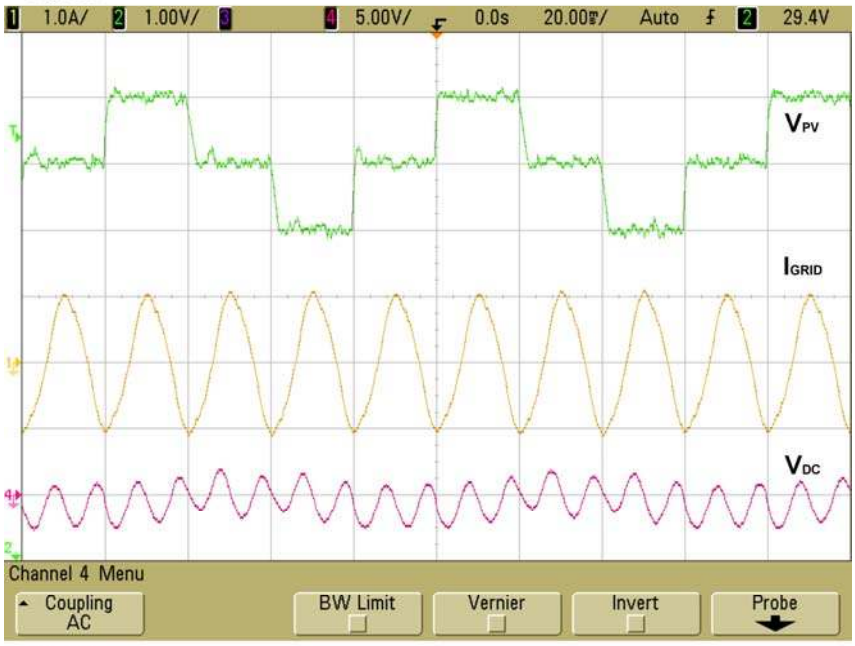
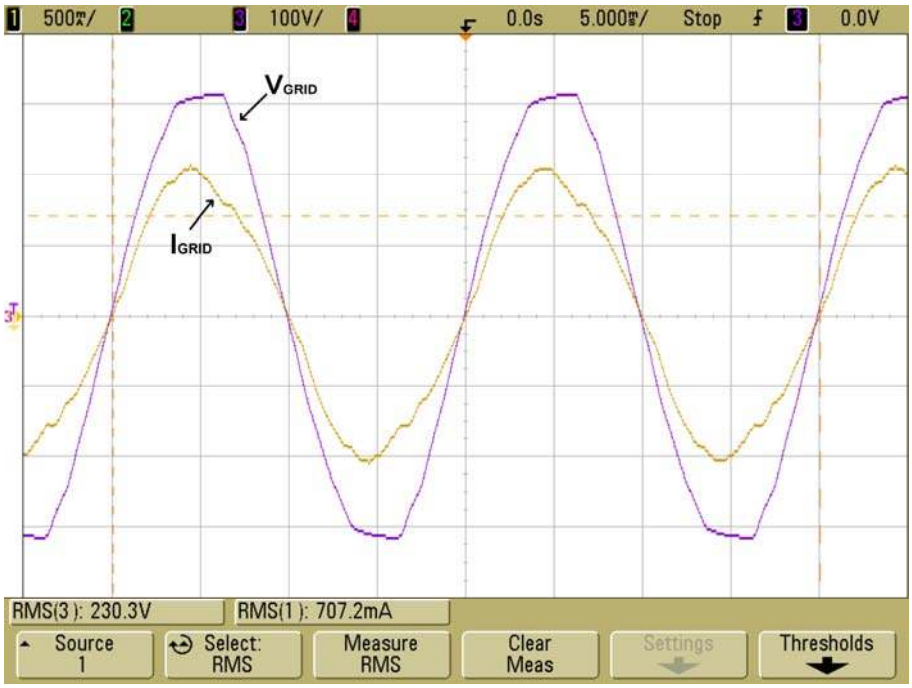


Fig 15b

[Fig. 15. Detail of the steady-state response of the PV inverter around the MPP for f_{MPPT}=50 Hz, V_{PV_MPP}≈29 V, P_{PV_MPP}≈182 W and two values of Δv_{PV}. V_{PV} (up), I_{GRID} (middle) and V_{DC} (down). Horizontal Scale=20 ms/div.
***(a) Δv_{PV}=600 mV*. Vertical Scales: V_{PV}=500 mV/div, I_{GRID}=1 A/div, V_{DC}=5 V/div (V_{DC} is AC coupled).**
***(b) Δv_{PV}=1V*. Vertical Scales: V_{PV}=1 V/div, I_{GRID}=1 A/div, V_{DC}=5 V/div (V_{DC} is AC coupled).**]

Figure 16 shows the grid injected current, I_{GRID}, and the grid voltage, V_{GRID}, at the MPP of Fig. 15: V_{PV_MPP}≈29 V, P_{PV_MPP}≈182 W. With a distortion of the grid voltage of THD_V=3.5 % (a typical distortion value for the grid voltage in our lab), the distortion of the grid current is THD_i=6.3 %. Under those conditions the power factor of the inverter is PF=0.99. The inverter widely complies with the IEC 61000-3-2 norm, corresponding to its power level.



[Fig. 16. Experimental response of the grid current, I_{GRID} (yellow), and the grid voltage, V_{GRID} (purple), at the MPP: V_{PV_MPP}≈*29 V*, P_{PV_MPP}≈*182 W*. Horizontal Scale=*5 ms/div*. Vertical Scales: I_{GRID}=*0.5 A/div*, V_{GRID}=*100 V/div*.]

5. CONCLUSION

Double-stage conversion topologies with HF isolation are common for commercial photovoltaic grid-connected inverters. There are two widely accepted options for the control structure of these power conversion systems. In the simplest option an MPPT algorithm directly provides the duty cycle for the DC-DC converter [4]. The other option is to close a PV panel voltage control loop working from a PV panel reference voltage provided by an MPPT algorithm [5]-[7]. None of the conventional control structures provides a quick overcurrent protection in the case of short circuit or saturation of the magnetic components of the DC-DC converter.

The main contribution of this paper is to add an inner Peak Current Control loop to provide an efficient cycle-by-cycle overcurrent protection to the DC-DC converter. In the proposed control structure the MPPT circuit provides the reference to the PV panel outer voltage loop, whereas the output of the voltage controller is the reference of the current loop. The maximum value of the voltage controller output determines the maximum peak value of the instantaneous sensed current, providing a fast overcurrent protection to both the power switches and the magnetic components of the DC-DC converter. A further advantage of PCC is that the transfer function to be compensated by the voltage regulator becomes basically first order, avoiding the need of a complex integrator+2 poles+2 zeroes regulator, typical from VMC.

In order to illustrate the proposed control structure, it has been applied to a *230 W* Flyback DC-DC converter in a double-stage grid-connected low power inverter for a single PV panel. The Flyback converter works in DCM, and it is controlled by Peak Current mode Control (sensing the current through the power transistor) and voltage control of its input voltage, V_{PV}, i.e. the PV panel voltage. A state-space representation of the small-signal model has been shown, useful for the adjustment of the control loops and for the derivation of the dynamic characteristics. The influence of P_{PV} and V_{PV} on the most important transfer functions has been studied: closed loop response of the current loop, loop gain of the voltage loop

and susceptibility of V_{PV} to the low frequency ripple at the inverter DC-link. The effect of the PCC external ramp on stability is explained.

Furthermore, the relationship between the control design and the choice of the parameters f_{MPPT} and Δv_{PV} of a conventional P&O MPPT algorithm has been highlighted. Finally, the time and frequency response of the whole PV inverter system has been shown to validate the concept. The proposed control structure provides a fast and accurate tracking to a PV panel reference voltage coming from a conventional P&O MPPT algorithm. The voltage reference update frequency is as fast as $f_{MPPT}=50\ Hz$, which is an outstanding value.

Both the PCC control structure and its analysis can be extended to the DC-DC converters in other double-stage PV inverters. This paper may constitute the basis for the design of the PCC loop of inverters using the boost, the isolated full-bridge, the push-pull or other DC-DC stages.

6. ACKNOWLEDMENTS

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TABLE I
MAIN PARAMETERS OF THE PV INVERTER

Flyback DC-DC converter		**PWM grid-connected inverter**	
Input voltage, V_{pv}	*24 V* to *35 V* at the MPP	Input voltage, V_{DC}	*380 V*
Input current, I_{pv}	*8 A* (max.) at the MPP	Rated input power, P_{inv_max}	*230 W*
Rated input power, P_{pv_max}	*230W*	RMS nominal grid voltage, V_{grid}	*230 V*
Switching frequency, f_{sw}	*24 kHz*	Switching frequency, f_{sw_inv}	*10 kHz*
Input capacitance, C_{IN}, and ESR, R_C	*4.08 mF* *2.5 mΩ*	Nominal grid frequency, f_{grid}	*50 Hz*
Transformer turns ratio, $N=N1/N2$	*1/16*	DC-link capacitance, C_{DC}	*470 µF*
Transformer magnetizing inductance (seen from the primary), L_m, and ESL, R_L	*10 µH* *2 mΩ*	Grid filter inductance, L_f	*37 mH*
		Grid filter capacitance, C_f, and damping resistance, R_f	*270 nF* *50 Ω*
Mosfet switch	IRFP4468PbF	IGBT switches	IKP04N60T
Output diode	BY359-1500		

TABLE II
EXPRESSIONS OF THE SMALL-SIGNAL MODEL PARAMETERS

Operation point value		Small-signal model parameter	
Variable name	**Expression**	**Variable name**	**Expression**
I_a	$\frac{P_{pv}}{V_{pv}}$	g_i	$\frac{I_a}{V_{ac}} = \frac{P_{pv}}{{V_{pv}}^2}$
I_p	$\frac{P_{pv}}{\frac{N_1}{N_2} \cdot V_{DC}}$	g_f	$2 \cdot \frac{I_p}{V_{ac}} = \frac{2 \cdot P_{pv}}{\frac{N_1}{N_2} \cdot V_{DC} \cdot V_{pv}}$
V_{ac}	V_{pv}	g_o	$\frac{I_p}{V_{cp}} = \frac{P_{pv}}{\left(\frac{N_1}{N_2} \cdot V_{DC}\right)^2}$
V_{cp}	$\frac{N_1}{N_2} \cdot V_{DC}$	K_i	$2 \cdot \frac{I_a}{D} = \frac{2 \cdot P_{pv}}{\sqrt{L_m \cdot f_{SW}}}$
D	$\frac{\sqrt{2 \cdot L_m \cdot f_{SW} \cdot P_{pv}}}{V_{pv}}$	K_o	$2 \cdot \frac{I_a}{D} = \frac{V_{pv} \cdot \sqrt{\frac{2 \cdot P_{pv}}{L_m \cdot f_{SW}}}}{\frac{N_1}{N_2} \cdot V_{DC}}$

TABLE III
GAINS AND TRANSFER FUNCTIONS OF THE FLYBACK CONTROL

Name	***Value or expression***
Current sensor gain, R_i	$8\ m\Omega$
Slope of PCC external ramp, S_e	$110\ V/ms$
Voltage sensor gain, β	$52 \cdot 10^{-3}$
Digital delay of one sampling period (T_S=25 μs), ***Del(s)***	$e^{-s \cdot T_s} \approx \frac{1 - \frac{s \cdot T_s}{2} + \frac{(s \cdot T_s)^2}{12}}{1 + \frac{s \cdot T_s}{2} + \frac{(s \cdot T_s)^2}{12}}$
Butterworth 2nd order low pass filter, ***FPB(s)***	$\frac{1}{\frac{s^2}{\omega_o^2} + \frac{s}{Q \cdot \omega_o} + 1}$ $Q = 1/\sqrt{2} \quad \omega_o = 2\pi \cdot 4500\ \text{rad/s}$
Voltage regulator, $G_V(s)$	$-\left(34 + \frac{12000}{s}\right)$
Closed loop current loop response, $V_{PV\_VC}(s)$	$\left.\frac{\hat{v}_{pv}(s)}{\hat{v}_c(s)}\right\|_{\vartheta_{dc}=0}$
Open loop susceptibility to DC-link ripple, $A(s)$	$\left.\frac{\hat{v}_{pv}(s)}{\hat{v}_{dc}(s)}\right\|_{\vartheta_c=0}$
Loop gain of the voltage loop, $T_V(s)$	$G_v(s) \cdot V_{PV\_VC}(s) \cdot \beta \cdot FPB^2(s) \cdot Del(s)$
Closed loop response of the voltage loop to its reference, $V_{PV\_VREF}(s)$	$\left.\frac{\hat{v}_{pv}(s)}{\hat{v}_{PVref}(s)}\right\|_{\vartheta_{dc}=0} = \frac{1}{\beta \cdot FPB(s)} \cdot \frac{T_v(s)}{1 + T_v(s)}$
Closed loop susceptibility to DC-link ripple, $A_{CL}(s)$	$\left.\frac{\hat{v}_{pv}(s)}{\hat{v}_{dc}(s)}\right\|_{\vartheta_{PVref}=0} = \frac{A(s)}{1 + T_v(s)}$