Dynamic Noise Analysis with Capacitive and Inductive Coupling

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Abstract— **In this paper we propose a dynamic noise model to verify functional failures due to crosstalk in high-speed circuits. Conventional DC noise analysis produces pessimistic results because it ignores the fact that a gate acts as a low-pass filter. In contrast, the dynamic noise model considers the temporal property of a noise waveform and analyzes its effect on functionality. In this model, both capacitive and inductive coupling are considered as the dominant source of noise in high-speed deep-submicron circuits. It is observed that in the case of the local interconnects (where wire lengths are short), the effect of inductive coupling is small; however, for long interconnects this effect may be considerable. Based on this noise model, we have developed an algorithm to verify high-speed circuits for functional failures due to crosstalk. Design of a 4-bit precharge-evaluate full adder circuit is verified, and many nodes which are susceptible to crosstalk noise are identified. It is observed and further verified by SPICE simulation that dynamic noise analysis is more realistic for verifying functional failures due to crosstalk than DC noise analysis.**

I. INTRODUCTION

Continual scaling of feature sizes has made signal integrity one of the most vulnerable problems in deep submicron (DSM) circuits [1]. Until recently, the tolerance of the circuits to noise has often been addressed by designing logic gates to handle the worst case noise level at any point of the circuit. However, an increasing emphasis on improving the performance of very high speed circuits has led to the use of precharge-evaluate forms of logic in some critical parts of the circuits. This in turn makes VLSI circuits more prone to coupling noise.

Coupling noise, which is also known as crosstalk noise, imposes two serious side effects on digital design. It can affect timing (which can result in delay failures) and/or it can cause functional failures. Identifying portions of the design that are noise sensitive is therefore vital to understanding the noise immunity of a design. A good noise model can help to efficiently verify a design and to identify nodes that are susceptible to delay and functional failures. Unfortunately, the DC (static) noise margins are too conservative a measure of noise immunity because it ignores the fact that logic gates also act as low-pass filters. Noise amplitude can be safely higher than static noise margin depending on the shape of the noise. Adhering to static noise margin could severely restrict the performance of the circuit. Extensive work has been done to analyze noise (DC and dynamic) in VLSI circuits [2-4]. However, these attempted mostly to handle noise from interconnect perspective, both in the VLSI domain as well as the board level. In [5], the dynamic behavior of the noise was studied by considering a circuit as a set of channel-connected components. The effect of noise is analyzed via transistor level simulations. Recently, a dynamic noise model [6], was developed and applied to compare the noise immunities of dynamic logic families by evaluating the maximum capacitance between two nets that can tolerate crosstalk noise. In that model, authors assumed capacitive coupling as the dominant source of noise in deep submicron (DSM) circuits and ignored the inductive coupling effect. Inductive coupling, however, may become a potential contributor to the coupling noise due to continual scaling of feature sizes.

In this paper, we include both inductive and capacitive coupling as the source of noise in DSM circuits. We have developed a tool to verify a design for functional failures using this model. A precharge-evaluate circuit implemented in 0.18 μm technology is verified for functional failures using the above model. We restrict our experiments to a precharge-evaluate form of logic only, because these logic families are mainly used for very high speed operations and are very sensitive to noise.

This paper is orgainzed as follows: In section 2, a brief description of the dynamic noise model is given. Evaluation of noise due to inductive and capacitive coupling is also described in detail in this section. Section 3 discusses the effect of capacitive and inductive coupling noise in high speed deep submicrion circuits. In section 4, we describe an algorithm for verifying a design for functional failures using this model. Verification of a precharge-evaluate logic design for functional failures is also discussed in this section.

II. DYNAMIC NOISE MODEL

There are various sources of noise in VLSI circuits - coupling noise, circuit noise (arises due to subthreshold leakage or charge sharing), and power supply noise. Among these, however, coupling noise is recognized as the dominant source of noise in DSM circuits [7]. In this paper, we restrict our attention to crosstalk as the only source of noise in our model. The effect of other sources of noise, however, can be incorporated through some minor modifications to the model.

A. Dynamic Noise Margin

Crosstalk noise occurs mainly due to capacitive and inductive coupling between adjacent nets. Consider the circuit shown in Fig.1. Both aggressor and victim nets are modeled with lumped resistance (R), inductance (L) and capacitance (C). C_L includes aggressor wire capacitance and the load to the aggressor, and

This research was funded in part by DARPA MARCO Gigascale Silicon Research Center (SA3273JB)

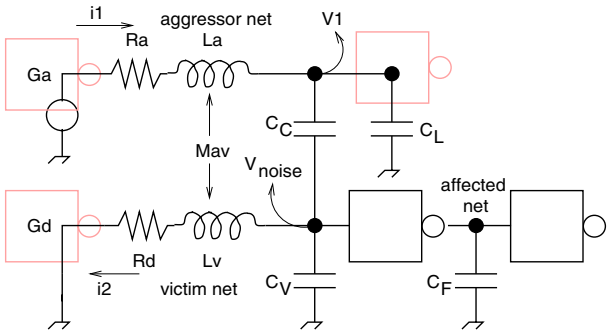

Fig. 1. Dynamic noise model with RLC

C_V represents the same for the victim net. While R_a represents aggressor net resistance, R_d represents both victim net and driver (G_d) resistance. M_{av} is the mutual inductance between the aggressor and the victim nets and v_{in} is the voltage waveform at aggressor net input (the output of aggressor gate G_a). Any transition in aggressor net due to the switching of the gate G_a will cause a noise to be induced at the victim net due to the coupling. In the DC noise model, a failure is considered to occur if the peak of this noise voltage v_{noise} exceeds the DC noise margin of the victim gate G_v. In practice, however, this may not necessarily cause a failure in the circuit. In particular, v_{noise} propagates through the gate G_v to its output and we consider a fault may occur only if the victim output voltage exceeds the DC noise margin of the following gate G_f. The propagated noise at victim gate output is obtained as follows.

The generated gate current, $i_o(t)$, due to the noise input voltage $V_{noise}(t)$ is given by

$$\begin{aligned} i_o(t) &= 0 \quad : v_{noise} < V_{onset} \\ &= g_m \times (v_{noise} - V_{onset}) \quad : v_{noise} \geq V_{onset} \end{aligned} \tag{1}$$

where g_m is the transconductance of the gate G_v and V_{onset} represents its switching threshold voltage. We assume a linear relationship between the input voltage v_{noise} and the gate current $i_o(t)$. This assumption is fairly accurate when devices are velocity saturated so that a linear relation is present between gate drive and output current. The above equation is for a falling output transition of the gate. A similar equation can be written for a rising transition at the output. A charge transfer thus occurs at the output capacitance C_f of gate G_v. This charge Q_t is given by

$$Q_t = g_m \int_{t_0}^{t_1} (v_{noise}(t) - V_{onset})\,dt \tag{2}$$

when the noise voltage, v_{noise} exceeds V_{onset} during the time interval t_0 to t_1 (Fig. 2). This transfer of charge Q_t sets up a voltage change $V_a = \frac{Q_t}{C_f}$ at the input of gate G_f. According to the dynamic noise model a functional failure occurs if V_a exceeds the DC noise margin NM_f of gate G_f. The necessary condition to prevent this failure is thus given by

$$V_a = \frac{Q_t}{C_f} \quad < \quad NM_f$$

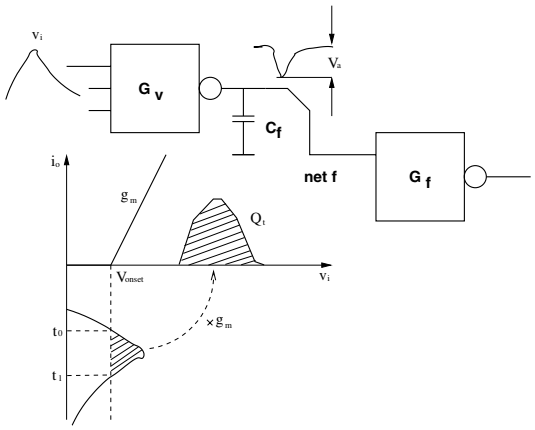

Fig. 2. Propagation of coupled noise through victim gate

$$\text{or,} \quad \int_{t0}^{t1} (v_{noise}(t) - V_{onset})\,dt \quad < \quad \frac{NM_f C_f}{g_m} \tag{3}$$

The term $\frac{NM_f C_f}{g_m}$ has the unit of $volts \cdot sec$ and is defined as the dynamic noise-margin (DNM), a new measure of noise margin analogous to the DC noise-margin (NM). v_{noise}, therefore, plays the most important role in dynamic noise analysis and it has to be calculated accurately. The evaluation process of v_{noise} is described in the following sections.

B. Calculation of v_{noise}

In the previous model [6], it was assumed that crosstalk noise occurs mainly due to capacitive coupling between adjacent nets. Due to the continuous scaling of feature sizes, however, it is important to study the contribution of inductive coupling to the coupling noise in DSM circuits. The coupled noise voltage v_{noise} at the input of the victim gate G_v is obtained as follows. Using KCL and KVL the circuit equations can be written as

$$L_a \frac{di_1}{dt} - M_{av} \frac{di_2}{dt} + R_a i_1 + v_1 = v_{in} \tag{4}$$

$$L_v \frac{di_2}{dt} - M_{av} \frac{di_1}{dt} + R_d i_2 + v_{noise} = 0 \tag{5}$$

$$C_L \frac{dv_1}{dt} + C_c \frac{d(v_1 - v_{noise})}{dt} = i_1 \tag{6}$$

$$C_c \frac{d(v_1 - v_{noise})}{dt} - C_v \frac{dv_{noise}}{dt} = i_2 \tag{7}$$

Substituting i_1 and i_2 we get

$$a_1 \frac{d^2 v_1}{dt^2} + a_2 \frac{d^2 v_{noise}}{dt^2} + a_3 \frac{dv_1}{dt} + a_4 \frac{dv_{noise}}{dt} + v_1 = v_{in} \tag{8}$$

$$b_1 \frac{d^2 v_1}{dt^2} + b_2 \frac{d^2 v_{noise}}{dt^2} + b_3 \frac{dv_1}{dt} + b_4 \frac{dv_{noise}}{dt} - v_{noise} = 0 \tag{9}$$

$$\text{where,} \quad a_1 = L_a(C_c + C_L) - M_{av} C_c$$

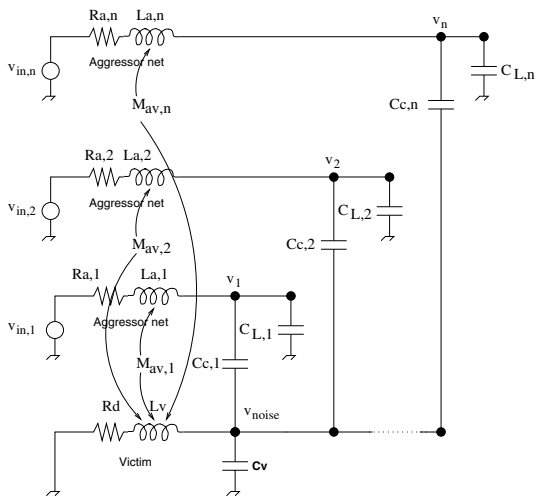

Fig. 3. Multiple aggressors noise model

$$
\begin{aligned}
a_2 &= M_{av}(C_c + C_v) - L_a C_c \\
a_3 &= R_a(C_c + C_L) \\
a_4 &= -R_a C_c \\
b_1 &= L_v C_c - M_{av}(C_c + C_L) \\
b_2 &= M_{av} C_c - L_v(C_c + C_v) \\
b_3 &= R_d C_c \\
b_4 &= -R_d(C_c + C_v)
\end{aligned}
$$

v_{noise} can be evaluated from equations (8) and (9) using Laplace transformation. Assuming all initial conditions to be zero, the transfer function of v_{noise} for impulse response (for v_{in} as impulse) can be obtained as

$$H_{noise}(s) = \frac{b_1 s^2 + b_3 s}{P_4 s^4 + P_3 s^3 + P_2 s^2 + P_1 s + P_0} \tag{10}$$

$$
\begin{aligned}
\text{where} \quad P_4 &= a_2 b_1 - a_1 b_2 \\
P_3 &= a_2 b_3 + a_4 b_1 - a_1 b_4 - a_3 b_2 \\
P_2 &= a_4 b_3 - a_3 b_4 + a_1 - b_2 \\
P_1 &= a_3 - b_4 \\
P_0 &= 1
\end{aligned}
$$

By taking the inverse Laplace transform, v_{noise} therefore can be obtained as

$$v_{noise}(t) = \mathcal{L}^{-1}(H_{noise}(s) V_{in}(s)) \tag{11}$$

where $V_{in}(s)$ is the Laplace transform of $v_{in}(t)$. Once v_{noise} is calculated, propagated noise ($\int_{t0}^{t1}(v_{noise}(t) - V_{onset})dt$) can be obtained following the same method as explained above.

C. Multiple Aggressors Transition

The above equation is derived for a single aggressor transition. In practice however, many aggressor net transitions may occur simultaneously. This effect can be accounted for by suitably modifying the coupled voltage v_{noise} at the victim net.

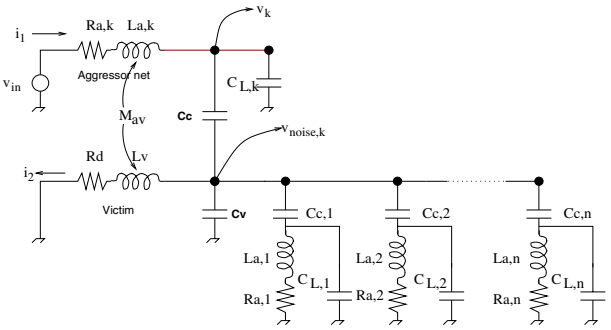

Fig. 4. Equivalent circuit

Consider the circuit shown in Fig. 3, in which multiple aggressor nets are coupled to a victim net by their respective coupling capacitances and mutual inductance. We assume that aggressor nets are not coupled among each other and that they are not affected by the victim transition, as well. It is difficult to calculate v_{noise} in this circuit configuration. We therefore assume supersposition of voltages to solve this problem, i.e., when one aggressor is switching, all other aggressors are quiet. $v_{noise,k}$ thus can be calculated for the kth aggressor transition by solving the equivalent circuit shown in Fig. 4. Even in this case solving $v_{noise,k}$ analytically is impossible. It can be solved directly by using SPICE or by reduced order modeling [8]. We solve $v_{noise,k}$ using SPICE. The total voltage induced at the victim net by n aggressor nets transition is therefore given by

$$v_{noise}(t) = \sum_{i=1}^{n} v_{noise,i}(t) \tag{12}$$

The propagated noise ($\int_{t0}^{t1}(v_{noise}(t) - V_{onset})dt$) due to this modified noise voltage can be compared with the dynamic noise margin of gate G_v to identify whether the net is susceptible to a functional fault.

III. Inductive Effects

Prior to calculating v_{noise} for local and long interconnects, inductance values for typical wires were extracted using FastHenry. Table I shows inductance values for two different types of copper interconnects. The height of the wire was set according to the aspect ratio (height/width) of two. k in the table represents the absolute value of the mutual inductance coefficient and was obtained from two identical wires placed in parallel. From the values in the table, self inductance values for local and long interconnects were chosen as 10pH and 1nH, respectively, for the following experiments.

TABLE I
Inductance extraction for copper interconnects.

type	length	width	spacing	self ind.	k
local	12μm	0.27μm	0.27μm	9.37pH	0.71
long	700μm	0.54μm	0.54μm	1.016nH	0.75

v_{noise} was calculated for typical local interconnects (approximately 12 μm in length) in 0.18 μm technology and is shown

in Fig. 5. We assumed a typical value of mutual inductance ($M_{av} = 0.7(L_a L_v)^{\frac{1}{2}}$) in this experiment. It is observed that the effect of inductive coupling is not significant compared to capacitive coupling. However, the experiment shows a considerable effect in case of long interconnects (Fig 6). In case of long interconnects, we assumed the same mutual inductance coefficient as local interconnects and that only the self inductance increases due to the longer length of the wire. The effect of inductive coupling can be neglected for local interconnects, however, it should be considered for long interconnects. It is also observed that the effect of only inductive coupling without capacitive coupling is insignificant for noise analysis.

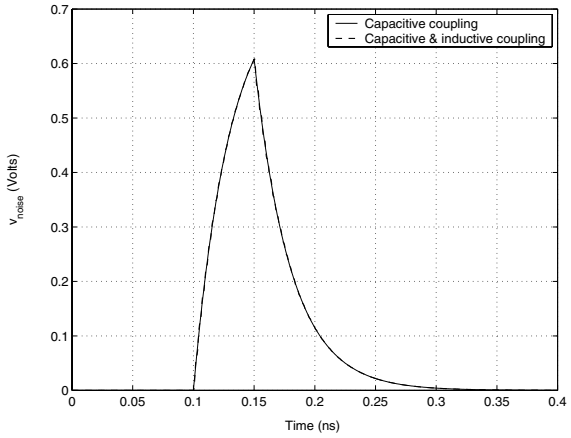

Fig. 5. Coupling noise in local interconnects

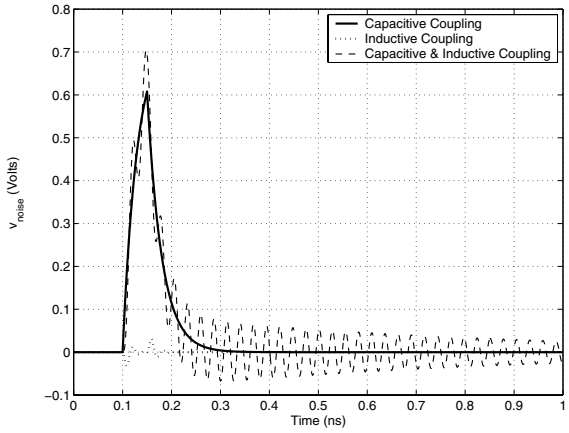

Fig. 6. Coupling noise in long interconnects

A. *Effect of Mutual Inductance*

Mutual inductance can be negative or positive depending on how the current loop is formed. Formation of a current loop depends mainly on the current direction in the wire and the return path [9]. We therefore consider both positive and negative values of mutual inductance in our experiment. Fig. 7 shows the effect of mutual inductance on coupling noise voltage. For all values of M_{av} (from -0.7$(L_a L_v)^{\frac{1}{2}}$ to 0.7$(L_a L_v)^{\frac{1}{2}}$), coupled noise shows a higher peak value than the corresponding noise with only capacitive coupling. For negative M_{av}, however, the effect becomes less significant than the effect of positive mutual inductance. It is also seen that when there is no mutual inductance ($M_{av} = 0$), the v_{noise} waveform is nearly the same as the waveform with negative mutual inductance. Therefore, if the mutual inductance can be made negative through efficient layout techniques, the effect of inductive noise can be minimized.

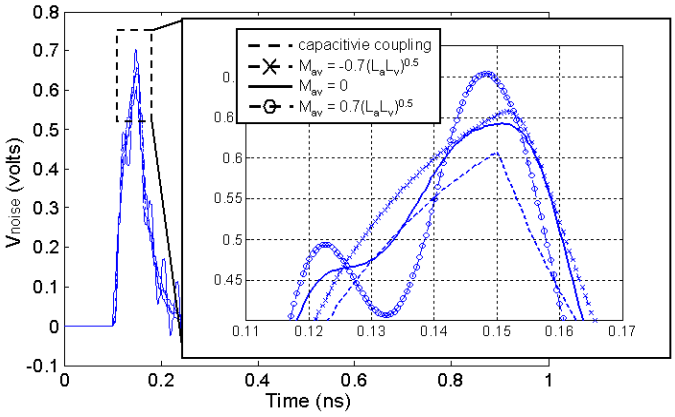

Fig. 7. Effect of mutual inductance

B. *Effect of Self Inductance*

We discussed the effect of self inductance on coupling noise (Fig. 5 and 6). We assumed the same self inductance values ($L_a = L_v$) for aggressor and victim nets in these experiments. In practice, however, the length of these nets are different and their self inductance values are also different. We need a detailed analysis of the effect of self inductance of aggressor and victim nets on coupling noise. Fig. 8 shows the effect of self inductance on coupling noise. It is seen from the figure that the effect of larger self inductance of an aggressor net (L_a) is more severe than that of a victim net. Compare two curves with ($L_v = 10pH, L_a = 1nH$) and ($L_v = 1nH, L_a = 10pH$). The latter has less effect on v_{noise}. Of course, when both self inductances are high the effect is worse, as mentioned earlier.

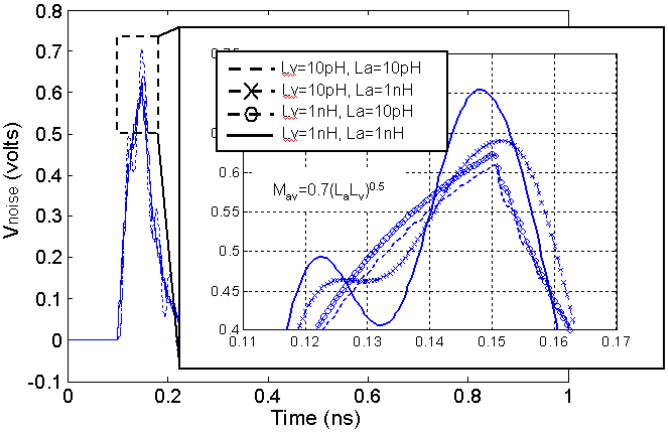

Fig. 8. Effect of self inductance

IV. Design Verification

We restrict our experiments only to precharge-evaluate logic families because they are most sensitive to noise. A dynamic noise model can also be used to verify failuress due to crosstalk in static CMOS design; however, proper assignment of aggressors to a victim net is extremely difficult due to poor predictability in signal transition. Circuits thus can be verified by considering all neighboring nets as aggressors to a victim net. In contrast, monotonic signal transition in precharge-evaluate circuits makes aggressor assignment more accurate.

A. *Functional Failure*

Fig.9 shows the algorithm for verifying a design for functional failures. At the first step after both circuit and technology information are read, a topological sort is performed to levelize the circuit. Since the circuit is a monotonic circuit, there can be only one possible transition at its primary inputs. A static timing analysis is performed in step 2, assuming that all the primary inputs have transition. Transitions are then propagated through the circuit in the levelized order. A delay metrix is obtained from the information provided in the gate library. At the end of this phase, the respective aggressors are identified for all individual nets. With the help of parasitic capacitances extracted from the layout, it is fairly easy to calculate the dynamic noise margein of a gate. This is done in step 3. In step 4, the propagated noise, $\int_{t0}^{t1}(v_{noise}(t) - V_{onset})dt$ (volt.sec.) through the gate is calculated and compared with its dynamic noise margin. The node is thus checked for a functional failure. Step 3 and 4 are then repeated for all the nets in the circuit.

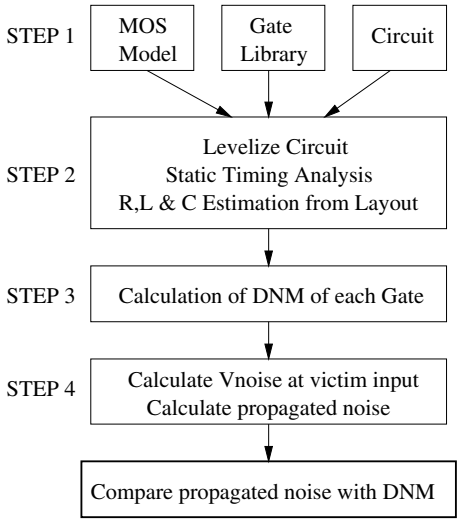

Fig. 9. Flow diagram for the verification of functional failure

A precharge-evaluate 4-bit full adder circuit implemented using skewed CMOS logic [10] is verified for functional failures using the above algorithm. Skewed logic is a fully complementary static logic circuit. The sizes of PMOS and NMOS transistors are adjusted to make one of the transitions faster than the other. Changing the driving capabilities of PMOS and NMOS to make transition faster in one direction is known as skewing. The

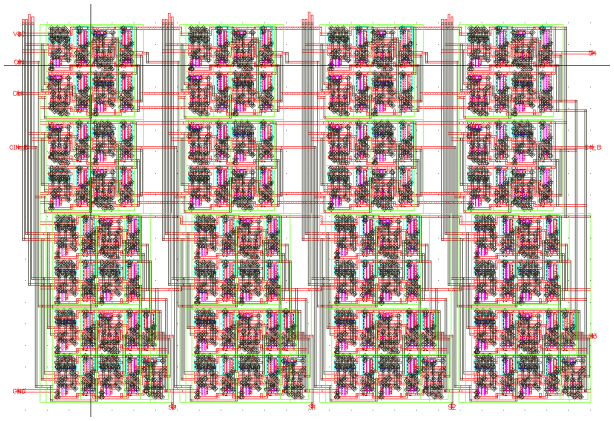

Fig. 10. Layout of skewed CMOS 4-bit full adder circuit

layout of the circuit is drawn using a custom design approach with 0.18 μm technology as shown in Fig. 10. While it is easy to extract parasitic capacitances from the layout using an automated tool, extracting inductance (self and mutual) is not that straightforward. It has been discussed in the previous section that the effect of inductive coupling is not significant for local interconnects. We therefore calculate inductance values manually for only long wires and include them in the experiment. The layout showed that the longest wires are approximately 60 $\sim$ 70 μm long and they correspond to the self inductance values of about 70 pH, which is comparatively smaller than the value shown in table I.

Fig.11 shows the comparison of propagated noise ($\int_{t0}^{t1}(v_{noise}(t) - V_{onset})dt$) with DNM for all nets in the circuit. A ramp type aggressor transition is considered for the experiment. Nodes that are susceptible to functional failures based on the DC noise margin are also shown in Fig. 12. It is observed that the number of nodes susceptible to failures based on the DC noise margin is 12; however, in dynamic noise analysis only three nodes are identified as possible failures. Table II shows the DC noise and dynamic noise violation for four susceptible nodes from the DC noise analysis. Even all four nets have noise whose peak values are greater than corresponding DC noise margins, only one net shows violation in terms of dynamic noise. This is because in dynamic noise analysis we consider that a failure may occur when the victim output voltage due to noise coupled at its input exceeds the DC noise margin of the following gate. In contrast, in the DC noise margin approach we consider a failure to have occurred when the coupled noise peak exceeds the DC noise margin of the victim gate itself. In dynamic noise analysis, both noise voltage and time are considered to verify the noise immunity of the circuit. It is therefore more realistic than DC noise analysis.

We verify this result through SPICE simulation to validate the model. We set the primary input transition in such a way that a particular suspected net is quiet and all its aggressors switch. For verification, we select two nets as victims; one from the DC noise margin analysis and the other from dynamic noise analysis. We select nodes in such a way that the first one is susceptible to a failure based on the DC noise analysis but not by

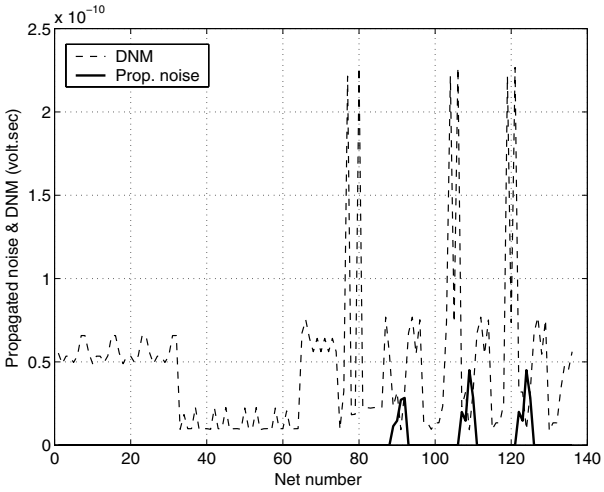

Fig. 11. Fault verification by dynamic noise analysis

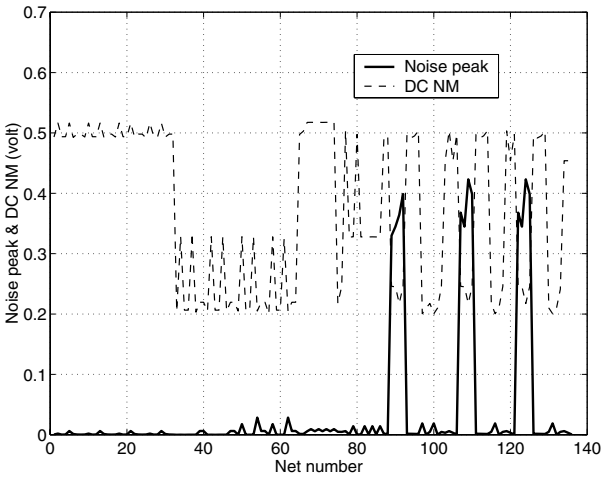

Fig. 12. Fault verification based on DC noise margin

dynamic noise analysis. The second victim is chosen from one of the three susceptible nets from dynamic noise analysis in Fig. 11. The SPICE result shows that noise coupled at the first victim net does not have any impact on circuit functionality (Fig. 13(a)). There is no considerable change at the victim output though the noise peak exceeds the DC noise margin of the gate. In the second case, however, there is a significant change at the victim output (Fig. 13(b)). The victim gate output thus may be wrongly evaluated causing a failure in the circuit.

V. Conclusion

We have described a noise model to verify functional failures due to crosstalk in high-speed circuits considering both capacitive and inductive coupling. It is observed that the effect of inductive coupling for local interconnects is insignificant; however, it can be significantly higher for long interconnects. It is also noticed that the self inductance of the aggressor net has more effect on coupling noise than the victim net inductance. An algorithm is described to verify a design for functional failures due to crosstalk using our model. The design of a precharge-evaluate 4-bit adder circuit is verified and a number of nodes that are susceptible to functional failures are identified.

TABLE II

DC noise vs. dynamic noise violation

net number	DC NM (mV)	peak noise (mV)	DNM $(volt \cdot ps)$	prop. noise $(volt \cdot ps)$
89	246	351	26.83	16.03
90	245	361	36.84	18.73
91	218	377	12.01	**31.55**
92	246	401	37.40	29.95

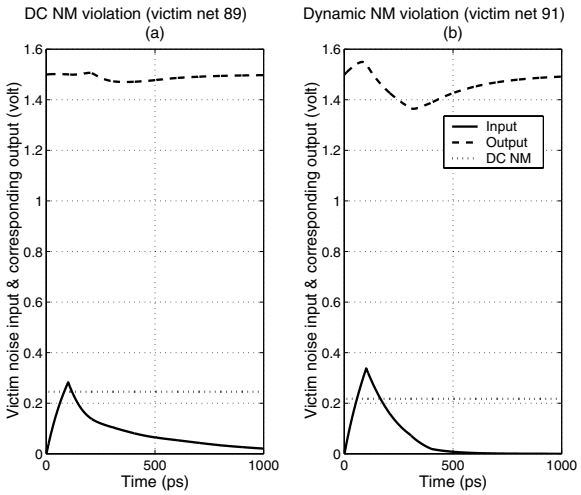

Fig. 13. Spice verification for two suspected nets

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