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Dynamic Performance and Control of a Static Var Generator Using Cascade Multilevel Inverters

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***Abstract*–A cascade multilevel inverter is proposed for static var compensation/generation applications. The new cascade M-level inverter consists of (M–1)/2 single-phase full bridges in which each bridge has its own separate dc source. This inverter can generate almost sinusoidal waveform voltage with only one time switching per cycle. It can eliminate the need for transformers in multipulse inverters. A prototype static var generator (SVG) system using 11-level cascade inverter (21-level line-to-line voltage waveform) has been built. The output voltage waveform is equivalent to that of a 60-pulse inverter. This paper focuses on dynamic performance of the cascade inverter based SVG system. Control schemes are proposed to achieve a fast response which is impossible for a conventional static var compensator (SVC). Analytical, simulated and experimental results show the superiority of the proposed SVG system.**

I. INTRODUCTION

Reactive power (var) compensation or control is an essential part in a power system to minimize power transmission losses, to maximize power transmission capability, to stabilize the power system, and to maintain the supply voltage. The so-called advanced static var compensators (ASVCs) using multipulse voltage-source inverters have been widely accepted as the state-of-the-art reactive power controllers of power systems to replace the conventional var compensators such as thyristor switched capacitors and thyristor controlled reactors [1–6].

Typically, a 48-pulse ASVC consists of eight three-phase voltage-source inverters connected together through eight zig-zag-arrangement transformers, in order to reduce harmonic distortion using the harmonic neutralization (cancellation) technique and to reach high voltage. These transformers, (1) are the most expensive equipment in the system, (2) produce about 50% of the total losses of the system, (3) occupy a large area of real estate, about 40% of the total system, (4) cause difficulties in control due to DC magnetizing and surge over-voltage problems resulting from saturation of the transformers in transient state, and (5) are prone to fail. In addition, the dynamic response of these ASVCs is very slow because their inverters are usually operated in the 6-pulse mode with phase shifting, and the output voltage is solely in proportion to the dc voltage that cannot have an instantaneous change. Although the pulse-width-modulation (PWM) can be applied to these ASVCs, the losses introduced by switching are not acceptable in high power applications. It has been shown that these ASVCs cannot respond faster than a quarter of line cycle, i.e., about 4~5ms, from the rated lagging reactive power to rated leading reactive power [5, 6]. For rapidly changing loads and line disturbances, such as arc furnaces, a faster response within a couple of ms is required. To achieve this order of response, a high frequency PWM inverter is required; however, one cannot afford to do so due to switching losses [10].

A cascade multilevel inverter has been proposed [9]. The new cascade inverter not only can eliminate the bulky transformers of the ASVCs, but also can respond within 1ms, much faster than the ASVCs do. A prototype SVG system using an 11-level cascade inverter has been built. The output line-to-line voltage waveform presents 21 levels, almost sinusoidal with only one time switching per line cycle and without high frequency PWM operation. This paper focuses on dynamic performance of the cascade inverter based SVG system. System models and control schemes are presented to achieve a fast response within 1ms which is impossible for today's ASVCs. A fully digital control is implemented with a digital signal processor (DSP) board. Analytical, simulated and experimental results show the superiority of the proposed SVG system.

II. SYSTEM CONFIGURATION OF SVG

A. Cascade Inverter Structure and Control

Fig. 1 shows the Y-configured 11-level cascade inverter used in the experimental SVG system. As shown in Fig. 1, the cascade inverter uses a separate dc source for each H-bridge inverter unit of each phase. The required dc capacitance is slightly higher than the ASVC [9]. These dc capacitors, however, are far smaller and much more efficient than the bulky transformers of the ASVC according to the experimental system and analysis.

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Fig. 2 shows output waveforms of phase *a*. Each H-bridge inverter unit generates a quasi-square wave, v_{Cai} (i=1, 2, ... 5), as shown in the figure. As a result, a staircase voltage waveform, v_{Ca_n}, is obtained. The switching phase angles, θ_i (i=1, 2, ..., 5), are off-line calculated to minimize harmonics for each modulation index (MI). The MI is defined as V_C^*/V_{Cmax}, where V_C^* is the magnitude reference of the inverter output voltage, $V_C^* = \sqrt{v_{Ca}^{*\,2} + v_{Cb}^{*\,2} + v_{Cc}^{*\,2}}$, and V_{Cmax} is the maximum obtainable magnitude of voltage when all the switching phase angles equal zero, $V_{Cmax} = \sqrt{\frac{3}{2}}\frac{4}{\pi}(5V_{dc})$. Table I shows the off-line calculated phase angles, which are stored in a look-up table to generate gate signals for each inverter unit.

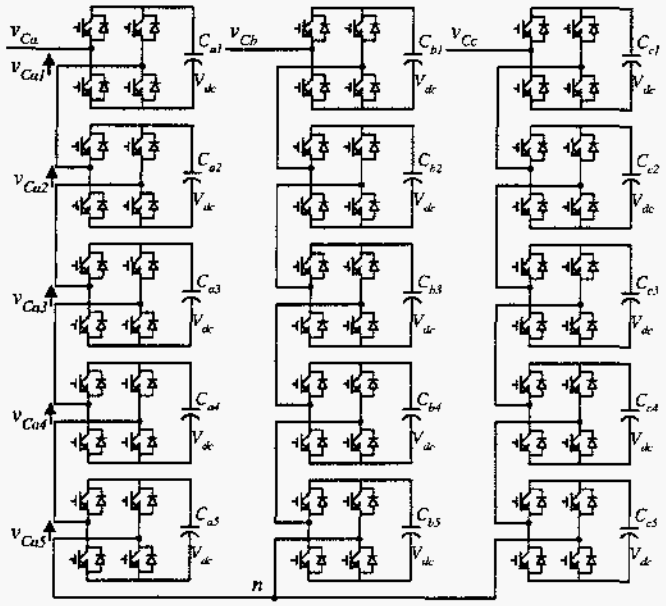

Fig. 1. The 11-level cascade inverter used in the experimental SVG system.

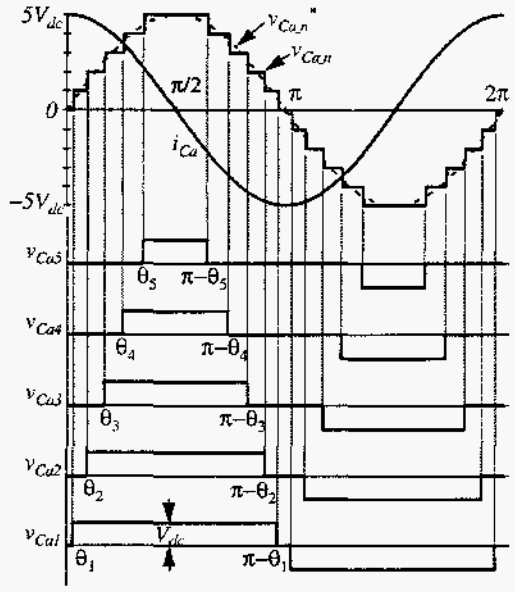

Fig. 2. Waveforms of phase *a* in the 11-level cascade inverter of Fig.1.

TABLE I
SWITCHING ANGLE TABLE OF 11-LEVEL CASCADE INVERTER

Modulation Index $MI=V_C^*/(\sqrt{\frac{3}{2}}\frac{4}{\pi}\cdot 5V_{dc})$	Switching Timing Angles [rad.]				
MI	θ_1	θ_2	θ_3	θ_4	θ_5
0.500	0.6236	0.8179	1.0070	1.2117	1.4518
0.510	0.6218	0.8048	0.9931	1.2010	1.4340
...	...	...	...	...	...
1.000	0.0000	0.0000	0.0000	0.0000	0.0000

B. System Configuration of SVG

Fig. 3 shows the experimental system configuration of the 11-level cascade inverter based SVG, where L_C is the interface inductor coupling the inverter to the line and L_S is the line impedance. I_{Cq}^* (or q_C^*) is the reactive current (or reactive power) reference, and V_{dc}^* is the dc voltage reference. The SVG system control block provides amplitude reference, V_C^*, and phase shift reference, α_C^*, of the output voltage. Control of this SVG system is different from the conventional control scheme of the ASVCs that have only one controllable variable, α_C^*. θ is the phase angle of the source voltage. Switching gate signals are then generated from the amplitude reference, V_C^*, and phase reference, θ_C^*, through the look-up table.

The SVG in steady state will generate a leading reactive current when the amplitude of the output voltage, V_C, is larger than the source voltage's amplitude, V_S, and it will draw a lagging current from the source when V_C is smaller than V_S. However, both the amplitude and phase shifting angle, V_C and α_C, need to be controlled at transient states.

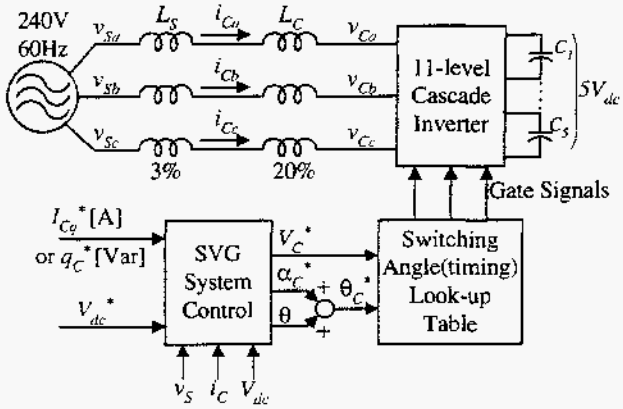

Fig. 3. Experimental system configuration of the SVG.

III. DYNAMIC ANALYSIS AND CONTROL SCHEMES

A. Dynamic Models of SVG System

Fig. 4 shows the equivalent circuit of the SVG system, where v_S is the source voltage, v_C is the generated voltage of the SVG, i_C is the current drawn by the SVG, and L and R are the total ac inductance and resistance. The source voltage, v_S, SVG voltage, v_C, and SVG current, i_C, are instantaneous quantities and represented in the $\alpha\beta$-phase frame through the *abc*-to-$\alpha\beta$ transformation [*C*] as follows:

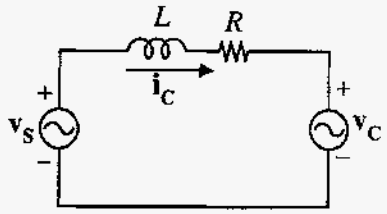

Fig. 4. Equivalent circuit of the SVG system.

$$\mathbf{v_S} = \begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = [C] \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix}, \quad \mathbf{v_C} = \begin{bmatrix} v_{C\alpha} \\ v_{C\beta} \end{bmatrix} = [C] \begin{bmatrix} v_{Ca} \\ v_{Cb} \\ v_{Cc} \end{bmatrix}, \text{ and}$$

$$\mathbf{i_C} = \begin{bmatrix} i_{C\alpha} \\ i_{C\beta} \end{bmatrix} = [C] \begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix}, \text{ where, } [C] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}.$$

From the equivalent circuit of Fig. 4, we have

$$L\frac{d\mathbf{i_C}}{dt} + R\mathbf{i_C} = \mathbf{v_S} - \mathbf{v_C}. \tag{1}$$

Assuming that the source voltage is sinusoidal, we can represent $\mathbf{v_S}$ as

$$\mathbf{v_S} = V_S \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \tag{2}$$

where, V_S is the rms value of the line-to-line voltage, and θ is the phase angle. Furthermore, we can get the dq-coordinate expressions of (1) and (2) by using the synchronous reference frame transformation $[T]$, i.e.,

$$\mathbf{V_S} = \begin{bmatrix} V_{Sd} \\ V_{Sq} \end{bmatrix} = [T]\mathbf{v_S}, \quad \mathbf{V_C} = \begin{bmatrix} V_{Cd} \\ V_{Cq} \end{bmatrix} = [T]\mathbf{v_C}, \quad \mathbf{I_C} = \begin{bmatrix} I_{Cd} \\ I_{Cq} \end{bmatrix} = [T]\mathbf{i_C},$$

and $[T] = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}$, thus resulting in

$$L\frac{d\mathbf{I_C}}{dt} + L\boldsymbol{\omega} \times \mathbf{I_C} + R\mathbf{I_C} = \mathbf{V_S} - \mathbf{V_C}, \tag{3}$$

$$\text{or} \quad L\frac{d}{dt}\begin{bmatrix} I_{Cd} \\ I_{Cq} \end{bmatrix} + \omega L\begin{bmatrix} -I_{Cq} \\ I_{Cd} \end{bmatrix} + R\begin{bmatrix} I_{Cd} \\ I_{Cq} \end{bmatrix} = \begin{bmatrix} V_{Sd} - V_{Cd} \\ V_{Sq} - V_{Cq} \end{bmatrix}, \tag{4}$$

$$\text{and} \quad \mathbf{V_S} = \begin{bmatrix} V_{Sd} \\ V_{Sq} \end{bmatrix} = \begin{bmatrix} V_S \\ 0 \end{bmatrix}. \tag{5}$$

Fig. 5 shows the $dq\omega$ coordinates where $\omega = d\theta/dt$, both θ and ω are vectors. "×" in (3) denotes the vector or cross product. Since $V_{Sd}=V_S$ and $V_{Sq}=0$, the instantaneous active power, p_C, flowing into the SVG, and instantaneous reactive power, q_C, drawn by the SVG can be obtained as:

$$p_C = V_S I_{Cd}, \quad \text{and} \quad q_C = V_S I_{Cq}. \tag{6}$$

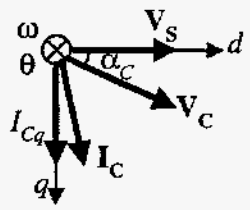

Fig. 5. The $dq\omega$ coordinates.

Therefore, I_{Cd} and I_{Cq} are the active current component and reactive current component of the SVG, respectively. This feature enables a decoupled control of the two current components and thus decoupling the control of the two power components, p_C and q_C. Both I_{Cd} and I_{Cq} can be positive and negative. Active power flows into the inverter for positive I_{Cd} and out from the inverter for negative I_{Cd}. The SVG generates leading reactive power when I_{Cq} is positive and lagging reactive power when I_{Cq} is negative.

Fig. 6 shows the block diagram of the SVG derived from (3) or (4). Here, we have derived two models to describe the SVG main system. One is represented by (1) and Fig. 4 in which the stationary $\alpha\beta$ frame is used. The other is described in the synchronous dq frame based on (4) and Fig. 6. Fig. 6 shows that the active current component and reactive current component, I_{Cd} and I_{Cq}, are coupled with each other through the ac inductance ωL, although the instantaneous voltages and currents of $\alpha\beta$ phases represented in (2) and Fig. 4 are independent of each other. For most cases it is required that we can directly and independently control the instantaneous active current component and reactive current component, I_{Cd} and I_{Cq}.

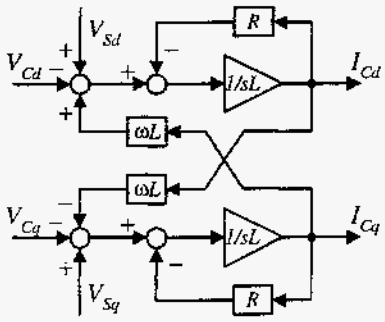

Fig. 6. Block diagram of the SVG main system.

B. Decoupling Feed-Forward Control

From (4) or Fig. 6 it is straightforward that in order for the SVG system to generate the desired active and reactive current components, I_{Cd}^* and I_{Cq}^*, the references of the SVG voltages V_{Cd} and V_{Cq}, V_{Cd}^* and V_{Cq}^*, should be given as:

$$\begin{bmatrix} V_{Cd}^* \\ V_{Cq}^* \end{bmatrix} = \begin{bmatrix} V_{Sd} + \omega L I_{Cq}^* - \left(L\frac{d}{dt} I_{Cd}^* + R I_{Cd}^* \right) \\ V_{Sq} - \omega L I_{Cd}^* - \left(L\frac{d}{dt} I_{Cq}^* + R I_{Cq}^* \right) \end{bmatrix}, \text{ and} \tag{7}$$

$$\begin{cases} V_C^* = \sqrt{V_{Cd}^{*2} + V_{Cq}^{*2}} \\ \alpha_C^* = \tan^{-1}\left(\dfrac{V_{Cq}^*}{V_{Cd}^*}\right) \end{cases} \quad (8)$$

Based on (7) and (8), we have a decoupling feed-forward control as shown in Fig. 7. In this figure, the active current reference, I_{Cd}^*, is generated from a PI controller that regulates the dc voltage of each inverter unit. The detailed control principle has been presented in [9]. The reactive current reference, I_{Cq}^*, is given according to different compensation aims. For instance, for an SVG to compensate the reactive power of a load, it will be the load reactive current. The dq components of source voltage, $\mathbf{V_S}=[V_{Sd}\ V_{Sq}]^t=[V_S\ 0]^t$, are obtained from the directly sensed source voltage; v_{Sa}, v_{Sb} and v_{Sc}, through the abc-to-$\alpha\beta$ transformation; $[C]$, and the synchronous reference frame transformation $[T]$ as mentioned before. The phase angle of the source voltage, θ, can be obtained from a vector phase-locked loop (PLL) circuit as shown in Fig. 8. In the experimental system, a digital PLL circuit is implemented.

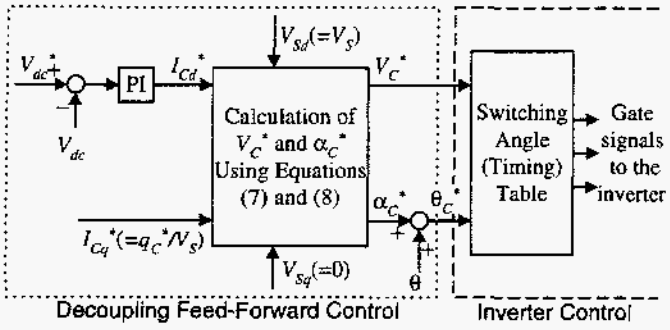

Fig. 7. Block diagram of decoupling feed-forward control of the SVG system.

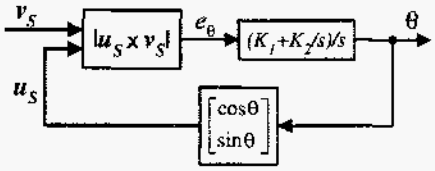

Fig. 8. Vector PLL circuit.

Fig. 9 shows the calculated waveforms for a 1ms ramp change reference from zero to the rated leading reactive power according to (7) and (8). Table II shows the detailed system parameters. The calculated results shown in Fig. 9 help system design. Given a required or desirable response, in this case 1ms from zero to the rated leading reactive power, one can calculate V_C^* which in turn helps determination of the dc voltage since the maximum modulation index is one. Fig. 9 also shows that a large lagging phase shift angle, α_C^*, will result during the building current transient, although it becomes almost zero in the steady state since the ac resistance is normally very small.

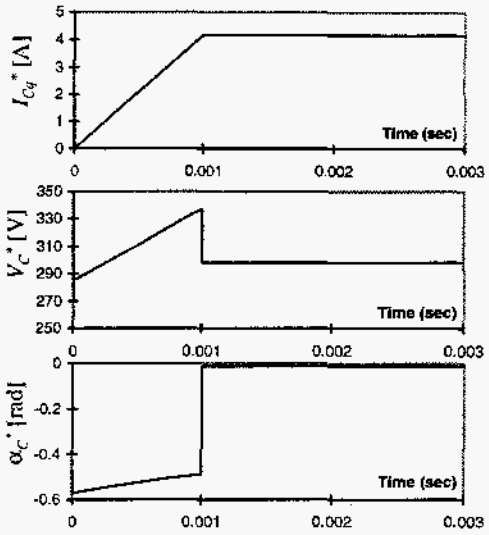

Fig. 9. Waveforms of decoupling feed-forward control for a ramp change reference of reactive current (or reactive power).

TABLE II
SYSTEM PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Source voltage rating V_S	240 V (rms)
Var rating Q_C/current rating I	± 1 kvar/2.4 A (rms)
DC voltage V_{dc}/regulation factor ε	43.5 V/ ± 10%
Interface inductance L_C	20% (32 mH)
Source impedance L_S	3% (0.03 pu)
Total ac resistance R	1.6% (1.0Ω)

C. Decoupling Feedback Control

From (7) one can see that we need to know the source voltage and exact parameters of the total resistance and inductance on the ac side of the SVG to achieve the feed-forward decoupling control. It is often impossible to precisely know the source impedance and source voltage. Errors in these parameters will result in deterioration of dynamic response and steady-state errors of control. A feedback decoupling control is hence proposed as shown in Fig. 10(a) to resolve this problem. A PI controller is used for both active and reactive current control loops. Because of this decoupling control, the equivalent control diagrams for I_{Cd} and I_{Cq} can be derived as Fig. 10(b). The controlled plant is reduced to a first-order transfer function. Therefore, the PI gains can be arbitrarily designed to meet the required response.

Fig. 11 shows simulated waveforms, where the active current reference, I_{Cd}^*, stays zero, while the reactive current reference, I_{Cq}^*, is given a step change. It is seen that the actual reactive current, I_{Cq}, rapidly tracks the step changing reference while the actual active current, I_{Cd}, maintains zero. Complete decoupled control is achieved. The figure also shows a large voltage reference, V_C^*, during the transient state. Because the output voltage is bounded at $V_{Cmax} = \sqrt{\frac{3}{2}}\frac{4}{\pi}(5V_{dc})$, the response speed of this system is only constrained by a practical dc voltage, although in principle its response has no limit.

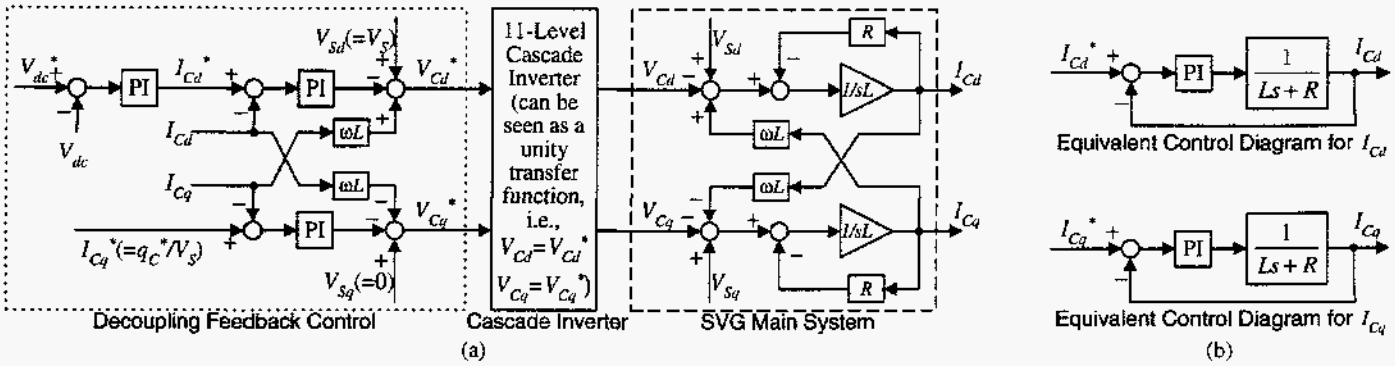

Fig. 10. (a) Decoupling feedback control diagram of the SVG system, where a PI controller is used in the active current and reactive current feedback loops with PI gains as G_P=70 and G_I=2000, (b) equivalent control diagrams for I_{Cd} and I_{Cq}.

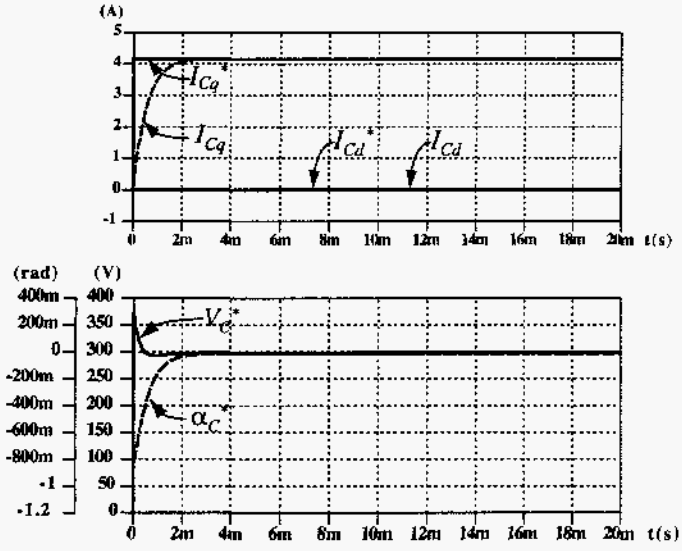

Fig. 11. Simulated waveforms showing decoupling feedback control.

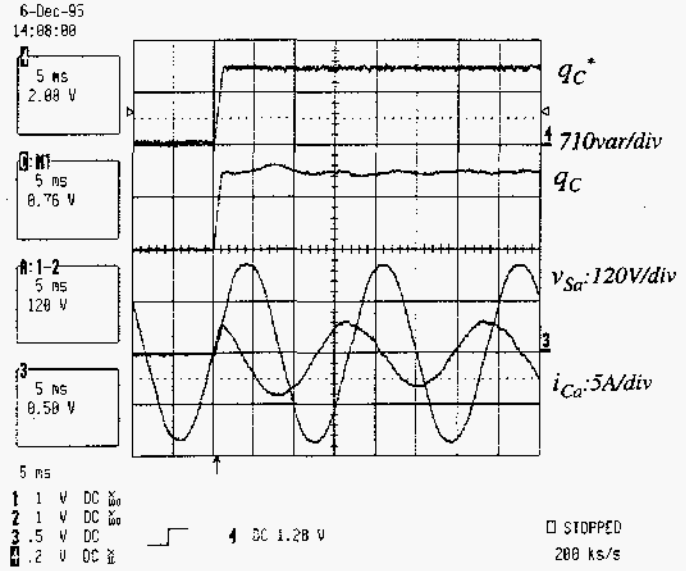

Fig. 12. Experimental waveforms of decoupling feed-forward control with a ramp change reference of the reactive current (or reactive power).

IV. Experimental Results

Based on the previously mentioned prototype system, an experiment has been carried out using the proposed decoupling feed-forward control and decoupling feedback control. The control circuit is fully digitized and based on a TMS320C31 DSP board. The sampling rate is (60×1024)Hz, and the switching pattern for each MI of Table I is stored in a look-up table with 1024 point data per fundamental cycle.

Figs. 12, 13, and 14 show the experimental results of the ramp change reference of the reactive power from zero to the rated leading reactive power within 1ms. The experimental results are consistent with the calculated waveforms of Fig. 9, showing excellent dynamic response.

Figs. 15, 16, and 17 show experimental results of the dynamic response at a step change reference of reactive power. The results show excellent dynamic response with a 0.6 ms time constant to the step change.

The control schemes presented are applicable to PWM inverter based SVG systems. Their dynamic response is also expected to be fast. However, such a fast response cannot be obtained for today's ASVCs.

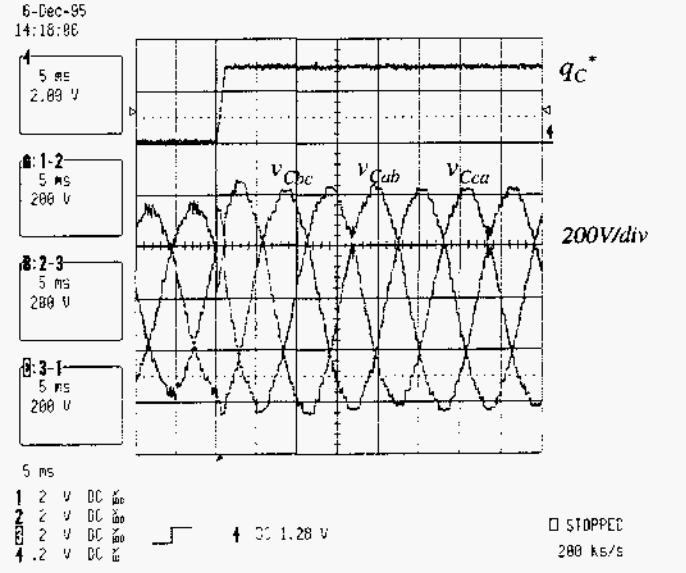

Fig. 13. Experimental inverter voltage waveforms of decoupling feed-forward control with a ramp change reference.

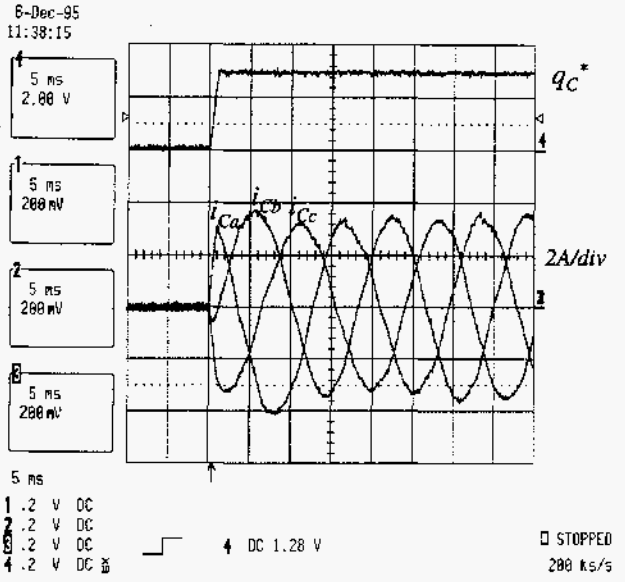

Fig. 14. Experimental current waveforms of decoupling feed-forward control with a ramp change reference.

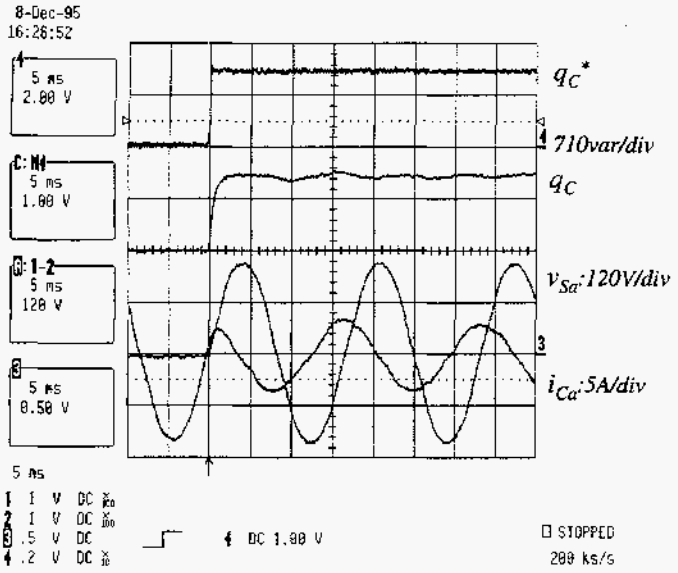

Fig. 15. Experimental waveforms of decoupling feedback control with a step change reference of the reactive current (or reactive power).

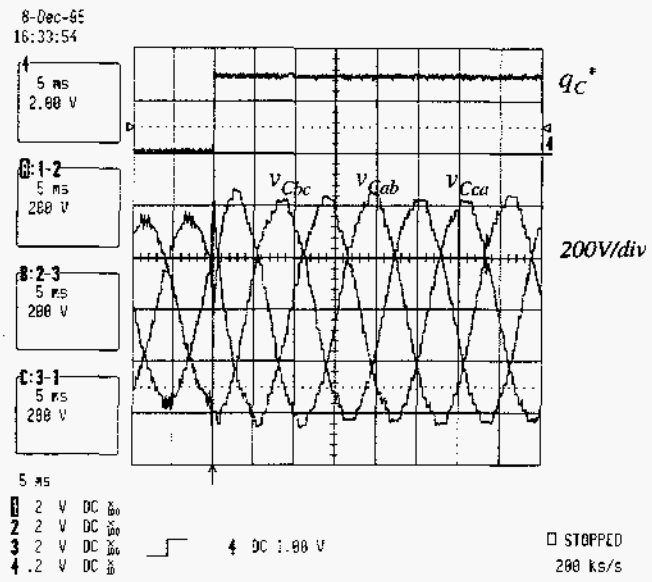

Fig. 16. Experimental inverter voltage waveforms of decoupling feedback control with a step change reference of the reactive current.

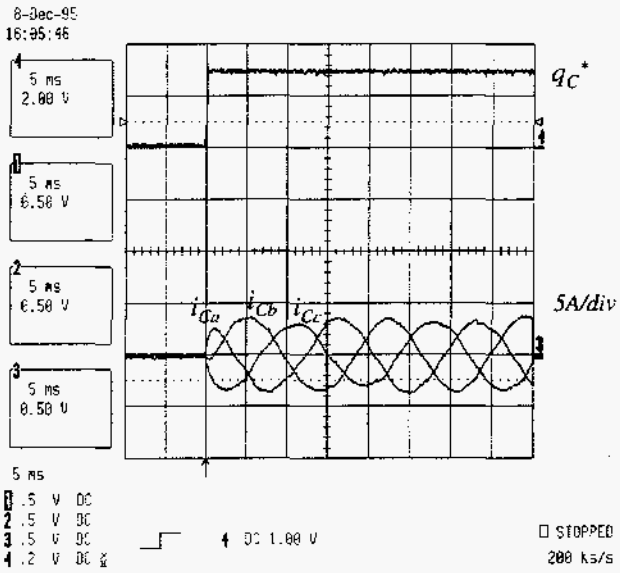

Fig. 17. Experimental current waveforms of decoupling feedback control with a step change reference of the reactive current (or reactive power).

V. Conclusions

A newly developed multilevel inverter has been presented for static var compensation/generation applications. With the presented control schemes, the dynamic performance of the cascade inverter based SVG system has been satisfactory. Simulation and experiment have demonstrated that the new inverter based SVG system can achieve much faster dynamic response than conventional SVCs and today's ASVCs using transformer-coupled inverters. With the minimum switching frequency, this new inverter can achieve performance equal to that of a high-frequency PWM inverter.

The new cascade multilevel inverter, (1) eliminates the bulky transformers of a multipulse inverter, (2) can generate almost sinusoidal waveform voltage and current with only a single switching per fundamental cycle, and (3) has fast dynamic response. In addition, because of its modular and simple structure the cascade inverter can be stacked up to a practically unlimited number of levels. These features make it the best candidate for medium to high voltage power system applications. This new inverter is also suited for other utility applications, such as active power filters, series compensation, etc.

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