Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site SoC Power Integrity Verification

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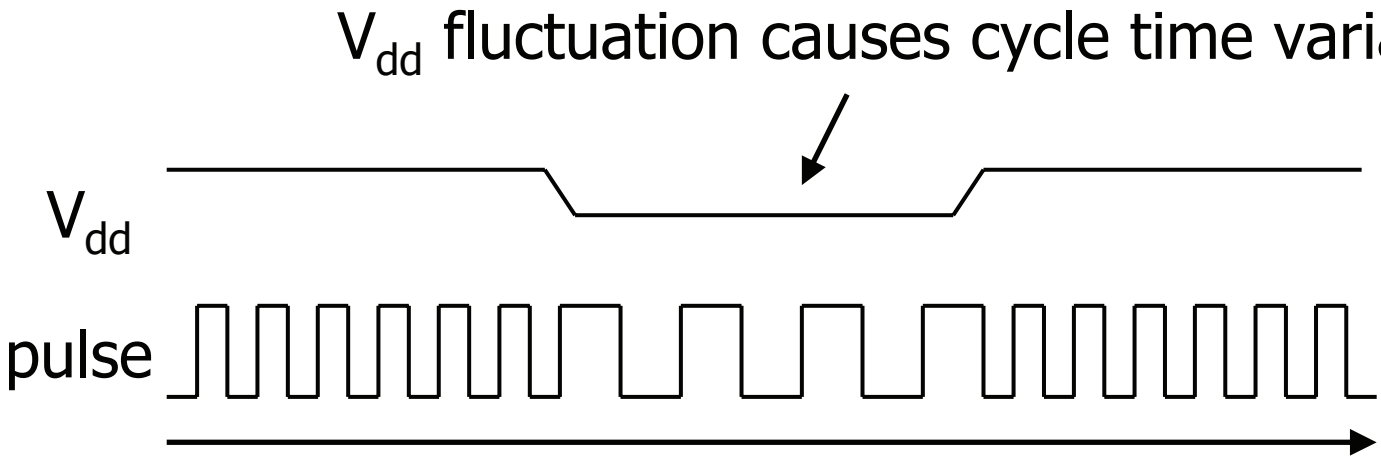
SoC Power Integrity Verification

- Measurement circuit suitable for embedding
  - Area
  - Layout/routing cost
  - Circuit design cost
  - Synchronization with clock for digital circuit

	sample & hold	Improved ring osci.[1]	Proposed circuit
Time/voltage resolution	◎	○	○
Circuit design cost	X	○	◎
Physical design cost for embedding	△	◎	◎
area		○	○
synchronization with clock	○	X	○

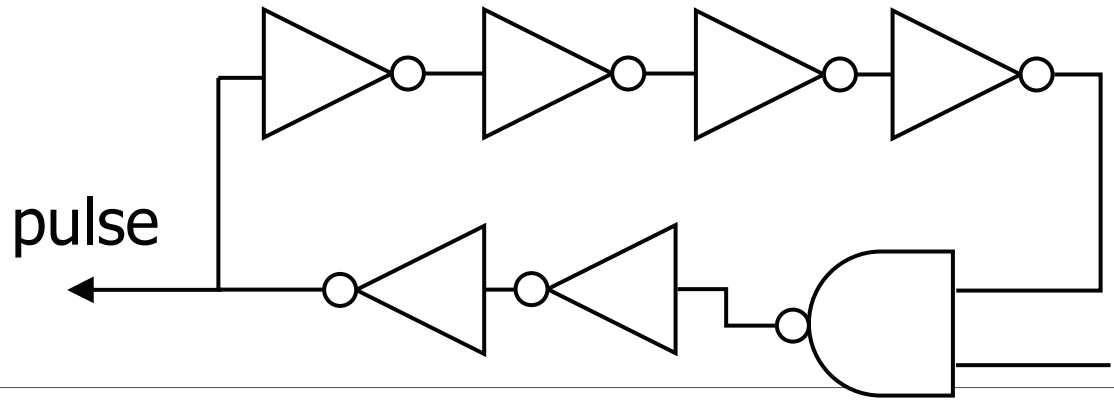
[1] T. Sato, et. al, CICC 2006

Ordinary ring oscillator



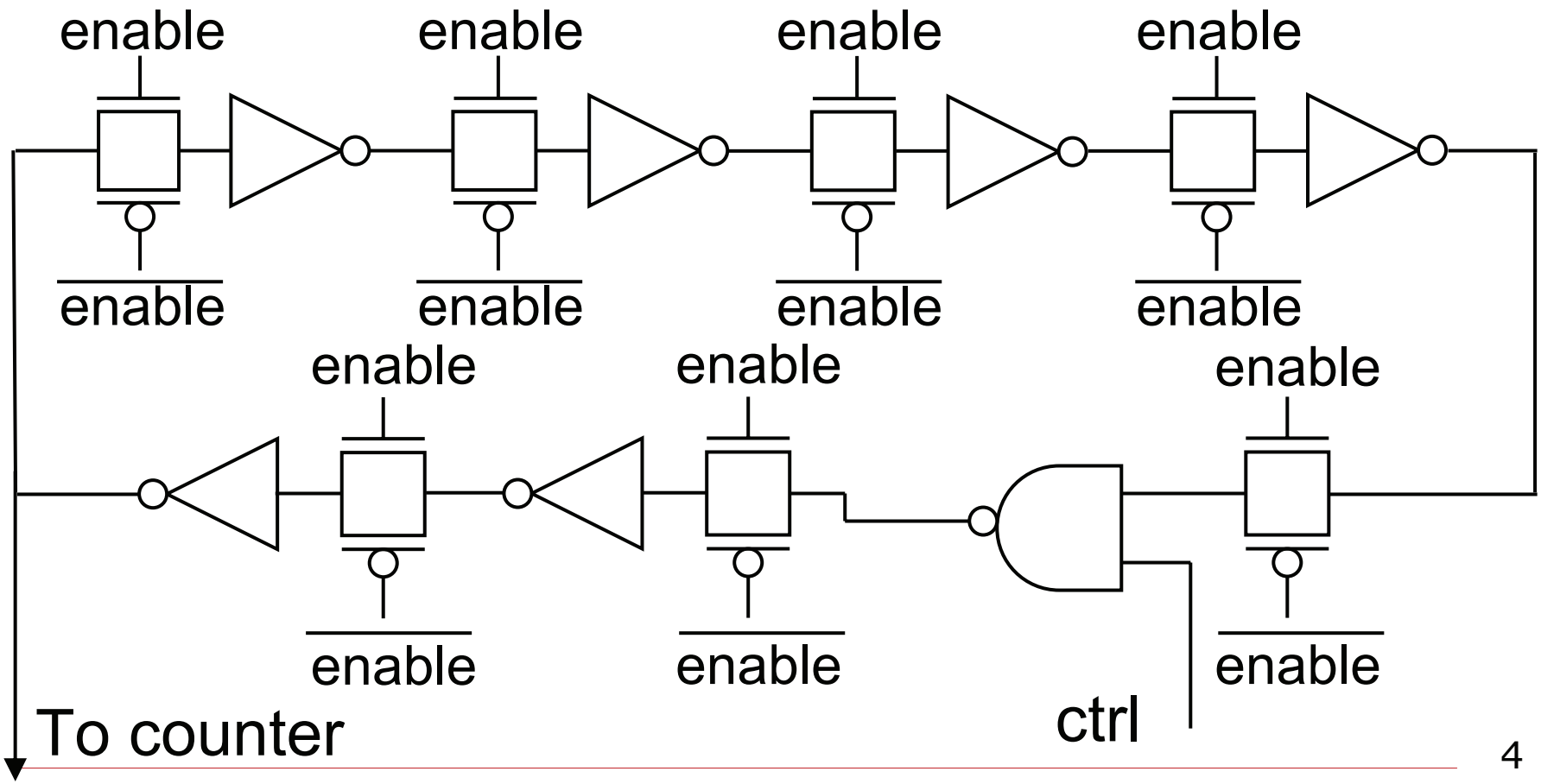
Operating continuously

→ V_{dd} at specific timing cannot be observed.
(Average of V_{dd} is observed)



Proposed ``gated oscillator”

- Transmission gates are inserted into ring oscillator.
- Holding oscillation state with transmission gates



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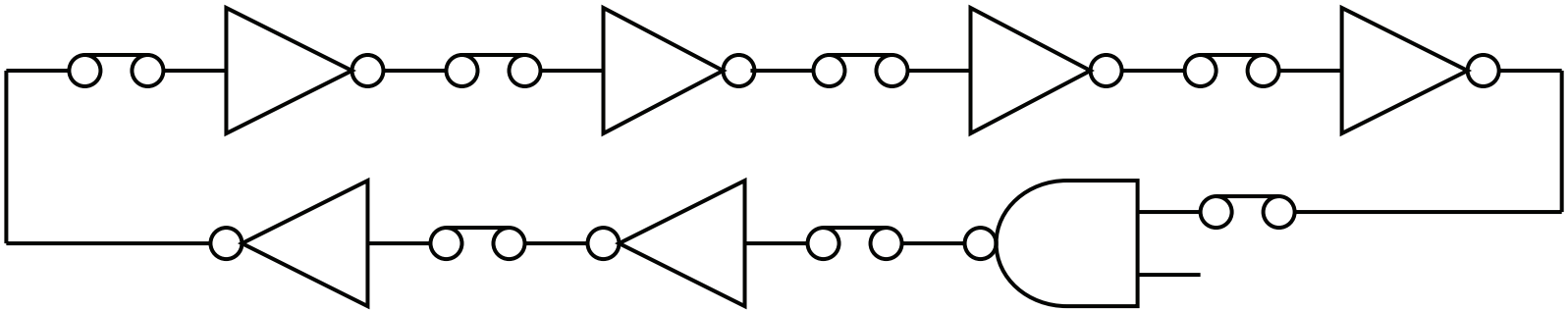

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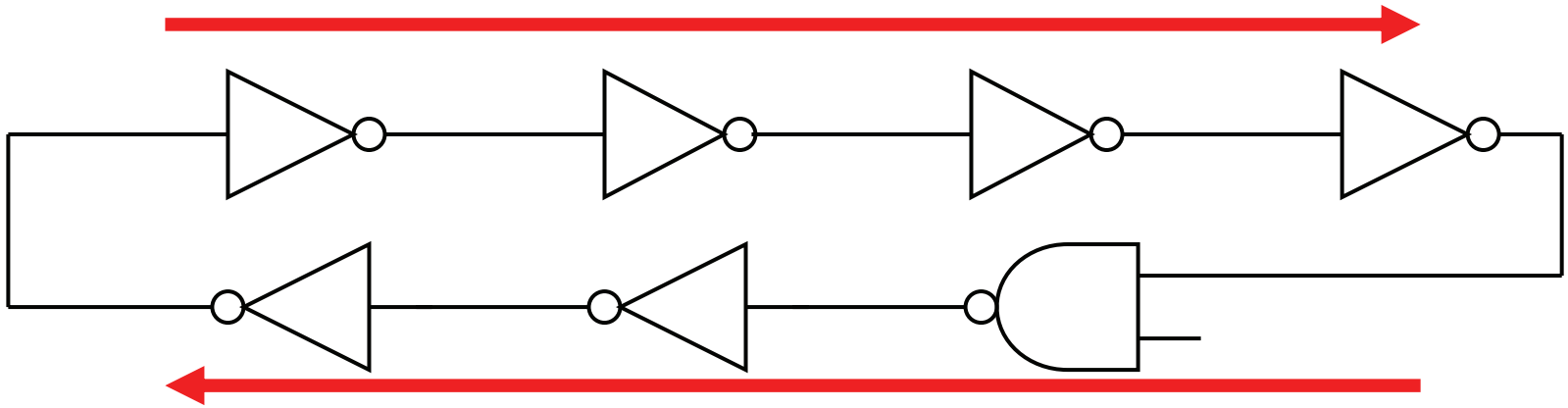

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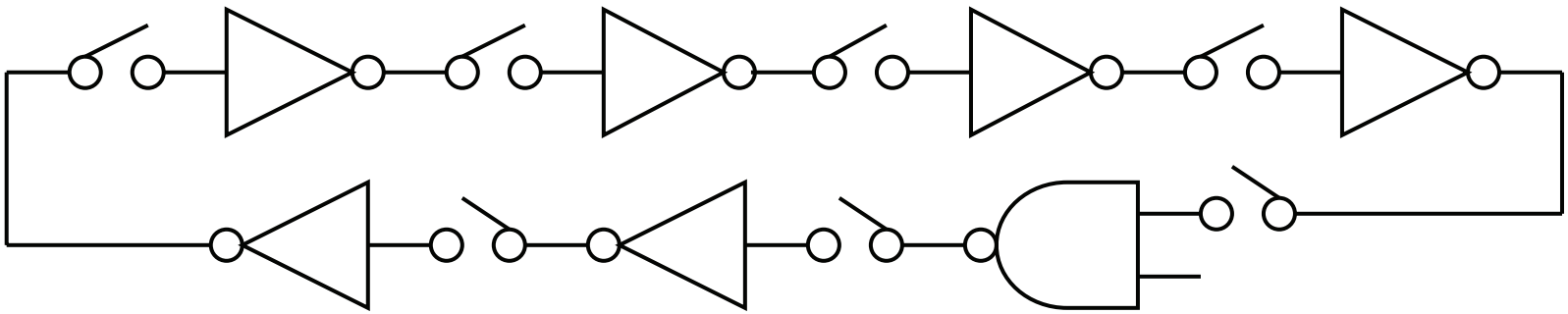

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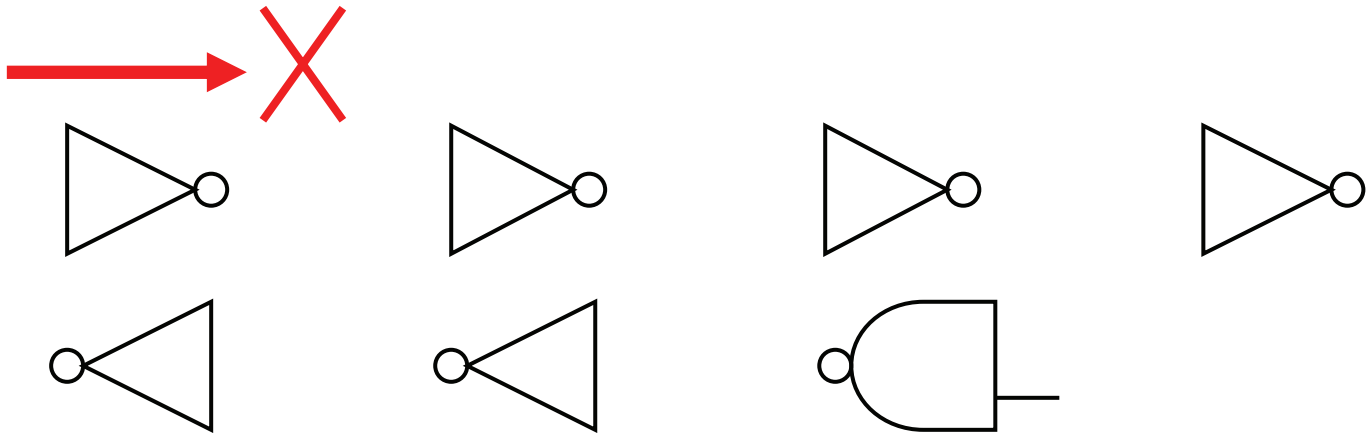
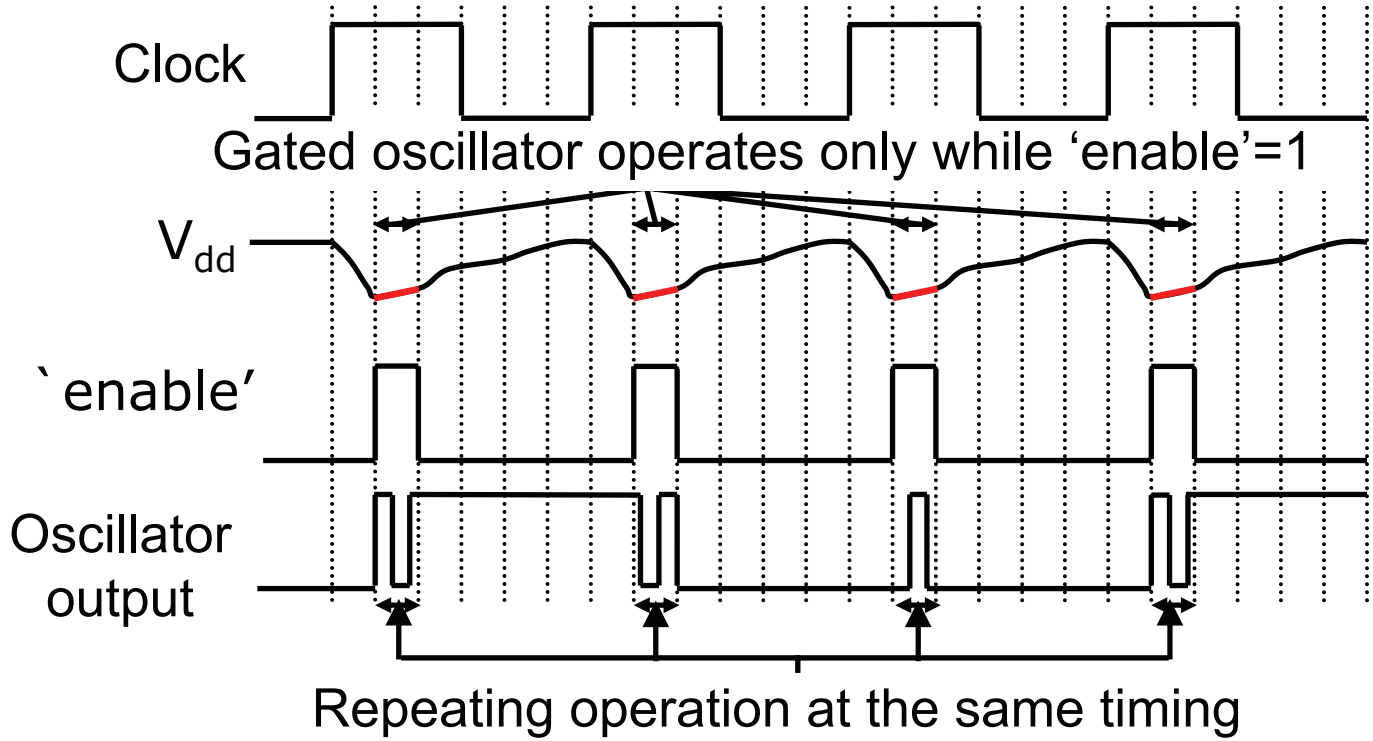


Operation of gated oscillator

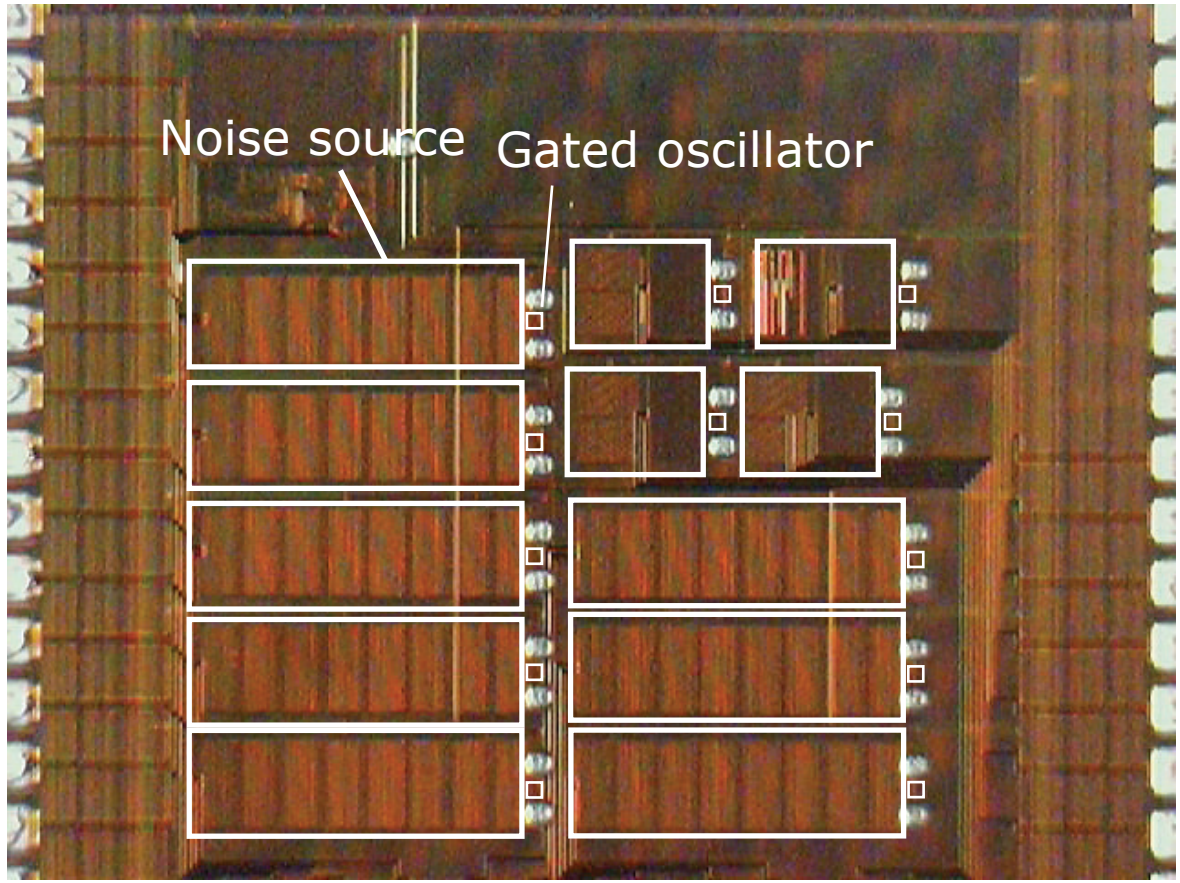
- Operating only while `enable'=1
  → Capturing V_{dd} at specified timing
- Accumulating cycle count by repetition



Micrograph of test chip

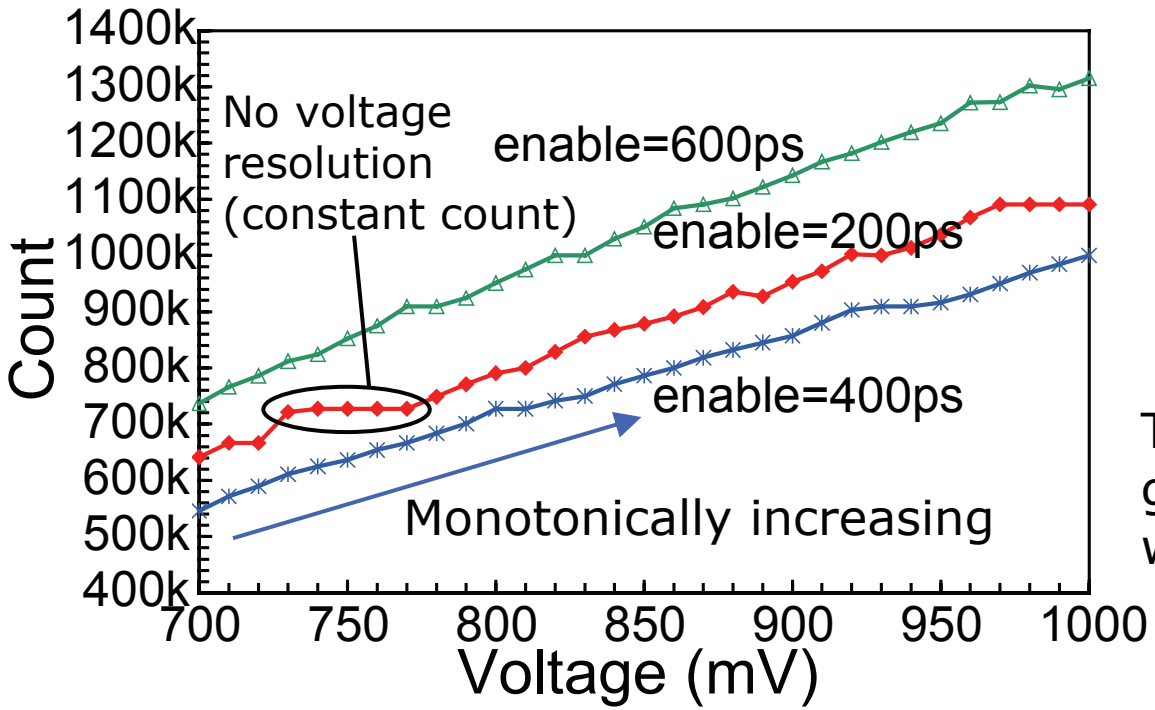
Process: 90nm CMOS
Supply voltage: 1.0V
Area: 1.54 x 1.54mm
Num. of gates: 100k

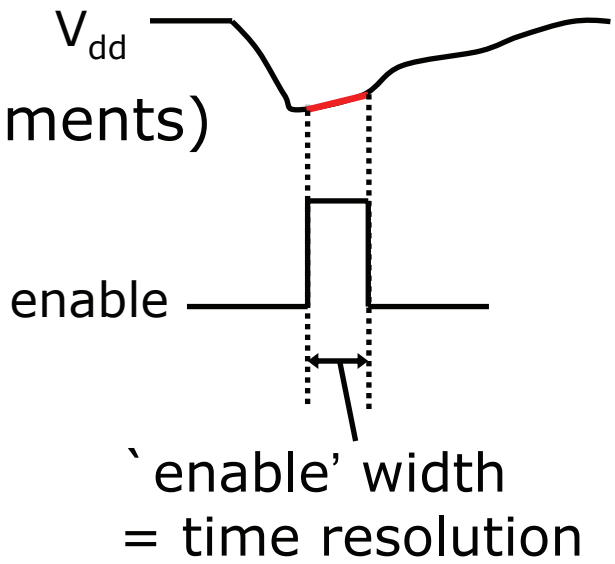
Test structures including noise sources and gated oscillators are implemented.



Voltage resolution of ``gated oscillator''

- 10-20mV voltage resolution with 400ps `enable' signal width (= 2.5G sampling)
- Max. σ = 0.98% (1000 measurements)
  - Fine reproducibility

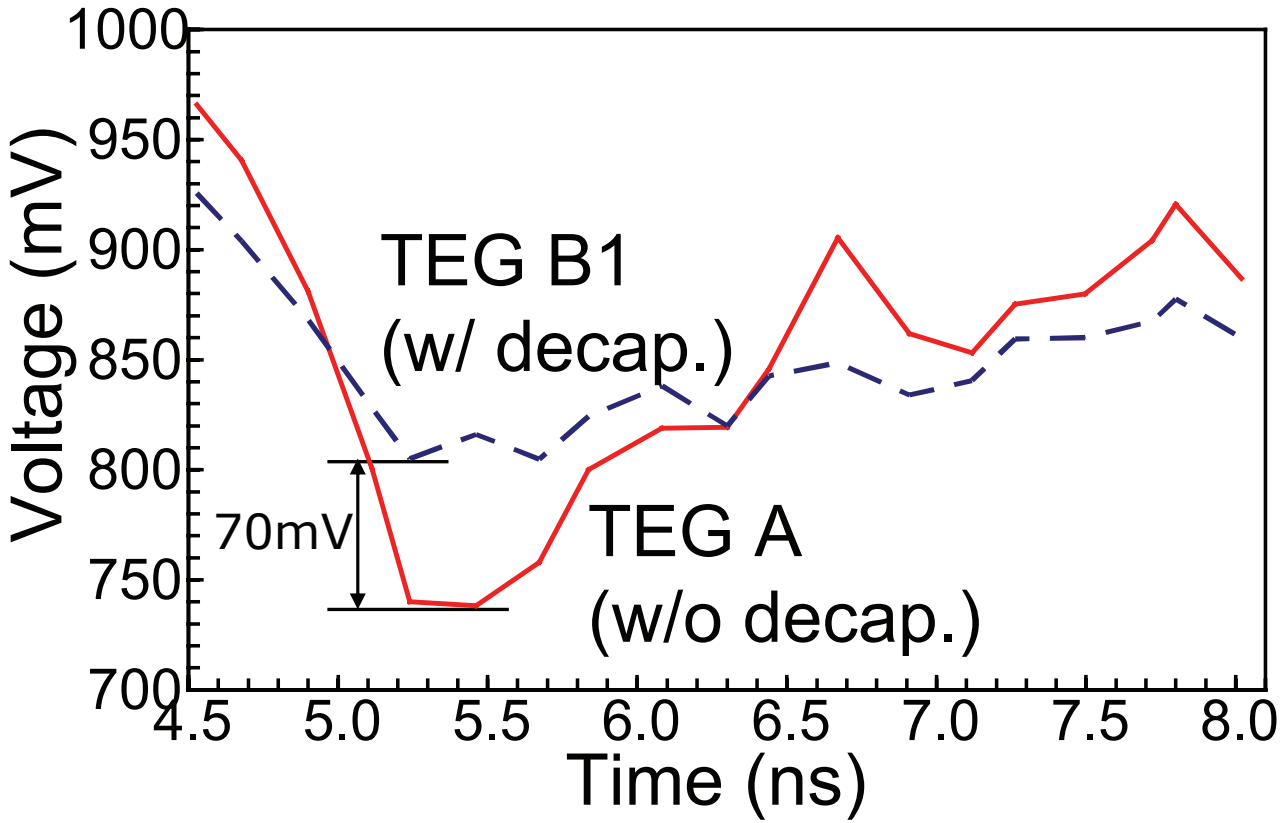




The cycle count of gated oscillator is measured with stable supply voltage.

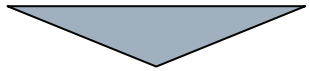
Waveform observation

- 70mV difference of peak drop was observed.
- Dynamic noise waveform is observed with gated oscillator.



Features of proposed circuit

- Waveform sampling with digital circuit
  - Consisting of standard cells
  - Dedicated power and bias lines are not needed.



  - Circuit design is easy.
  - Physical design (place, route) cost is small.
  - Size and shape are flexible.
- Small area
  - 11.76μm X 15.12μm
    (A layout sample in 90nm process)
- Synchronization with any external clock

  - Application for SoC power integrity verification

Thank you