Dynamics Assessment of Advanced Single-Phase PLL Structures

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***Abstract*—Recently, several advanced phase-locked loop (PLL) techniques have been proposed for single-phase applications. Among these, the Park-PLL and the second-order-generalized-integrator-based PLL are very attractive, owing to their simple digital implementation, low computational burden, and desired performance under frequency-varying and harmonically distorted grid conditions. Despite the wide acceptance and use of these two advanced PLLs, no comprehensive design guidelines to fine-tune their parameters have been reported yet. Through a detailed mathematical analysis, it is shown that these two PLL structures are equivalent to each other, from the control point of view. Then, a linearized model is developed which is valid for both PLLs. The derived model significantly simplifies the stability analysis and the parameter design. To fine-tune the PLL parameters, a systematic design approach is suggested afterward, which guarantees a fast dynamic response, a high disturbance rejection ability, and a robust performance. Finally, the simulation and experimental results are presented to support the theoretical analysis.**

***Index Terms*—Frequency estimation, orthogonal signal generator (OSG), phase estimation, phase-locked loop (PLL), second-order generalized integrator (SOGI), single phase, small-signal modeling.**

I. Introduction

SYNCHRONIZATION with the utility grid is one of the most important aspects in the control of an increasing number of single-phase grid-tied power conditioning systems such as active power filters [1], dynamic voltage restorers [2], [3], uninterruptible power supplies [4], and distributed power generation and storage systems [5].

Various synchronization techniques have been proposed in recent years. Zero-crossing-detection-based methods [6], [7], Kalman filtering [8], digital Fourier transform and its modifications [9], [10], recursive weighted least squares estimation algorithms [11], artificial neural networks [12], the methods based on the concept of adaptive notch filter [13], [14], and phase-locked loop (PLL)-based algorithms [3]–[5], [15]–[23] are among the existing synchronization techniques.

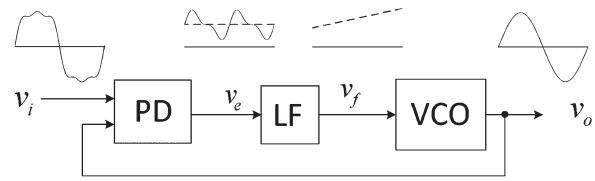

Fig. 1. Basic scheme of the single-phase PLL.

Among the various synchronization techniques, PLLs have found much attention, mainly due to their simplicity, robustness, and effectiveness. A PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with an input signal. Commonly, all PLL techniques are composed of three building blocks, as shown in Fig. 1: 1) phase detector (PD); 2) loop filter (LF); and 3) voltage-controlled oscillator (VCO). The main difference among different PLLs typically lies in how the PD block is implemented.

Mixers or product-type PD systems have a long history of use, particularly in the field of communications [24]. A product-type PD accepts two signals at two different frequencies (i.e., the reference and estimated frequencies) and generates a signal at the difference and sum of the two input frequencies. Despite the simplicity, a product-type PD suffers from a major drawback, i.e., generating a high-amplitude double-frequency term at its output in steady-state conditions [4]. Depending on the PLL's bandwidth, this undesired term can cause steady-state oscillations in the estimated phase/frequency. To overcome this drawback, an effective solution, referred to as the modified mixer PD, has been proposed by Thacker *et al.* [20]. In this method, the low-frequency oscillations in the estimated phase/frequency are significantly suppressed by placing a peak voltage detection scheme at the input of PLL and adding another trigonometric term to the standard mixer PD.

Transformation-based PDs (T-PDs) are very popular in three-phase systems, due to their simplicity and effectiveness [21]. However, for single-phase applications, because of the lack of multiple independent input signals, their implementation is more complicated [22], [23]. Thus, some techniques to create an orthogonal signal from the original single-phase input signal have been proposed. The earliest, and probably the simplest, orthogonal signal generator (OSG) is a transfer delay block [25].

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This technique gives satisfactory results if the grid frequency is at its rated value. However, when the grid voltage undergoes frequency variations, the output signal of the OSG will not be exactly orthogonal, which results in errors in the estimated phase/frequency by the PLL [26]. Another drawback of this approach is its no filtering capability [26]. In [27], the orthogonal signal is generated by differentiating the original signal. The noise amplification caused by derivative function is the main drawback of this approach. A Hilbert-transform-based OSG is presented in [28]. While this method provides satisfactory performance under ideal operation conditions, it suffers from two main drawbacks: poor performance under frequency-varying conditions [29] and high computational burden [30]. In [31], a Kalman-filter-based OSG is proposed, which provides a desired performance even under frequency-varying conditions. This approach suffers from high complexity [32]. An all-pass-filter-based OSG is suggested by Kim *et al.* [33]. This technique does not provide any filtering capability. Thus, it may not be a proper choice under distorted grid conditions. A simple and practical solution to generate the orthogonal signal is that proposed by Ciobotaru *et al.* [34], in which a second-order generalized integrator (SOGI) is utilized. Frequency adaptive performance, low computational burden, and relatively high filtering capability are the advantages of this method, which make it a successful solution for harmonically distorted and frequency-varying conditions. Another successful approach of creating the orthogonal signal, as reported in [30] and [35], uses the inverse Park transformation. This approach has the same unique features as the SOGI-based OSG. It is worth noting that a successful implementation of a T-PD, which does not require the generation of an orthogonal signal, can be found in [36].

In recent years, the PLLs based on SOGI and inverse Park OSGs (typically, referred to as the SOGI-PLL and the Park-PLL, respectively) have received much attention, owing to their simple digital implementation, low computational burden, and desired performance under frequency-varying and harmonically distorted grid conditions. Despite the wide acceptance and use of these PLLs in a variety of applications [4], [37]–[40], no comprehensive design guidelines to fine-tune their parameters have been reported, until now. For sure, some design instructions can be found in the literature [4], [26], [34], which do some simplifying assumptions such as neglecting the interaction between the OSG block and the LF and VCO blocks. Evidently, these simplified and suboptimal approaches are not able to extract the maximum benefits out of the PLL potentialities.

Through a detailed mathematical analysis, it is shown in this paper that the SOGI-PLL and Park-PLL are equivalent to each other, from the control point of view. Then, a small-signal linearized model for both PLL structures is derived. The derived model significantly simplifies the stability analysis and the parameter design. The parameter design guidelines are suggested afterward, ensuring a fast transient response, a high disturbance rejection capability, and a robust performance.

The rest of this paper is organized as follows. Section II introduces two PLL structures. The equivalence of the two PLL structures is also demonstrated in this section. A linearized model for both PLLs is then derived in Section III. A systematic design method for tuning of the PLL parameters is presented in Section IV. Evaluation results are presented in Section V. Finally, Section VI concludes this paper.

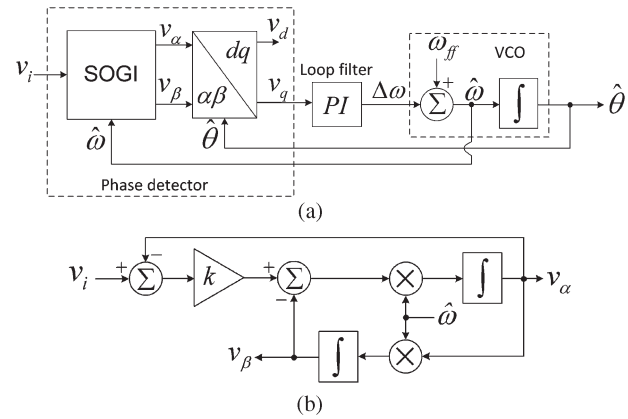

Fig. 2. SOGI-PLL. (a) Basic structure. (b) SOGI block.

II. Overview of the Two PLL Structures

In this section, a brief overview of the SOGI-PLL and the Park-PLL is presented. In each case, the general structure is presented, and its principle of operation is explained. The equivalence of the two PLL structures is also demonstrated.

A. SOGI-PLL

Fig. 2(a) shows the general structure of the SOGI-PLL proposed by Ciobotaru *et al.* [34], in which v_i is the input voltage, $\hat{\omega}$ and $\hat{\theta}$ $(= \hat{\omega}t + \hat{\phi})$ are the estimated frequency and angle, respectively, and ω_{ff} is the nominal frequency. The implementation of the SOGI block is shown in Fig. 2(b), and the Park $(\alpha\beta \rightarrow dq)$ transformation is defined as follows:

$$T = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix}. \tag{1}$$

From Fig. 2(b), the characteristic transfer functions of the SOGI block can be derived as

$$G_\alpha(s) = \frac{v_\alpha(s)}{v_i(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{2}$$

$$G_\beta(s) = \frac{v_\beta(s)}{v_i(s)} = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{3}$$

where k (commonly referred to as the damping factor) is a constant term.

Fig. 3(a) and (b) shows the Bode plots of transfer functions (2) and (3), respectively, for three different values of the damping factor k and for $\hat{\omega} = 2\pi 50$ rad/s. Based on these plots, the following can be concluded.

1) The transfer function G_α exhibits a bandpass filtering behavior with a center frequency of $\hat{\omega}$. The width of the passband is determined by the damping factor k and is independent of $\hat{\omega}$. The lower k leads to a narrower bandwidth and, hence, better filtering capability. If, somehow, it is provided that $\hat{\omega} = \omega$ (i.e., the estimated frequency is equal to the real one), then v_α will match in amplitude as

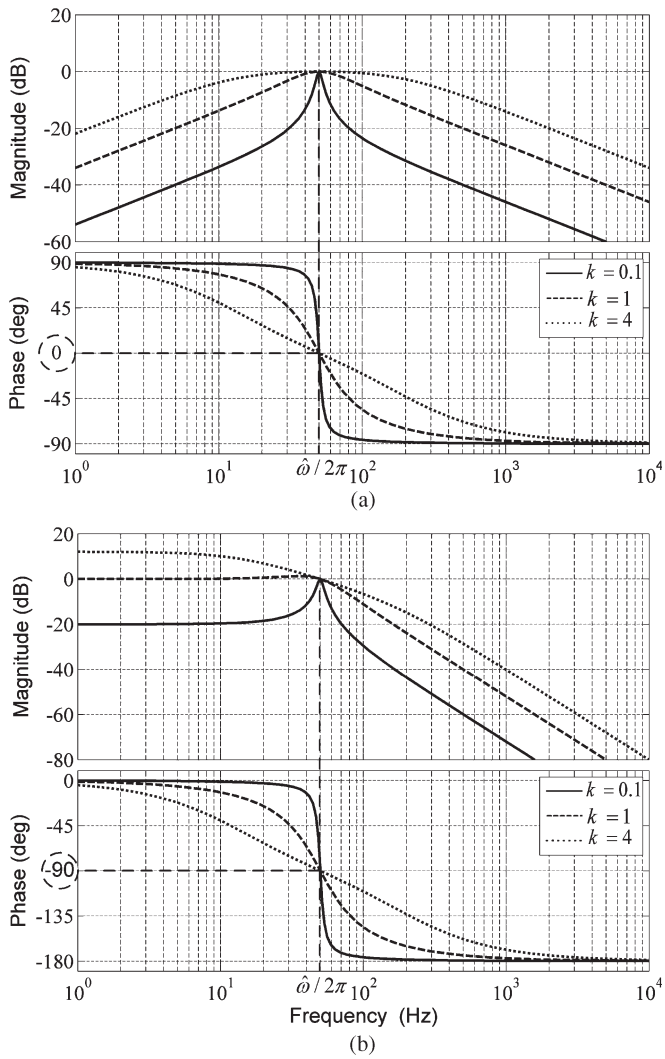

Fig. 3. Bode plots of the characteristic transfer functions of the SOGI block for different values of k: (a) $G_\alpha = v_\alpha/v_i$ and (b) $G_\beta = v_\beta/v_i$.

well as in phase with the fundamental component of the input voltage v_i.

2) The transfer function G_β exhibits a low-pass filtering characteristic. Again, if $\hat{\omega} = \omega$, then v_β will match in amplitude but with a 90° difference with the fundamental component of the input voltage v_i.

Let us assume that $v_i = V\cos(\omega t + \phi)$, where V, ω, and ϕ are the input voltage amplitude, frequency, and phase, respectively. Then, under frequency-locked condition (i.e., $\omega = \hat{\omega}$) and for $k < 2$, the mathematical expressions for v_α and v_β, when the input voltage is suddenly applied, are

$$v_\alpha(t) = V\cos(\omega t + \phi) + A_\alpha \cos\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\alpha\right) e^{-\frac{k\omega}{2}t} \quad (4)$$

$$v_\beta(t) = V\sin(\omega t + \phi) + A_\beta \sin\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\beta\right) e^{-\frac{k\omega}{2}t} \quad (5)$$

where A_α, A_β, ϕ_α, and ϕ_β are functions of V, ϕ, and k.

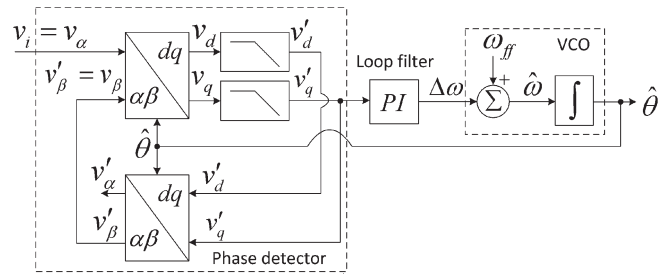

Fig. 4. Park-PLL.

As expected, in steady state, v_α and v_β are in phase and quadrature phase with the input voltage, respectively. Applying the transformation matrix (1) to (4) and (5) yields v_d and v_q signals as expressed in

$$v_d(t) = V\cos(\phi - \hat{\phi}) + \left[A_\alpha \cos\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\alpha\right)\cos(\omega t + \hat{\phi}) + A_\beta \sin\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\beta\right)\sin(\omega t + \hat{\phi})\right] \times e^{-\frac{k\omega}{2}t} \quad (6)$$

$$v_q(t) = V\sin(\phi - \hat{\phi}) - \left[A_\alpha \cos\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\alpha\right)\sin(\omega t + \hat{\phi}) - A_\beta \sin\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\,t + \phi_\beta\right)\cos(\omega t + \hat{\phi})\right] \times e^{-\frac{k\omega}{2}t} \quad (7)$$

respectively. Note that the second terms on the right-hand side of (6) and (7) decay to zero in steady state. Hence, for a small phase difference $\phi - \hat{\phi}$, v_d yields an estimation of the input voltage amplitude, and v_q gives the phase error information.

To further attenuate the high-frequency noises, the PD output signal, i.e., v_q, is passed through the LF (here, a proportional–integral controller). The nominal value of the fundamental frequency (i.e., ω_{ff}) is then added to the LF output signal, to reduce the control effort and expedite the initial lock-in process. The resulting signal (i.e., $\hat{\omega}$) is integrated afterward, to generate the estimated angle $\hat{\theta}$.

B. Park-PLL

Fig. 4 shows the general structure of the Park-PLL [30], [35]. In this PLL, the required orthogonal signal (i.e., v_β) is generated by applying the inverse Park transformation to the filtered direct and quadrature signals, i.e., v'_d and v'_q, respectively. The PD dynamics mainly depends on the characteristics of the low-pass filters (LPFs) used to filter out the possible harmonics/noises from v_d and v_q. The LPFs are of first order, as follows:

$$LPF(s) = \frac{\omega_p}{s + \omega_p} \quad (8)$$

where ω_p is the cutoff frequency of the LPF.

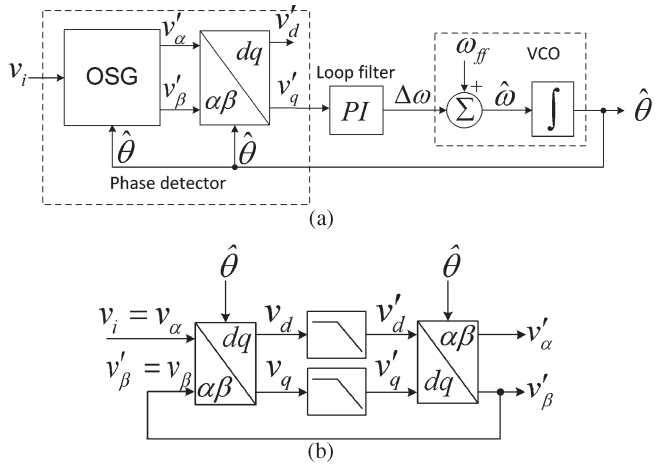

Fig. 5. Park-PLL. (a) Modified structure. (b) OSG block.

It is demonstrated in the next section that the Park-PLL and SOGI-PLL are equivalent to each other. Thus, a more detailed examination of the Park-PLL sounds unnecessary.

C. Equivalence of Two PLL Structures

To simplify the analysis, let us redraw the Park-PLL structure as shown in Fig. 5(a), where the OSG block is shown in Fig. 5(b). By making an analogy with SOGI-PLL [Fig. 2(a)], one can see that the only difference between the two PLL structures lies in the PD block. In the following, it is demonstrated that the OSG block in Fig. 5(b) is equivalent to the SOGI block in Fig. 2(b).

In control system terms, the OSG block shown in Fig. 5(b) is a single-input two-output system, which can be described in time domain as expressed in

$$\begin{bmatrix} v'_\alpha(t) \\ v'_\beta(t) \end{bmatrix} = \underbrace{\begin{bmatrix} \cos\hat{\theta} & -\sin\hat{\theta} \\ \sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix}}_{\alpha\beta\leftarrow dq} \times \left\{ \underbrace{\begin{bmatrix} LPF(t) & 0 \\ 0 & LPF(t) \end{bmatrix}}_{\text{low-pass filter}} * \left\{ \underbrace{\begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix}}_{dq\leftarrow\alpha\beta} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \right\} \right\} \tag{9}$$

where * is the convolution operator. Taking the Laplace transform of both sides of (9) and performing some mathematical manipulations, we can derive (10), shown at the bottom of the page [41]. Substituting the LPF transfer function (8) into (10), and performing some mathematical simplifications, gives

$$\begin{bmatrix} v'_\alpha(s) \\ v'_\beta(s) \end{bmatrix} = \begin{bmatrix} \frac{\omega_p(s+\omega_p)}{s^2+2\omega_p s+\omega_p^2+\hat{\omega}^2} & \frac{-\hat{\omega}\omega_p}{s^2+2\omega_p s+\omega_p^2+\hat{\omega}^2} \\ \frac{\hat{\omega}\omega_p}{s^2+2\omega_p s+\omega_p^2+\hat{\omega}^2} & \frac{\omega_p(s+\omega_p)}{s^2+2\omega_p s+\omega_p^2+\hat{\omega}^2} \end{bmatrix} \begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix}. \tag{11}$$

Substituting $v_\alpha = v_i$ and $v_\beta = v'_\beta$ into (11) yields the characteristic transfer functions of the OSG block as given in

$$G'_\alpha(S) = \frac{v'_\alpha(s)}{v_i(s)} = \frac{\omega_p s}{s^2+\omega_p s+\hat{\omega}^2} \tag{12}$$

$$G'_\beta(S) = \frac{v'_\beta(s)}{v_i(s)} = \frac{\omega_p \hat{\omega}}{s^2+\omega_p s+\hat{\omega}^2}. \tag{13}$$

Comparing (12) and (13) with (2) and (3), respectively, one can see that, for $\omega_p = k\hat{\omega}$, the characteristic transfer functions of the OSG block are the same as those of the SOGI block, resulting in the same properties for the two PLL strategies.

It is worth remarking that, due to the variations of the input frequency (and, hence, the estimated frequency), the equivalent condition (i.e., $\omega_p = k\hat{\omega}$) may not be exactly satisfied. However, since the grid frequency is typically allowed to change in a narrow band (e.g., 47 Hz $< \omega <$ 52 Hz, as defined in [42]), selecting $\omega_p = k\omega_{\text{ff}}$ gives rise to similar properties for both PLL techniques, as it will be shown later in Section V.

III. Linearized Model

In this section, a linearized model for SOGI-PLL is presented, which is also valid for Park-PLL, due to the equivalence of the two PLL structures. To derive the linearized model, the following are assumed.

1) The estimated frequency is almost equal to the real one (i.e., $\omega \cong \hat{\omega}$).
2) There is a small difference between the real and estimated phase angles; thus, $\sin(\phi - \hat{\phi}) \cong \phi - \hat{\phi}$, and $\cos(\phi - \hat{\phi}) \cong 1$.
3) The input voltage is polluted with harmonics and is represented by

$$v_i = V\cos(\omega t + \phi) + \sum_{h=3,5,7,\ldots} V_h \cos(h\omega t + \phi_h) \tag{14}$$

where V_h and ϕ_h are the amplitude and phase angle of the hth harmonic component, respectively.

First, let us neglect the harmonic components and consider a pure sine wave as the input voltage. In this case, the PD output signal (i.e., v_q) is as expressed in (7). Note that, in (7), the fluctuating terms decay to zero with a time constant of $2/k\omega$ and v_q converges to $V(\phi - \hat{\phi})$. Thus, for a step phase change, the PD output signal can be approximated in Laplace domain as

$$v_q(s) \cong \frac{V}{\tau_p s + 1}\phi_e(s) \tag{15}$$

where $\phi_e = \phi - \hat{\phi}$ and $\tau_p = 2/k\omega$.

Once the PD response to a pure sine wave is determined, the next step is to take into account the harmonic components. Note

$$\begin{bmatrix} v'_\alpha(s) \\ v'_\beta(s) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} LPF(s+j\hat{\omega}) + LPF(s-j\hat{\omega}) & -jLPF(s+j\hat{\omega}) + jLPF(s-j\hat{\omega}) \\ jLPF(s+j\hat{\omega}) - jLPF(s-j\hat{\omega}) & LPF(s+j\hat{\omega}) + LPF(s-j\hat{\omega}) \end{bmatrix} \begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} \tag{10}$$

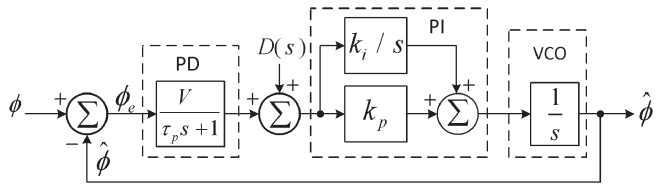

Fig. 6. Linearized model valid for both PLL structures.

that we are only concerned with the steady-state effect of the input harmonics on the estimated variables by the PLL.

In steady-state condition, an input harmonic component (of order h) leads to two different components (of orders $h \pm 1$) after the PD. This can be mathematically expressed as

$$\begin{aligned} q_h(t) = &\frac{(h+1)}{2} V_h \left|G_\beta(jh\omega)\right| \\ &\times \cos\left[(h-1)\omega t + \phi_h - \hat{\phi} + \measuredangle G_\beta(jh\omega)\right] \\ &- \frac{(h-1)}{2} V_h \left|G_\beta(jh\omega)\right| \\ &\times \cos\left[(h+1)\omega t + \phi_h + \hat{\phi} + \measuredangle G_\beta(jh\omega)\right] \end{aligned} \quad (16)$$

in which $|G_\beta(jh\omega)|$ and $\measuredangle G_\beta(jh\omega)$ denote the magnitude and the phase angle of the transfer function $G_\beta(s)$, respectively, for $s = jh\omega$. Thus, to consider the input voltage harmonics as well, the PD output signal must be rewritten as follows:

$$v_q(s) \cong \frac{V}{\tau_p s + 1}\phi_e(s) + D(s) \quad (17)$$

where $D(s) = L\sum_{h=3,5,7,\ldots} q_h(t)$, in which L denotes the Laplace operator.

Based on the aforementioned analysis, the linearized model of the SOGI-PLL can be obtained as shown in Fig. 6, where k_p and k_i are the proportional and integral gains, respectively. This model is also valid for Park-PLL, if the time constant τ_p is set to $2/\omega_p$. Note that $D(s)$ appears as a disturbance input to the PLL linearized model. It is worthwhile mentioning here that the derived linearized model is highly accurate for a k within the range of (0, 2) [or an ω_p within the range of $(0, 2\omega_{\text{ff}})$]. Obviously, beyond this range, the accuracy of the model starts to decrease.

IV. Design Guidelines

In this section, a systematic design method to fine-tune the PLL parameters is proposed. For the sake of simplicity, in the PLL linearized model, the input voltage amplitude V is assumed to be unity. This assumption can be simply realized by dividing the PD output signal by an estimation of the input voltage amplitude before it was fed into the LF. In this case, the disturbance input to the linearized model [i.e., $D(s)$] must be replaced by $D'(s)$, as shown in Fig. 7, where $D'(s) = D(s)/V$.

A. Stability

The main focus of this section is to establish a criterion, based on the extended symmetrical optimum method [43], [44], so that the maximum possible stability margin for the PLLs is achieved. Application of this method to the PLL-based frequency synthesizers can be found in [44].

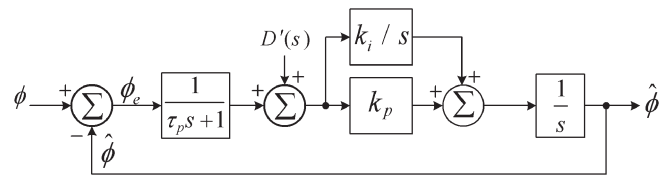

Fig. 7. Modified linearized model.

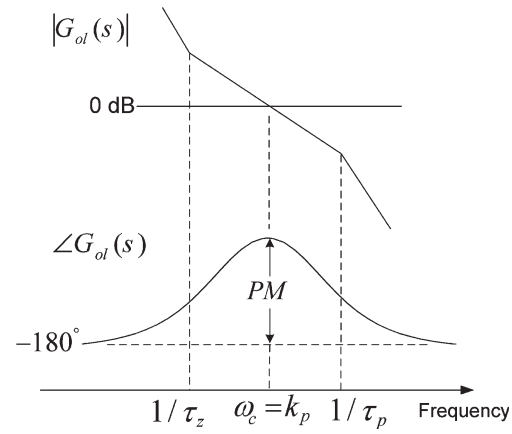

Fig. 8. Logarithmic plot of the open-loop transfer function.

From Fig. 7, considering $k_p/k_i = \tau_z$, the open-loop transfer function can be derived as

$$G_{\text{ol}}(s) = \left.\frac{\hat{\phi}(s)}{\phi_e(s)}\right|_{D'(s)=0} = \frac{k_i(\tau_z s + 1)}{s^2(\tau_p s + 1)}. \quad (18)$$

From (18), the phase margin (PM) can be simply obtained as

$$PM = \underbrace{\tan^{-1}(\tau_z\omega_c)}_{\phi_z} - \underbrace{\tan^{-1}(\tau_p\omega_c)}_{\phi_p} \quad (19)$$

where ω_c is the crossover frequency and is determined by

$$\omega_c = k_p\frac{\cos(\phi_p)}{\sin(\phi_z)}. \quad (20)$$

Taking the derivative of (19) with respect to ω_c, and equating the result to zero, gives [44]

$$\omega_c = \frac{1}{\sqrt{\tau_z\tau_p}}. \quad (21)$$

Substituting (21) into (20) yields

$$\omega_c = k_p. \quad (22)$$

From (21) and (22), it can be concluded that, for given values of τ_z and τ_p, the PLL PM is maximized, if the crossover frequency ω_c is equal to the proportional gain k_p. This is graphically shown in Fig. 8.

From (21), supposing that $\tau_z = b^2\tau_p$, where b is a constant term, we can obtain

$$\begin{cases} \tau_z\omega_c = b \\ \tau_p\omega_c = \frac{1}{b}. \end{cases} \quad (23)$$

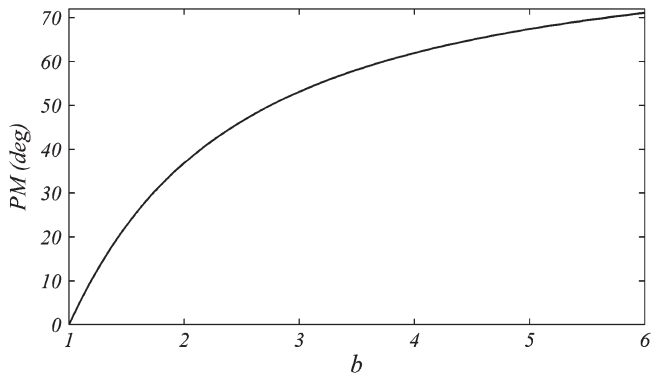

Fig. 9. PM as a function of b.

Substituting (23) into (19) and after some mathematical manipulations, we derive

$$PM = \tan^{-1} \frac{b^2 - 1}{2b}. \tag{24}$$

Fig. 9 shows the PM as a function of b. It can be seen that a higher b results in a higher PM and, hence, a more stable operation.

Typically, a PM within the range of 30°–60° is recommended [45]. To achieve this, we require that $1.732 < b < 3.732$.

B. Transient Performance

The main focus of this section is to minimize the PLL settling time in response to the phase and frequency step changes.

Substituting (22) and (23) into (18), the open-loop transfer function $G_{\rm ol}(s)$ can be rewritten as

$$G_{\rm ol}(s) = \frac{b\omega_c^2 s + \omega_c^3}{s^2(s + b\omega_c)}. \tag{25}$$

Notice that the open-loop transfer function in (25) describes a type-2 system (i.e., there are two poles at the origin). Hence, the PLL tracks both phase jump (step input) and frequency jump (ramp input) with zero steady-state error [24].

From Fig. 7, the phase error transfer function relating the phase error ϕ_e to the phase input ϕ can be obtained as

$$G_e(s) = \left.\frac{\phi_e(s)}{\phi(s)}\right|_{D'(s)=0} = \frac{1}{1 + G_{\rm ol}(s)}. \tag{26}$$

Substituting (25) into (26) and after some mathematical manipulations, we have

$$G_e(s) = \frac{s^2(s + b\omega_c)}{(s + \omega_c)\left(s^2 + (b-1)\omega_c s + \omega_c^2\right)}. \tag{27}$$

Supposing that $\omega_c = \omega_n$ and $\zeta = (b-1)/2$, (27) can be rewritten as

$$G_e(s) = \frac{s^2\left(s + (2\zeta + 1)\omega_n\right)}{(s + \omega_n)\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)} \tag{28}$$

where ω_n is the natural frequency and ζ is the damping factor.

Using (28), the Laplace transforms of the phase error in response to the phase and frequency jumps can be simply obtained as expressed in (29) and (30), respectively

$$\phi_e^{\Delta\phi}(s) = \frac{\Delta\phi}{s} G_e(s) = \frac{s\left(s + (2\zeta + 1)\omega_n\right)\Delta\phi}{(s + \omega_n)\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)} \tag{29}$$

$$\phi_e^{\Delta\omega}(s) = \frac{\Delta\omega}{s^2} G_e(s) = \frac{\left(s + (2\zeta + 1)\omega_n\right)\Delta\omega}{(s + \omega_n)\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)}. \tag{30}$$

Taking the inverse Laplace transform from (29) and (30) yields (31) and (32), respectively, shown at the bottom of the page [44].

From (31) and (32), it is clear that, for both phase and frequency jumps and for all values of ζ, the PLL transient-response speed is proportional to the natural frequency ω_n. Thus, to achieve a faster transient response, ω_n must be chosen as high as possible. However, a high value of ω_n degrades the disturbance rejection ability of the PLL. Hence, one has to find a satisfactory compromise.

It was shown in the previous section that the proper operation of the PLL in terms of stability requires $1.732 < b < 3.732$ and, hence, $0.366 < \zeta < 1.366$. It can be shown simply that, for this range of variations, ζ has a relatively little effect on the disturbance rejection ability of the PLL. Therefore, ω_n must be chosen to meet the disturbance rejection requirements of the PLL, and ζ must be chosen to provide a fast transient response as well as a stable operation.

Fig. 10 shows the normalized simulated settling time as a function of ζ, for both phase jump (solid line) and frequency jump (dotted line). The normalizing factor is the natural frequency ω_n. Clearly, for underdamped situations (i.e., $\zeta < 1$), almost identical settling times can be observed for both phase

$$\phi_e^{\Delta\phi}(t) = \begin{cases} \frac{\Delta\phi}{\zeta-1}\left[\zeta e^{-\omega_n t} - e^{-\zeta\omega_n t}\cos(\omega_n t\sqrt{1-\zeta^2})\right], & \zeta < 1 \\ \Delta\phi e^{-\omega_n t}\left(1 + \omega_n t - \omega_n^2 t^2\right), & \zeta = 1 \\ \frac{\Delta\phi}{\zeta-1}\left[\zeta e^{-\omega_n t} - \frac{1}{2}e^{-(\zeta-\sqrt{\zeta^2-1})\omega_n t} - \frac{1}{2}e^{-(\zeta+\sqrt{\zeta^2-1})\omega_n t}\right], & \zeta > 1 \end{cases} \tag{31}$$

$$\phi_e^{\Delta\omega}(t) = \begin{cases} \frac{\Delta\omega}{(1-\zeta)\omega_n}\left[\zeta e^{-\omega_n t} + e^{-\zeta\omega_n t}\left\{-\zeta\cos(\omega_n t\sqrt{1-\zeta^2}) + \sqrt{1-\zeta^2}\sin(\omega_n t\sqrt{1-\zeta^2})\right\}\right], & \zeta < 1 \\ \frac{\Delta\omega}{\omega_n}e^{-\omega_n t}\left(\omega_n t + \omega_n^2 t^2\right), & \zeta = 1 \\ \frac{\Delta\omega}{(1-\zeta)\omega_n}\left[\zeta e^{-\omega_n t} - \frac{\zeta+\sqrt{\zeta^2-1}}{2}e^{-(\zeta-\sqrt{\zeta^2-1})\omega_n t} - \frac{\zeta-\sqrt{\zeta^2-1}}{2}e^{-(\zeta+\sqrt{\zeta^2-1})\omega_n t}\right], & \zeta > 1 \end{cases} \tag{32}$$

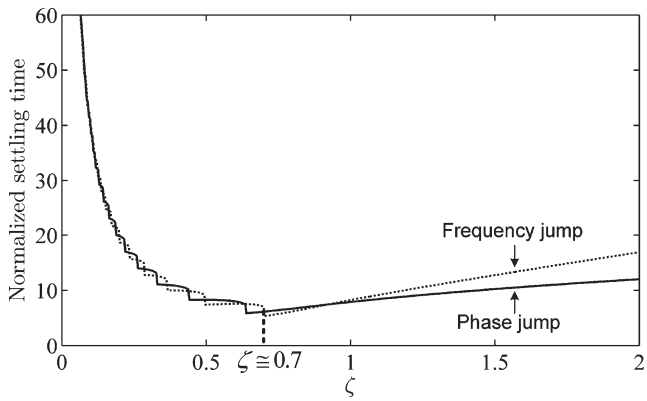

Fig. 10. Normalized simulated settling time as a function of ζ for both (solid line) phase jump and (dotted line) frequency jump.

and frequency jumps. However, for overdamped situations (i.e., $\zeta > 1$), a longer settling time is observed for the frequency jump. The minimum settling time for both phase and frequency jumps happens approximately at $\zeta = 0.7$. Thus, in terms of settling time, $\zeta = 0.7$ is optimum.

To make sure that $\zeta = 0.7$ is also a good choice in terms of stability, let us determine the PM for this value of ζ. Substituting $b = 2.4$ (which corresponds to $\zeta = 0.7$) into (24) gives

$$PM|_{b=2.4} = 44.76^\circ \tag{33}$$

which can be interpreted as a perfect stability.

C. Disturbance Rejection

The aim of this section is to select the natural frequency ω_n in such a way that a desired attenuation in all disturbance frequencies (i.e., $2\omega, 4\omega, 6\omega, \ldots$) is achieved.

Due to the low-pass filtering characteristics of the PLL, providing a sufficient attenuation at the lowest disturbance frequency (here, 2ω) guarantees a high attenuation at the rest of them. The proper attenuation at 2ω (which depends on the input voltage distortion level and also the application where the PLL is used) is selected to be 20 dB, in this paper.

From (16) and remembering that $D'(s) = D(s)/V$, the amplitude of the double-frequency disturbance input to the PLL linearized model can be obtained as

$$\begin{aligned} V_{d2} &= 2\frac{V_3}{V}\left|G_\beta(j3\omega)\right| = 2\frac{V_3}{V}\left|\frac{k\omega^2}{s^2+k\omega s+\omega^2}\right|_{s=j3\omega} \\ &= 2\frac{V_3}{V}\left|\frac{k}{-8+j3k}\right|. \end{aligned} \tag{34}$$

Substituting $k = 2/\tau_p\omega = 2b\omega_n/\omega$ into (34) gives

$$V_{d2} = \left|\frac{2b\omega_n}{-4\omega + j3b\omega_n}\right|\frac{V_3}{V}. \tag{35}$$

Once V_{d2} is determined, the next step is to derive the disturbance transfer function, relating the estimated phase $\hat{\phi}(s)$ to the disturbance input $D'(s)$. From Fig. 7, it can be simply obtained as follows:

$$G_d(s) = \left.\frac{\hat{\phi}(s)}{D'(s)}\right|_{\phi(s)=0} = \frac{(k_p s + k_i)(\tau_p s + 1)}{\tau_p s^3 + s^2 + k_p s + k_i}. \tag{36}$$

Substituting (22) and (23) into (36) and after some arrangements, the disturbance transfer function $G_d(s)$ can be rewritten as

$$G_d(s) = \omega_n \frac{(s+\omega_n/(2\zeta+1))\,(s+\omega_n(2\zeta+1))}{(s+\omega_n)\,(s^2+2\zeta\omega_n s+\omega_n^2)}. \tag{37}$$

Based on (35) and (37), the attenuation provided by the PLL at 2ω can be obtained as

$$Atten_{@2\omega} = \left|\frac{2b\omega_n}{-4\omega + j3b\omega_n}\right| \left|G_d(j2\omega)\right|. \tag{38}$$

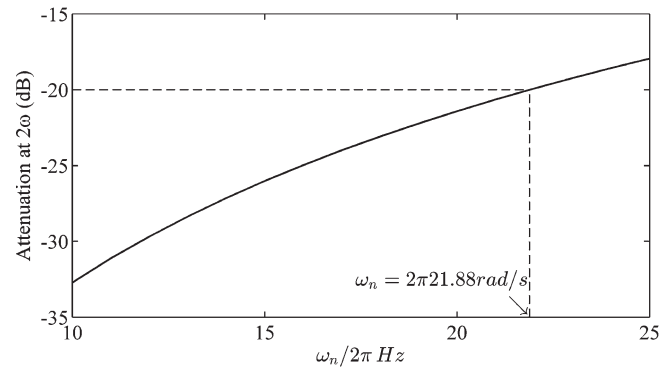

Fig. 11. PLL attenuation at 2ω as a function of ω_n.

Fig. 11 shows (38) as a function of ω_n for $\zeta = 0.7$ ($b = 2.4$). As highlighted, to achieve 20-dB attenuation at 2ω, we require that $\omega_n = 2\pi 21.88$ rad/s.

Considering that $b = 2.4$ and $\omega_c = 2\pi 21.88$ rad/s, the PLL parameters can be obtained as

$$\begin{cases} k_p = \omega_c = 137.5 \\ k_i = \frac{\omega_c^2}{b} = 7878 \\ \tau_p = \frac{1}{b\omega_c} = 3.03e-3 \text{ s.} \end{cases} \tag{39}$$

From the designed time constant τ_p, we can simply determine k and ω_p, as given in (40) and (41), respectively

$$k = \frac{2}{\tau_p \omega_{\text{ff}}} = 2.1 \tag{40}$$

$$\omega_p = \frac{2}{\tau_p} = 660 \text{ rad/s} = 105 \text{ Hz}. \tag{41}$$

One important issue that needs to be addressed here is the presence of a dc component in the input signal, which can be generated due to the digital quantization/rounding errors [36], [46], measurement devices [47], and temporary system faults [48]. Using a simple mathematical analysis, it can be shown that, in the presence of such a component, the loop suffers from a disturbance input at the fundamental frequency. In this

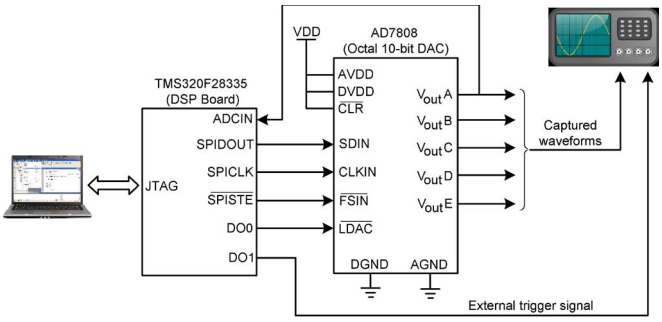

Fig. 12. Experimental setup.

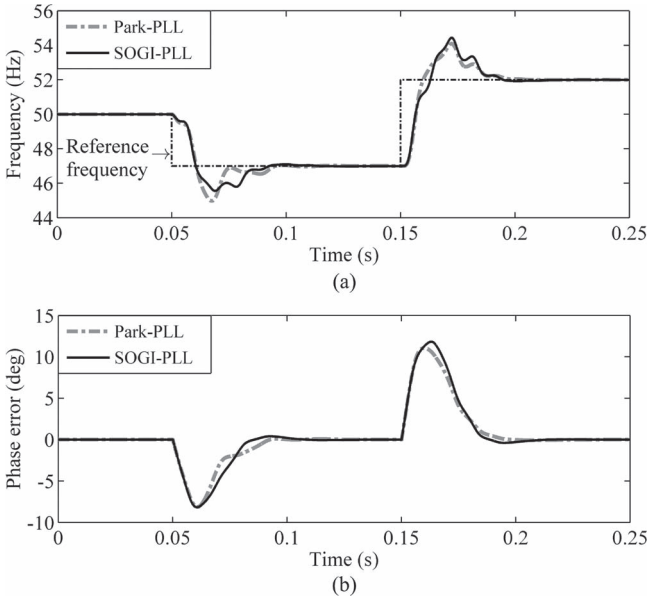

Fig. 13. Simulation results for SOGI-PLL and Park-PLL when the input voltage undergoes frequency step changes: (a) Estimated frequency and (b) phase error.

case, the previously suggested crossover frequency for PLLs may not be suitable. Here, one can simply consider the lowest disturbance frequency at the fundamental frequency and select ω_c in accordance with the required attenuation in this frequency. For example, providing an attenuation of 15 dB (or 20 dB) at the fundamental frequency requires a crossover frequency of 9.3 Hz (or 7 Hz). As one can see, at the presence of a dc component, it may be hard to meet a well-balanced tradeoff between the degree of dc rejection and system dynamics.

Some other techniques to deal with the problem of a dc component in the input signal can be found in [36], [46], [49], and [50].

V. Simulation and Experimental Results

In this section, the proposed design procedure has been evaluated through extensive simulations and experimental tests. Simulations are carried out in Matlab/Simulink environment, and experiments are based on a TMS320F28335 floating-point 150-MHz digital signal processor (DSP) from Texas Instruments. The sampling frequency has been fixed to 10 kHz, and the nominal frequency has been set to 50 Hz. To ensure the discrete accuracy, the trapezoidal method has been used for discretizing the continuous system.

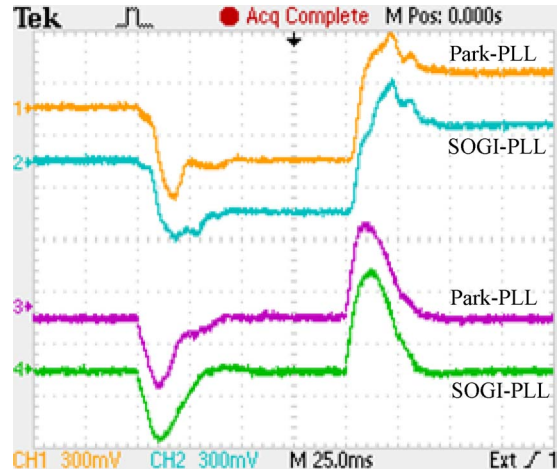

Fig. 14. Experimental results for SOGI-PLL and Park-PLL when the input voltage undergoes frequency step changes: Ch1 and Ch2 denote the estimated frequency (3 Hz/div), and Ch3 and Ch4 denote the phase error (6°/div).

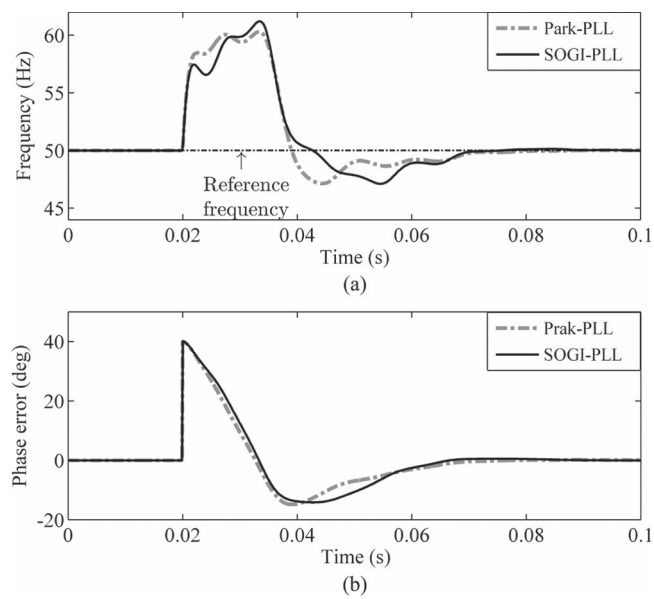

Fig. 15. Simulation results for SOGI-PLL and Park-PLL when the input voltage undergoes a phase jump of 40°: (a) Estimated frequency and (b) phase error.

The block diagram of the experimental setup is shown in Fig. 12. In experimental verifications, the desired input signal is generated internally in the DSP. It is then sent to the external digital-to-analog (D/A) converter AD7808 via the serial peripheral interface to generate the analog test signal. This waveform is then acquired by the DSP to perform the PLL algorithm. The selected waveforms are also sent to the octal D/A converter to be displayed by the digital oscilloscope.

A. Frequency Variation

Figs. 13 and 14 show the simulation and experimental results, respectively, for both Park-PLL and SOGI-PLL, when the input voltage undergoes frequency step changes (alternating between 47 and 52 Hz). A similar performance for both PLLs can be observed in simulated as well as experimental waveforms. The frequency settling time is about 45 ms, i.e., less than 2.5 cycles of the fundamental frequency.

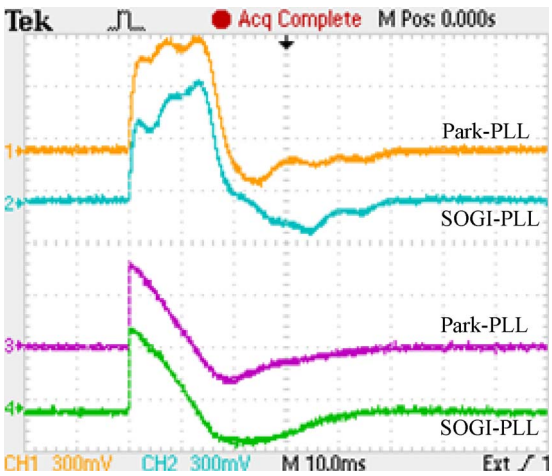

Fig. 16. Experimental results for SOGI-PLL and Park-PLL when the input voltage undergoes a phase jump of 40°: Ch1 and Ch2 denote the estimated frequency (5 Hz/div), and Ch3 and Ch4 denote the phase error (25°/div).

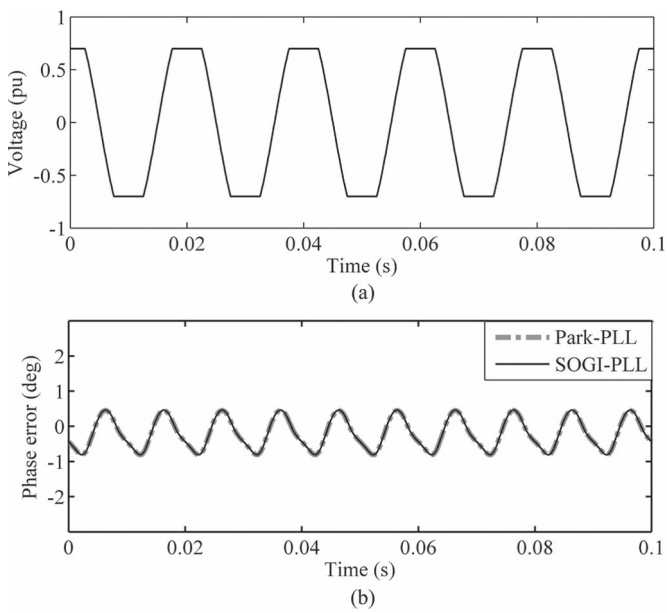

Fig. 17. Simulation results for SOGI-PLL and Park-PLL under distorted grid conditions: (a) Input voltage and (b) phase error.

B. Phase Jump

Figs. 15 and 16 show the simulation and experimental results, respectively, when the input voltage undergoes a phase jump of 40°. The responses obtained for the two PLLs are again close. The phase error decays to zero in about 47 ms (i.e., less than 2.5 cycles).

C. Harmonic Distortion

The performance of the two PLLs in distorted grid conditions is investigated in this section. A 70% clipped sine wave (13.76% total harmonic distortion) is considered as the input signal in this study. Figs. 17 and 18 show the steady-state simulated and experimental waveforms, respectively. It can be seen that the two PLLs exhibit well-matched responses in steady state. A peak-to-peak phase error of 1.3° is observed, which is because of the presence of harmonics in the input voltage.

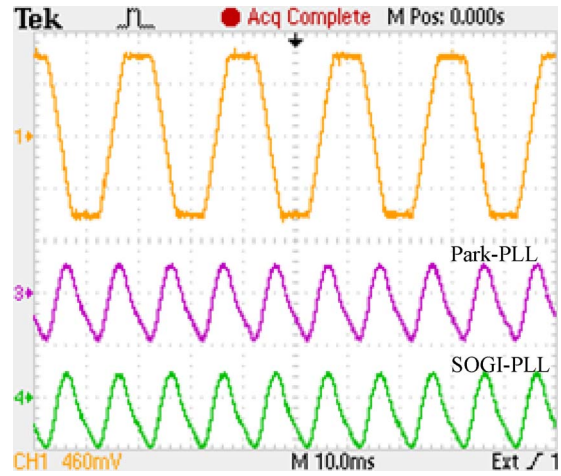

Fig. 18. Experimental results for SOGI-PLL and Park-PLL under distorted grid condition: Ch1 denotes the input voltage (460 mV/div), and Ch3 and Ch4 denote the phase error (1°/div).

VI. Conclusion

Two advanced single-phase PLL structures, known as Park-PLL and SOGI-PLL, have been deeply analyzed in this paper. Through a detailed mathematical analysis, it has been shown that these two PLLs are equivalent to each other, from the control point of view. Then, a linearized model for both PLLs has been developed. A systematic design approach for tuning of the PLL parameters has been proposed afterward, which provides a fast transient response, a high disturbance rejection capability, and a robust performance. Theoretical evaluations have been finally verified through extensive simulation and experimental studies.

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