Missouri University of Science and Technology
Scholars' Mine

Electrical and Computer Engineering Faculty Research & Creative Works

Electrical and Computer Engineering

01 Jul 2007

Early Time Charge Replenishment of the Power Delivery Network in Multi-Layer PCBs

Giuseppe Selli

Matteo Cocchini

James L. Knighten

Bruce Archambeault
Missouri University of Science and Technology, archamb@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1571

Follow this and additional works at: https://scholarsmine.mst.edu/ele_comeng_facwork

Part of the Electrical and Computer Engineering Commons

Recommended Citation

G. Selli et al., "Early Time Charge Replenishment of the Power Delivery Network in Multi-Layer PCBs," *IEEE International Symposium on Electromagnetic Compatibility (2007, Honolulu, HI)*, Institute of Electrical and Electronics Engineers (IEEE), Jul 2007.
The definitive version is available at https://doi.org/10.1109/ISEMC.2007.100

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

Early Time Charge Replenishment of the Power Delivery Network in Multi-Layer PCBs

G. Selli*, M. Cocchini*, J.L. Knighten***, B. Archambeault**, J. Fan***, S. R. Connor**, A. Orlandi****, J. L. Drewniak*

**University of Missouri-Rolla, Rolla, MO, USA*
***IBM Co., Research Triangle Park, NC, USA*
****NCR Co., San Diego, CA, USA*
*****University of L'Aquila, L'Aquila, Italy*

***Abstract*-The investigation of decoupling issues has been extensively treated in the literature in both the frequency and the time domain [1-9]. The two domains describe from different perspectives the same physical phenomenon, being related by a Fourier transform. In this article, well known decoupling issues usually addressed in the frequency domain [1,2] are discussed in the time domain. Moreover, some modeling issues related to the cavity model approach are discussed and, in particular, the circuit extraction feature associated with this methodology is utilized throughout the article to carry out the time domain simulations within a SPICE based-tool. The depletion of charges stored between the power bus is investigated in the time domain as a function of the plane thickness, SMT decoupling closeness and interconnect inductance values.**

Keywords – Decoupling Issues, Power Delivery Network, Charge Depletion, Cavity Model.

I. INTRODUCTION

Understanding decoupling issues in both the frequency and the time domain is important for effective design of the power distribution network for printed circuit boards (PCB) for high-speed signaling. Many contributions can be found in the literature [1-9] dealing with PDN decoupling aspects to ensure the functionality of PCB systems. Different schools of thoughts exist regarding the utilization of decoupling capacitors, typically in terms of a target impedance of the power/ground plane pair (power bus). The ability to perform circuit extraction when describing the power bus in terms of cavity modes [10-17] is used in this paper to investigate these issues mainly in the time domain by means of SPICE-based tools. Firstly, a couple of modeling problems are discussed in order to explain some intricacies associated with the circuit models and the choice of the observation points. Then, well known decoupling, issues that are usually addressed in the frequency domain, are investigated in the time domain. Design tips and conclusions drawn are consistent regardless of whether frequency or time domains are examined [1,2].

II. MODELING ISSUES AND IMPLEMENTATION

The circuit extraction feature of the cavity model approach [10-17] can be utilized to model the power delivery network. The circuit models extracted are run in a SPICE-based tool allowing for the possibility to investigate the same issues from a time domain prospective. The circuit interpretation of the cavity model approach is given below:

$$Z_{ij} = \frac{1}{j\omega C_p} + \sum_{n=0}^{N}\sum_{m=0}^{M} \frac{N_{nmi}N_{nmj}}{j\omega C_p + \frac{1}{j\omega L_{nm}} + G_{nm}}\Bigg|_{n=m\neq 0} + j\omega L_{ij}^{HM} \quad (1)$$

Equation (1) is divided into three terms. The first term corresponds to the interplane capacitance of the plane pair. It represents the impedance of the board at low frequencies, i.e., when the impedance declines at -20dB/dec. The third term is the higher order interconnect inductance. This term comprises all the contributions of the modes, whose resonant frequencies fall above the maximum frequency of interest. It is well-known that each resonant mode can described in terms of an equivalent R-L-C parallel circuit [11-14]. Hence, all the inductive contributions of those higher order modes are grouped together to create the inductive behavior. Also, this inductance resonates with the interplane capacitance creating the characteristic first dip seen in any self-impedance profile. If no additional terms were to be considered in the impedance formula, a characteristic impedance rise of 20 dB/dec would be observed in the self-impedance profile at higher frequencies. The second term of the summation consists of a double summation of all the resonant modes considered for the board geometry. The maximum number of those modes for each propagating direction is chosen according to the formulas provided in [12-13]. All these modes superimpose their characteristic R-L-C behavior on top of the underlying $j\omega L_{ij}$ behavior as the frequency is increased. Fig.1 illustrates the equivalent circuit realized by Equation (1).

1-4244-1350-8/07/$25.00 ©2007 IEEE

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.

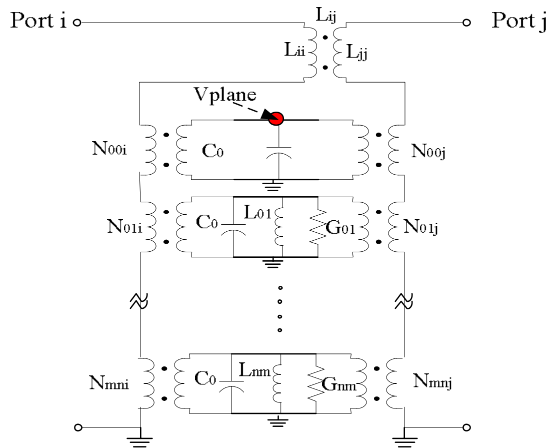

Fig.1. Equivalent circuit model corresponding to (1).

The original summation of Equation (1) consists of a double infinite summation, which is replaced by two finite N by M summations and the inductive term. The inductive term is obtained as the number which the double infinite summations converges, once the N by M terms - still explicitly present in the formulation (1) - are subtracted from it.

Further considerations need to be added regarding the investigation of decoupling issues in the time domain and in particular the charge depletion of the planes. As a repetitive triangular current waveform is drawn from a given location on the board, the sagging of the voltage is observed at the node specified in Fig.1 as Vplane. By placing a current source at Port i and leaving Port j open, the voltage observed at the driver port, or Port i, corresponds to the summation of all the voltage drops observed across the higher order mode inductance L_{ii}, the capacitance of the plane C_0 and all the R-L-C circuits associated with the resonant modes, coupled to the driver Port i by means of the ideal transformers N_{mni}. The quantity of interest is the voltage sag as a function of the charge depleted from the planes by the current drawn at the driver location, or Port i. Hence, the voltage, which is monitored and correlated to the amount of charge associated with the triangular current pulse, is the one specified in Fig.1 as Vplane. An alternative representation of the power delivery network, other than the equivalent circuit model shown in Fig.1, would not allow monitoring the voltage Vplane and relate its decrease the amount of charge depleted from the planes themselves.

The effectiveness of a decoupling capacitor is an important issue when designing a decoupled power bus. Often, effectiveness is defined as the ability to lower the power bus impedance. From studies in the frequency domain, this effectiveness is determined as a function of two frequency independent parameters [2,6], the coefficient of mutual coupling k and the ratio of the interconnect inductance above the plane over the interconnect inductance below the planes L_3/L_2. The coefficient of mutual coupling quantifies the amount of magnetic energy coupled between an IC-pin via and the connection via of a decoupling capacitor [2,6,8]. The farther away the capacitor via from the IC via, the lower the local decoupling effectiveness, the closer the k to zero. It is also desirable to have the ratio of the inductance above the plane over the inductance below the plane to be smaller than one when the mutual coupling coefficient is much larger than zero, in order to benefit from local decoupling effects [2,6]. This is usually achievable when the plane pair is thick, i.e., 35 mils plane spacing, and the interconnect inductance above the planes is minimized by choosing the decoupling capacitors with low ESL and properly designing the decoupling capacitor pads on the top or bottom sides of the PCB. Finally, the two frequency independent quantities can be grouped into the formula (2) [6], which quantifies the reduction, namely $|Z_{deacrease(dB)}|$, of the impedance.

$$\left|Z_{decrease(dB)}\right| = \left|20\log_{10}\left(\frac{(1-k)+\left(\frac{L_3}{L_2}\right)}{1+\left(\frac{L_3}{L_2}\right)}\right)\right| \quad (2)$$

III. Time Domain Behavior – Early Time

The equivalent circuit models extracted by means of the cavity model approach are used in this article to perform the investigation of power delivery issues as a function of various parameters such as decoupling capacitor distance and inductance above the planes. The inductance above the plane is varied in a range between 0.5nH and 3nH to observe the variations in the voltage noise excited between the power planes. On the other hand, the decoupling capacitor distance form Port 2, i.e., the point at which the current is drawn, is varied in a range between 50 mils to 5000 mils in order to observe the effects of the distance in reducing or increasing the power bus noise voltage.

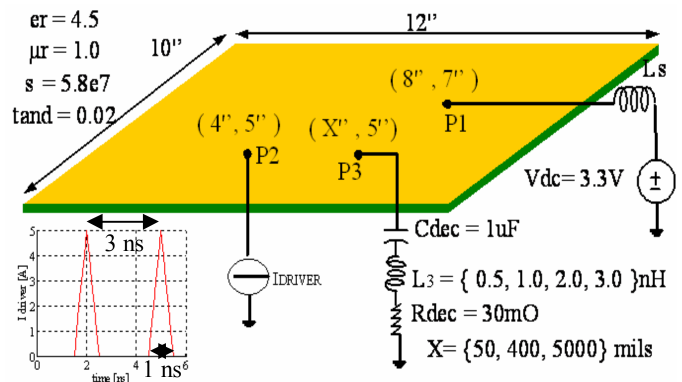

Fig.2. Geometry under test and triangular current waveform source connected at Port 2.

The two layer board of interest is shown in Fig.2. A constant DC voltage is connected at Port 1 through a interconnect inductance Ls of 50nH, a periodic triangular current waveform of 500ps rise time and 3 ns repetition , also shown in Fig.2, is hooked up at Port 2 in order to draw charges at a given rate

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.

and observe the PDN reaction to this disturbance. Also, a 1uF decoupling capacitor with 30Ω ESR and a variable L_3 is connected to Port 3, whose location is at a variable distance along the x direction from the driver, i.e., 50, 400, and 5000 mils. The peak value of the current waveform is chosen to be 5A so that every cycle approximately 20% of the overall plane charge is drawn from the driver. Finally, two values of plane separation are chosen, i.e., 35 and 10 mils.

A first comparison between the two aforementioned configurations is shown in Fig.3 and Fig.4. The current waveform of Fig.2 is applied at Port 2 and the interconnect inductance of the decoupling capacitor, located 400 mils away from the driver, is varied in the following range, i.e., 0.5nH, 1nH, 2nH, and 3nH.

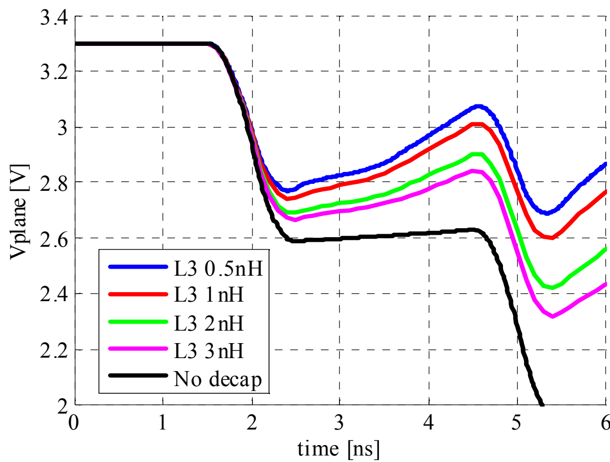

Fig.3. Configuration with 35 mils plane separation and decoupling capacitor 400 mils away from the driver.

It is important to observe that the time domain results agree with the frequency domain expectations [2,6] associated with the two configurations considered. The plane voltage reported in Fig.3 and Fig.4 is associated with the voltage across the plane capacitance, as indicated in Fig.1. By relating circuit models to the geometry, each point on the board would experience this voltage sag and each point would also have additional voltage terms associated with their positions with respect to the spatial variation of the resonant modes. Hence, the Vplane is the first order approximation of the voltage variation observed at any location. The reduction in the voltage sag observed in Fig.3 as a function of the decoupling capacitor interconnect inductance can be explained in terms of the impedance decrease formula given in Equation (2) [2,6,8]. Since the distance between the decoupling capacitor and the driver is constant for all the four different cases, the only variable in equation (2) is the ratio between the inductance above the plane L_3 and L_2 which is constant for all the cases. As the L_3 is increased becoming the dominant factor, the L_3/L_2 ratio also increases. Hence, the impedance-decrease factor is reduced or, the voltage swing is increased. This is true when examining results in the frequency domain, or in the time domain. The plane voltage sag lowers the plane voltage during the time when the current draw is increasing. During the time in which the current draw decreases, the plane voltage increases, but it doesn't return to the level at which it started, i.e., 3.3 V. Hence, when the second current pulse begins, the plane voltage sags again and later in the current cycle, when the current draw decreases, again, the voltage rises, but it cannot reach the value it had achieved after the first triangular pulse. This phenomenon reflects the physics of charge replenishment, or lack thereof in this case. The decoupling capacitor is not able to respond quick enough to meet the charge demand from the driver.

The negligible reduction in the voltage sag associated with the 10 mils configuration as a function of the decoupling interconnect inductance can also be explained in terms of Equation (2). The mutual coupling coefficient k is the same as the 35 mil case. However, the value of L_2 is 3.5 time smaller, hence the ratio of L_3/L_2 is 3.5 time larger, making this term the dominant one in equation (2).

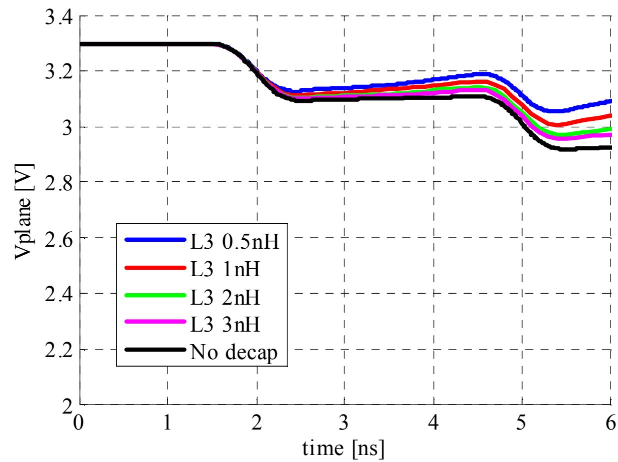

Fig.4. Configuration with 10 mils plane separation and decoupling capacitor 400 mils away from the driver.

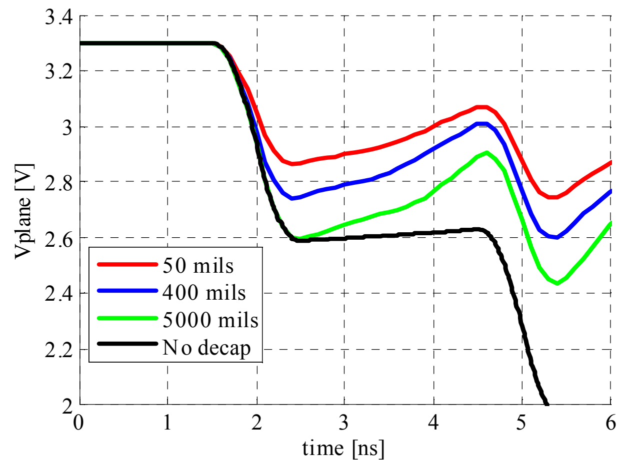

Fig.5. Plane separation 35 mils and 1nH decoupling capacitor interconnect inductance.

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.

The overall difference in the voltage swing observed when comparing the curves in Fig.3 and Fig.4 is also explained by considering that the interplane capacitance of the 10 mils case is also 3.5 larger than the interplane capacitance of the 35 mils case. Hence, the thin configuration is more effective in terms of decoupling by supporting the same amount of charge draw with a smaller voltage sag. Two additional comparisons of the decoupling capacitor effectiveness, as a function of the distance of the decoupling capacitor itself to the driver, are given in Fig.5 and Fig.6, for the 35 mils case and the 10 mil case, respectively. The reduction in the voltage sag in Fig.5 can be again explained in terms of Equation (2) [2,6,8]. As the decoupling capacitor is moved far away from the driver, the coupling coefficient k decreases, making Equation (2) in value close to one.

This effect is less important, hence the location of the decoupling capacitors with respect to the driver, is less important when considering thin parallel plane pair, as shown in Fig.6. As already mentioned in the previous paragraph, when reducing the plane separation from 35 mil down to 10 mil, the coupling coefficient is reduced of about 3.5 times and the plane capacitance is increased accordingly. Hence, the voltage swing is not significantly affected by the physics described in equation (2) and the overall voltage level is higher since the plane can provide the same amount of charges with a smaller voltage sag.

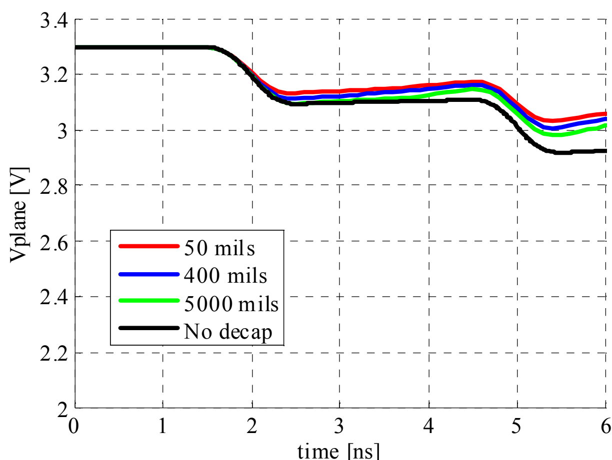

Fig.6. Plane separation 10 mils and 1nH decoupling capacitor interconnect inductance.

The values associated with the two frequency independent quantities constituting equation (2), i.e., the coupling coefficient k and the ratio of inductances L_3/L_2 are reported in Table 1, Table 2, Table 3 and Table 4 and for all the curves shown in Fig.3, Fig.4, Fig.5 and Fig.6. The value of the $|Z_{decrease}|$ is also shown in the two tables and it is possible to devise the correlation described in the previous paragraphs between the curves in the aforementioned plots and the values obtained from equation (2) [6].

Table 1. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Fig.3.

35 mils L_2 = 1.0nH & k = 0.38 @ 400 mil		
L_3 = 0.5nH	L_3/L_2 = 0.5	$\|Z_{decrease(dB)}\|$ = 2.62
L_3 = 1.0nH	L_3/L_2 = 1.0	$\|Z_{decrease(dB)}\|$ = 1.83
L_3 = 2.0nH	L_3/L_2 = 2.0	$\|Z_{decrease(dB)}\|$ = 1.21
L_3 = 3.0nH	L_3/L_2 = 3.0	$\|Z_{decrease(dB)}\|$ = 0.92

Table 2. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Fig.4.

10 mils L_2 = 0.28nH & k = 0.38 @ 400 mil		
L_3 = 0.5nH	L_3/L_2 = 1.78	$\|Z_{decrease(dB)}\|$ = 1.31
L_3 = 1.0nH	L_3/L_2 = 3.5	$\|Z_{decrease(dB)}\|$ = 0.82
L_3 = 2.0nH	L_3/L_2 = 7.1	$\|Z_{decrease(dB)}\|$ = 0.45
L_3 = 3.0nH	L_3/L_2 = 10	$\|Z_{decrease(dB)}\|$ = 0.25

Table 3. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Fig.5.

35 mils - L_3 = 1.0nH & L_2 = 1.0nH (~ same for all cases)			
50 mils	L_3/L_2 = 1.0	k = 0.74	$\|Z_{decrease(dB)}\|$ = 4.00
400 mils	L_3/L_2 = 1.0	k = 0.38	$\|Z_{decrease(dB)}\|$ = 1.83
5000 mils	L_3/L_2 = 1.0	k = 0.09	$\|Z_{decrease(dB)}\|$ = 0.45

Table 4. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Fig.6.

10 mils - L_3 = 1.0nH & L_2 = 0.28nH (~ same for all cases)			
50 mils	L_3/L_2 = 3.5	k = 0.74	$\|Z_{decrease(dB)}\|$ = 1.51
400 mils	L_3/L_2 = 3.5	k = 0.38	$\|Z_{decrease(dB)}\|$ = 0.82
5000 mils	L_3/L_2 = 3.5	k = 0.09	$\|Z_{decrease(dB)}\|$ = 0.18

Four additional comparisons are finally presented in Fig.7 and Fig.8 in the timed domain and in Fig.9 and Fig.10and in the frequency domain. A 400 mils radius ring of eight capacitors centered around the driver is compared against a single capacitor, 8 times larger also 400 mils away from the driver along one direction.

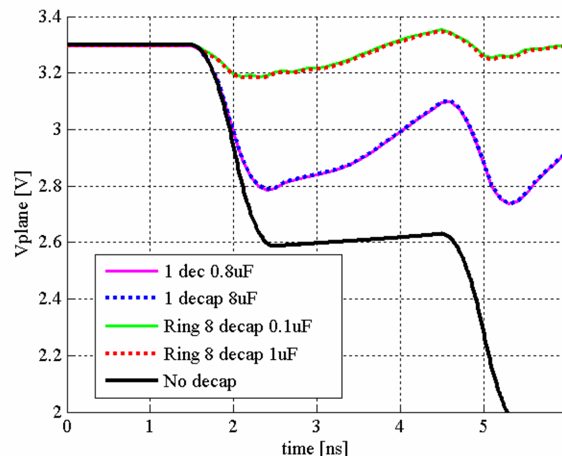

Fig.7. Early instants of time comparison between a ring of eight 0.1uF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8uF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5nH and ESR 30mΩ) and a ring of eight 1uF decoupling capacitor 400 mils away from the driver *vs.* single 8uF decoupling capacitor at 400 mils away from the driver for a 35 mil plane separation (L_3 = 0.5nH and ESR 30mΩ).

The conclusions to be drawn when comparing each set of curves within each plot is that the ring of decoupling capacitor

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.

acts by improving the speed of charge delivery from the capacitors themselves to the plane, where the voltage across the plane starts sagging. It is also seen, by comparing Fig.7 and Fig.8, that the value of decoupling capacitor is not important in the very early instants of time during the plane charge depletion. An array of decoupling capacitors, presenting a lower interconnect inductance, is superior to a single capacitor of much greater value.

There is a definitive improvement when compared with the case of no decoupling, but also the improvement with respect to the single capacitor is remarkable and it amount to approximately 400mV in the case of 35 mils. The smaller voltage swing associated with the 10 mil cases is again explained by considering that the interplane capacitance is 3.5 times higher.

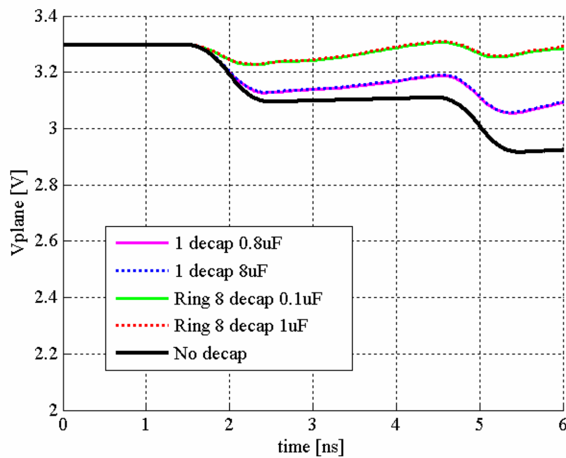

Fig.8. Early instants of time comparison between a ring of eight 0.1uF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8uF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5nH and ESR 30mΩ) and a ring of eight 1uF decoupling capacitor 400 mils away from the driver *vs.* a single 8uF decoupling capacitor at 400 mils away from the driver for 10 mil plane separation (L_3 = 0.5nH and ESR 30mΩ).

This rationale is also confirmed by looking at the frequency domain plots given Fig.9 and Fig.10 corresponding to the time domain graphs of Fig.7 and Fig.8, respectively. First of all, the self-impedance observed across the driver port, when the plane separation is 35 mils, is approximately 10 dB higher with respect to the 10 mils case above approximately 50 MHz. This improvement is well documented in the literature [1-9] and also confirmed by the timed domain simulations presented in the previous paragraph. Also, above 20-30 MHz, both graphs confirm the greater importance of the interconnect inductance over the values of the decoupling capacitance utilized. The two ring configurations as well as the single decoupling configurations exhibit the same frequency domain behavior, respectively, in both the 35 mils case and the 10 mil case.

It is important to note that different nodes are monitored when the pair of curves given in Fig.7 and Fig.8 and the pair of curves shown in Fig.9 and Fig.10 are obtained. In fact, the time domain curves were observed at the node Vplane shown in Fig.1. This node provides a first order approximation of the plane voltage noise and it is not affected by the $L_{ii}di/dt$ voltage drop, which is large compared to the one across the plane in the configuration of Fig.2. On the other hand, the input impedance plots were both observed from Port 2, or the driver port, hence the port inductance is considered and it prevails at higher frequencies. This is the reason why the self impedance in both the cases of the ring of decoupling capacitors and the single decoupling capacitor exhibits the same impedance behavior above 100 MHz, while the plots of early instants of time show significant differences. The difference between the ring and the single capacitors is more visible in the range between 10 MHz and approximately 100 MHz, where the effect of the interconnect inductance of the decoupling capacitors play a role in reducing the plane impedance.

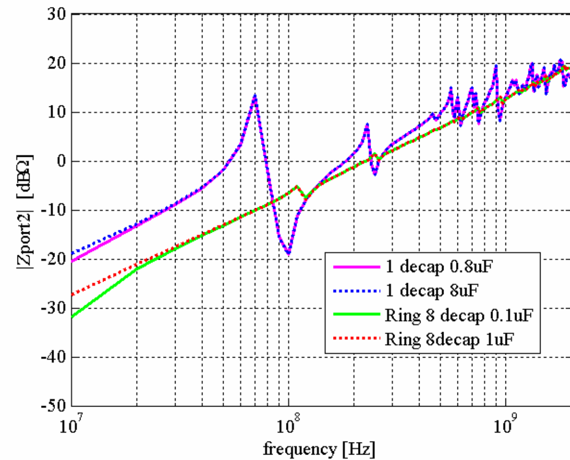

Fig.9. Frequency domain comparison between a ring of eight 0.1uF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8uF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5nH and ESR 30mΩ) and a ring of eight 1uF decoupling capacitor 400 mils away from the driver *vs.* single 8uF decoupling capacitor at 400 mils away from the driver for a 35 mil plane separation (L_3 = 0.5nH and ESR 30mΩ).

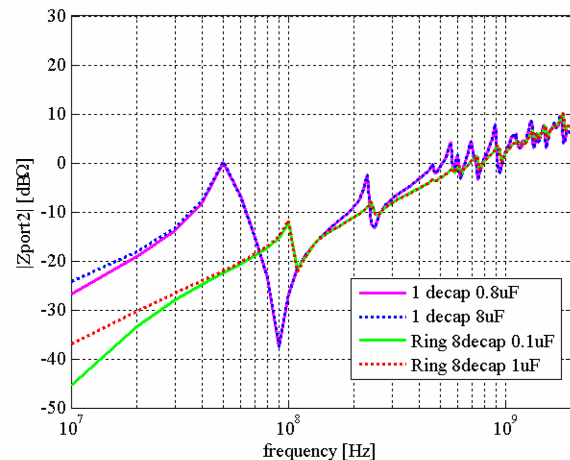

Fig.10. Frequency domain comparison between a ring of eight 0.1uF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8uF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5nH and ESR 30mΩ) and a ring of eight 1uF decoupling capacitor 400 mils away from the driver *vs.* a single 8uF decoupling capacitor at 400 mils away from the driver for 10 mil plane separation (L_3 = 0.5nH and ESR 30mΩ).

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.

IV. CONCLUSIONS

Modeling problems issues, as well as, some important design issues are in this paper. In particular, it is been shown the importance of the higher order mode self and mutual inductances, which are crucial parameters to represent correctly when dealing with decoupling issues. A reduction in the impedance, in the frequency domain, or a reduction in the voltage swing, in the time domain can be achieved for some PDN designs by placing the decoupling capacitors close to the drivers and minimizing their interconnect inductance. The PDN associated with thin power planes, i.e., 10 mil and below, are not significantly affected by the decoupling placement as shown in the time domain plots given in the previous paragraph. It is very interesting to note that the value of the decoupling capacitors themselves do not make a difference in the early instants of time. In this time frame, it is of more importance achieving a configuration with a low parasitic interconnect inductance rather than increasing the value of decoupling capacitors.

V. REFERENCES

[1] Knighten, James L., Bruce Archambeault, Jun Fan, Samuel Connor, James L. Drewniak, "PDN design strategies: I. Ceramic SMT decoupling capacitors – what values should I choose?," *IEEE EMC Society Newsletter*, Issue No. 207, Fall 2005, pp. 34-41.

[2] Knighten, James L., Bruce Archambeault, Jun Fan, Giuseppe Selli, Liang Xue, Samuel Connor, and James L. Drewniak, "PDN design strategies : I. Ceramic SMT decoupling capacitors – does location matter ?," *IEEE EMC Society Newsletter*, Issue No. 208, Winter 2006, pp. 56-67.

[3] L. Smith, R.E. Anderson, D.W. Forehand, T.J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transaction on Advanced Packaging*, Vol. 22, No. 3, August 1999, pp. 284-291.

[4] L. Smith, "Decoupling capacitor calculations for CMOS circuits," *Proceedings of Electrical Performance of Electronic Packages (EPEP), Monterey*, CA, November 1994.

[5] J.L.Drewniak, B.Archambeault, J.L.Knighten, G.Selli, J.Fan, M.Cocchini, S. Connor, and L.Xue, "Comparing Time-Domain and Frequency Domain Techniques for Investigation on Charge Delivery and Power-Bus Noise for High-Speed Printed Circuit Boards," *Accepted for Publication on Proceedings of Design Conference East,* CA, Feb. 2007.

[6] Fan, Jun, James L. Drewniak, James. L. Knighten, Norman W. Smith, and Antonio Orlandi, Thomas P. Van Doren, Todd H. Hubing, and Richard E. DuBroff "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multi-Layer PCBs," *IEEE Trans. of Electromagnetic Compatibility*, Vol. 43, No. 4, November 2001, pp. 588-599.

[7] Fan, Jun, Wei Cui, James L. Drewniak, Thomas Van Doren, and James L. Knighten, "Estimating the Noise Mitigating Effect of Local Decoupling in Printed Circuit Boards," *IEEE Transactions on Advanced Packaging,* Vol. 25, No. 2, May 2002, pp. 154-165.

[8] Jun Fan, James L. Knighten, Lin Zhang, Giuseppe Selli, Jingkun Mao, Bruce Archambeault, Richard E. DuBroff, and James L. Drewniak, "An investigation of the importance of decoupling capacitor values in high-speed digital PCBs," *IMAPS Advanced Technology Workshop on High-Speed Interconnect, EMC and Power Aspects of System Packaging for High-Performance Computing, Telecom and Semiconductor Capital Equipment*, Palo Alto, CA, October 2003.

[9] Archambeault, B., Juan Wang, and Samuel Connor, "Power and Ground-Reference Plane Impedance Determination As Decoupling Capacitor Distance Increases," *IEEE International Symposium on Electromagnetic Compatibility*, August 2003, pp. 875-880.

[10] Y. Lo, D. Solomon, W. Richards, "Theory and experiment on microstrip antennas," *IEEE Trans. Antennas and Propagation*, vol. 27, pp. 137-145, March 1979.

[11] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*, Springer-Verlag Berlin Heidelberg, 1985.

[12] G.T. Lei, R.W. Techentin, R.P. Hayes, D.J. Schwab, and B.K.Gilbert," Wave model to the Ground/Power Plane Noise Problem," *IEEE Transactions on Instrumentations and Measurements,* Vol.44, No.2, April 1995, pp. 300-303.

[13] G.T. Lei, R.W. Techentin, and B.K.Gilbert,"High-frequency characterization of power/ground-planes structures" *IEEE Transactions on microwave Theory and Technique,* Vol.47, No.5, May 1999, pp. 562-569.

[14] C. Wang, J. Mao, G. Selli, S. Luan, L. Zhang, J. Fan, D.J. Pommerenke, R.E. Dubroff, and J.L. Drewniak, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductance,", *IEEE Transactions on Advanced Packaging,* Vol. 29, No.2.

[15] G. Selli, J.L. Drewniak, L. Xue, J.L. Knighten, J. Fan, B. Archambeault, S. Connor, and C. Wang, "Modeling and design of embedded capacitances for power distribution networks on multilayer printed circuit board," *Proceedings of Design Conference East,* CA, Feb. 2006.

[16] G. Selli, L. Xue, J.L. Drewniak, B. Archambeault, J.Fan, S. Connor and J.L. Knighten "Power delivery effectiveness of multiple power plane pair configuration printed circuit board" *IMAPS Advanced Technology Workshop on High-Speed Interconnect, EMC and Power Aspects of System Packaging for High-Performance Computing, Telecom and Semiconductor Capital Equipment*, San Diego, CA, October 2006

[17] J. Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN Design Strategies: III. Planes and Materials – Are they Important Factors in Power Bus Design?," *IEEE EMC Society Newsletter*, Issue No. 208, Winter 2006, pp. 56-67.

Authorized licensed use limited to: University of Missouri. Downloaded on January 16, 2009 at 15:37 from IEEE Xplore. Restrictions apply.