

EDA for IC Implementation, Circuit Design, and Process Technology

Edited by

Louis Scheffer

Cadence Design Systems
San Jose, California, U.S.A.

Luciano Lavagno

Cadence Berkeley Laboratories
Berkeley, California, U.S.A.

Grant Martin

Tensilica Inc.
Santa Clara, California, U.S.A.



Taylor & Francis

Taylor & Francis Group

Boca Raton London New York

A CRC title, part of the Taylor & Francis imprint, a member of the
Taylor & Francis Group, the academic division of T&F Informa plc.

Contents

SECTION I RTL to GDS-II, or Synthesis, Place, and Route

1 Design Flows

<i>Leon Stok, David Hathaway, Kurt Keutzer, and David Chinnery</i>	1-1
1.1 Introduction	1-1
1.2 Invention	1-2
1.3 Implementation	1-2
1.4 Integration	1-5
1.5 Future Scaling Challenges	1-10
1.6 Conclusion	1-12

2 Logic Synthesis

<i>Sunil P. Khatri and Narendra V. Shenoy</i>	2-1
2.1 Introduction	2-1
2.2 Behavioral and Register Transfer-Level Synthesis	2-2
2.3 Two-Level Minimization	2-3
2.4 Multilevel Logic Minimization	2-4
2.5 Enabling Technologies for Logic Synthesis	2-10
2.6 Sequential Optimization	2-11
2.7 Physical Synthesis	2-13
2.8 Multivalued Logic Synthesis	2-14
2.9 Summary	2-15

3 Power Analysis and Optimization from Circuit to Register-Transfer Levels

<i>Jose Monteiro, Rakesh Patel, and Vivek Tiwari</i>	3-1
3.1 Introduction	3-1
3.2 Power Analysis	3-2
3.3 Circuit-Level Power Optimization	3-8
3.4 Logic Synthesis for Low Power	3-12
3.5 Conclusion	3-15

4	Equivalence Checking	
	<i>Andreas Kuehlmann and Fabio Somenzi</i>	4-1
4.1	Introduction	4-1
4.2	Equivalence Checking Problem	4-3
4.3	Boolean Reasoning	4-5
4.4	Combinational Equivalence Checking	4-10
4.5	Sequential Equivalence Checking	4-14
4.6	Summary	4-17
5	Digital Layout — Placement	
	<i>Andrew B. Kahng and Sherief Reda</i>	5-1
5.1	Introduction: Placement Problem and Contexts	5-1
5.2	Global Placement	5-4
5.3	Detailed Placement and Legalizers	5-15
5.4	Placement Trends	5-17
5.5	Academic and Industrial Placers	5-19
5.6	Conclusions	5-20
6	Static Timing Analysis	
	<i>Sachin S. Sapatnekar</i>	6-1
6.1	Introduction	6-1
6.2	Representation of Combinational and Sequential Circuits	6-1
6.3	Gate Delay Models	6-3
6.4	Timing Analysis for Combinational Circuits	6-3
6.5	Timing Analysis for Sequential Circuits	6-7
6.6	Clocking Disciplines: Edge-Triggered Circuits	6-8
6.7	Clocking and Clock-Skew Optimization	6-9
6.8	Statistical Static Timing Analysis	6-12
6.9	Conclusion	6-15
7	Structured Digital Design	
	<i>Fan Mo and Robert K. Brayton</i>	7-1
7.1	Introduction	7-1
7.2	Datapaths	7-2
7.3	Programmable Logic Arrays	7-13
7.4	Memory and Register Files	7-15
7.5	Structured Chip Design	7-17
7.6	Summary	7-21
8	Routing	
	<i>Louis Scheffer</i>	8-1
8.1	Introduction	8-2
8.2	Types of Routers	8-2
8.3	A Brief History of Routing	8-4
8.4	Common Routing Algorithms	8-5
8.5	Additional Router Considerations	8-9
9	Exploring Challenges of Libraries for Electronic Design	
	<i>James Hogan and Scott T. Becker</i>	9-1
9.1	Introduction	9-1
9.2	What Does It Mean to Design Libraries?	9-1

9.3	How Did We Get Here, Anyway?	9-2
9.4	Commercial Efforts	9-5
9.5	What Makes the Effort Easier?	9-5
9.6	The Enemies of Progress	9-6
9.7	Environments That Drive Progress	9-6
9.8	Libraries and What They Contain	9-6
9.9	Summary	9-7
10	Design Closure	
	<i>Peter J. Osler and John M. Cohn</i>	10-1
10.1	Introduction	10-1
10.2	Current Practice	10-13
10.3	The Future of Design Closure	10-28
10.4	Conclusion	10-30
11	Tools for Chip-Package Codesign	
	<i>Paul D. Franzon</i>	11-1
11.1	Introduction	11-1
11.2	Drivers for Chip-Package Codesign	11-1
11.3	Digital System Codesign Issues	11-2
11.4	Mixed-Signal Codesign Issues	11-5
11.5	I/O Buffer Interface Standard and Other Macromodels	11-5
11.6	Conclusions	11-7
12	Design Databases	
	<i>Mark Bales</i>	12-1
12.1	Introduction	12-1
12.2	History	12-2
12.3	Modern Database Examples	12-3
12.4	Fundamental Features	12-4
12.5	Advanced Features	12-9
12.6	Technology Data	12-12
12.7	Library Data and Structures: Design-Data Management	12-13
12.8	Interoperability Models	12-13
13	FPGA Synthesis and Physical Design	
	<i>Mike Hutton and Vaughn Betz</i>	13-1
13.1	Introduction	13-1
13.2	System-Level Tools	13-6
13.3	Logic Synthesis	13-6
13.4	Physical Design	13-13
13.5	Looking Forward	13-26

SECTION II Analog and Mixed-Signal Design

14	Simulation of Analog and RF Circuits and Systems	
	<i>Jaijeet Roychowdhury and Alan Mantooth</i>	14-1
14.1	Introduction	14-1
14.2	Differential-Algebraic Equations for Circuits via Modified Nodal Analysis	14-2

14.3	Device Models	14-4
14.4	Basic Circuit Simulation: DC Analysis	14-10
14.5	Steady-State Analysis	14-13
14.6	Multitime Analysis	14-17
14.7	Noise in RF Design	14-25
14.8	Conclusions	14-35
15	Simulation and Modeling for Analog and Mixed-Signal Integrated Circuits	
	<i>Georges G.E. Gielen and Joel R. Phillips</i>	15-1
15.1	Introduction	15-2
15.2	Top-Down Mixed-Signal Design Methodology	15-2
15.3	Mixed-Signal and Behavioral Simulation	15-8
15.4	Analog Behavioral and Power Model Generation Techniques	15-14
15.5	Symbolic Analysis of Analog Circuits	15-18
15.6	Conclusions	15-20
16	Layout Tools for Analog Integrated Circuits and Mixed-Signal Systems-on-Chip: A Survey	
	<i>Rob A. Rutenbar and John M. Cohn</i>	16-1
16.1	Introduction	16-1
16.2	Analog Layout Problems and Approaches	16-2
16.3	Analog Cell Layout Strategies	16-5
16.4	Mixed-Signal System Layout	16-8
16.5	Field-Programmable Analog Arrays	16-11
16.6	Conclusions	16-11

SECTION III Physical Verification

17	Design Rule Checking	
	<i>Robert Todd, Laurence Grodd, and Katherine Fetty</i>	17-1
17.1	Introduction	17-1
17.2	Geometric Algorithms for Physical Verification	17-6
17.3	Hierarchical Data Structures	17-7
17.4	Time Complexity of Hierarchical Analysis	17-8
17.5	Connectivity Models	17-9
17.6	Parallel Computing	17-11
17.7	Future Roles for Verification	17-11
18	Resolution Enhancement Techniques and Mask Data Preparation	
	<i>Franklin M. Schellenberg</i>	18-1
18.1	Introduction	18-1
18.2	Lithographic Effects	18-2
18.3	RET for Smaller k_1	18-5
18.4	Software Implementations of RET Solutions	18-11
18.5	Mask Data Preparation	18-24
18.6	Summary	18-27
19	Design for Manufacturability in the Nanometer Era	
	<i>Nicola Dragone, Carlo Guardiani, and Andrzej J. Strojwas</i>	19-1
19.1	Introduction	19-1
19.2	Taxonomy of Yield Loss Mechanisms	19-3

19.3	Logic Design for Manufacturing	19-6
19.4	Parametric Design for Manufacturing Methodologies	19-13
19.5	Design for Manufacturing Integration in the Design Flow: Yield-Aware Physical Synthesis	19-18
19.6	Summary	19-20
20	Design and Analysis of Power Supply Networks	
	<i>David Blaauw, Sanjay Pant, Rajat Chaudhry, and Rajendran Panda</i>	20-1
20.1	Introduction	20-1
20.2	Voltage-Drop Analysis Modes	20-3
20.3	Linear System Solution Techniques	20-5
20.4	Models for Power Distribution Networks	20-8
20.5	Conclusions	20-13
21	Noise Considerations in Digital ICs	
	<i>Vinod Kariat</i>	21-1
21.1	Introduction	21-1
21.2	Why Has Noise Become a Problem for Digital Chips?	21-2
21.3	Noise Effects in Digital Designs	21-3
21.4	Static Noise Analysis	21-7
21.5	Electrical Analysis	21-14
21.6	Fixing Noise Problems	21-18
21.7	Summary and Conclusions	21-20
22	Layout Extraction	
	<i>William Kao, Chi-Yuan Lo, Mark Basel, Raminderpal Singh, Peter Spink, and Louis Scheffer</i>	22-1
22.1	Introduction	22-1
22.2	Early History	22-2
22.3	Problem Analysis	22-2
22.4	System Capabilities	22-3
22.5	Converting Drawn Geometries to Actual Geometries	22-4
22.6	Designed Device Extraction	22-5
22.7	Connectivity Extraction	22-7
22.8	Parasitic Resistance Extraction	22-8
22.9	Capacitance Extraction Techniques	22-10
22.10	Inductance Extraction Techniques	22-13
22.11	Network Reduction	22-17
22.12	Process Variation	22-18
22.13	Conclusions and Future Study	22-19
23	Mixed-Signal Noise Coupling in System-on-Chip Design: Modeling, Analysis, and Validation	
	<i>Nishath Verghese and Makoto Nagata</i>	23-1
23.1	Introduction	23-2
23.2	Mechanisms and Effects of Mixed-Signal Noise Coupling	23-2
23.3	Modeling of Mixed-Signal Noise Coupling	23-7
23.4	Mixed-Signal Noise Measurement and Validation	23-18
23.5	Application to Placement and Power Distribution Synthesis	23-19
23.6	Summary	23-21

SECTION IV Technology CAD

24	Process Simulation	
	<i>Mark D. Johnson</i>	24-1
24.1	Introduction	24-1
24.2	Process Simulation Methods	24-2
24.3	Ion Implantation	24-3
24.4	Diffusion	24-8
24.5	Oxidation	24-12
24.6	Etch and Deposition	24-13
24.7	Lithography and Photoresist Modeling	24-20
24.8	Silicidation	24-20
24.9	Mechanics Modeling	24-20
24.10	Putting It All Together	24-22
24.11	Conclusions	24-23
25	Device Modeling —From Physics to Electrical Parameter Extraction	
	<i>Robert W. Dutton, Chang-Hoon Choi, and Edwin C. Kan</i>	25-1
25.1	Introduction	25-1
25.2	MOS Technology and Intrinsic Device Modeling	25-3
25.3	Parasitic Junction and Inhomogeneous Substrate Effects	25-20
25.4	Device Technology Alternatives	25-23
25.5	Conclusions	25-26
26	High-Accuracy Parasitic Extraction	
	<i>Mattan Kamon and Ralph Iverson</i>	26-1
26.1	Introduction	26-2
Part I:	Extraction via Fast Integral Equation Methods	26-3
26.2	Introduction	26-3
26.3	Forms of Maxwell's Equations	26-3
26.4	Fast Field Solvers: Capacitance Solution	26-5
26.5	Fast Inductance Solution	26-7
26.6	Distributed RLC and Full Wave	26-11
26.7	Conclusions	26-14
Part II:	Statistical Capacitance Extraction	26-14
26.8	Introduction	26-14
26.9	Theory	26-15
26.10	Characteristics	26-17
26.11	Summary	26-22
Index		Index-1