EDA for IC System Design, Verification, and Testing

Edited by

Louis Scheffer

Cadence Design Systems San Jose, California, U.S.A.

Luciano Lavagno

Cadence Berkeley Laboratories Berkeley, California, U.S.A.

Grant Martin

Tensilica Inc. Santa Clara, California, U.S.A.



A CRC title, part of the Taylor & Francis imprint, a member of the Taylor & Francis Group, the academic division of T&F Informa plc.

Contents

SECTION I Introduction

Overview
Luciano Lavagno, Grant Martin, and Louis Scheffer1-1
Introduction to Electronic Design Automation for Integrated Circuits
System Level Design
Micro-Architecture Design
Logical Verification
Test
RTL to GDS-II, or Synthesis, Place, and Route
Analog and Mixed-Signal Design1-11
Physical Verification
Technology Computer-Aided Design1-12
The Integrated Circuit Design Process and Electronic Design Automation
Robert Damiano and Raul Camposano2-1
2.1 Introduction
2.2 Verification
2.3 Implementation
2.4 Design for Manufacturing

SECTION II System Level Design

Too	ls and Methodologies for System-Level Design	
Shu	vra Bhattacharyya and Wayne Wolf	3-1
3.2	Characteristics of Video Applications	3-2
3.3	Other Application Domains	3 -3
3.4	Platform Characteristics	3 -3
	Shur 3.1 3.2 3.3	Tools and Methodologies for System-Level DesignShuvra Bhattacharyya and Wayne Wolf.3.1 Introduction3.2 Characteristics of Video Applications3.3 Other Application Domains3.4 Platform Characteristics

	3.5 3.6 3.7 3.8	Models of Computation and Tools for Model-Based Design.3-6Simulation.3-13Hardware/Software Cosynthesis.3-14Summary.3-15
4	Syst Josep 4.1 4.2 4.3 4.4	tem-Level Specification and Modeling Languages <i>bh T. Buck</i>
5		C Block-Based Design and IP AssemblyWilsonThe Economics of Reusable IP and Block-Based Design5-2Standard Bus Interfaces5-3Use of Assertion-Based Verification5-4Use of IP Configurators and Generators5-5The Design Assembly and Verification Challenge5-7The SPIRIT XML Databook Initiative5-8Conclusions5-10
6	Pert Ahm 6.1 6.2 6.3 6.4	formance Evaluation Methods for Multiprocessor System-on-Chip Design <i>ted Jerraya and Iuliana Bacivarov</i>
7		tem-Level Power Management <i>nyuck Chang, Enrico Macii, Massimo Poncino, and Vivek Tiwari</i>
8		cessor Modeling and Design Toolshat Mishra and Nikil DuttIntroductionProcessor Modeling Using ADLsADL-Driven Methodologies8-11Conclusions8-18
9		bedded Software Modeling and Design <i>to Di Natale</i>

	9.5	Research on Models for Embedded Software
	9.6	Conclusions
10	Usi	ng Performance Metrics to Select Microprocessor Cores for IC Designs
	Stev	2 Leibson
	10.1	Introduction
	10.2	The ISS as Benchmarking Platform 10-3
	10.3	Ideal Versus Practical Processor Benchmarks 10-4
	10.4	Standard Benchmark Types10-4
	10.5	Prehistoric Performance Ratings: MIPS, MOPS, and MFLOPS 10-5
	10.6	Classic Processor Benchmarks (The Stone Age) 10-6
	10.7	Modern Processor Performance Benchmarks10-13
	10.8	Configurable Processors and the Future of Processor-Core Benchmarks
	10.9	Conclusion
11	Par	allelizing High-Level Synthesis: A Code Transformational Approach
		High-Level Synthesis
	101	ingli Devel Gyntheolo

Gauri	av Singh, Sumit Gupta, Sandeep Shukla, and Rajesh Gupta	-1
11.1	Introduction	-2
11.2	Background and Survey of the State of the Art11-	-3
11.3	Parallelizing HLS	1
11.4	The SPARK PHLS Framework	5
11.5	Summary	.6

SECTION III Micro-Architecture Design

12	Cycle-Accurate System-Level Modeling and Performance Evaluation		
	Marc	ello Coppola and Miltos D. Grammatikakis	
	12.1	Introduction	
	12.2	System Modeling and Design Methodology 12-3	
	12.3	Back-Annotation of System-Level Modeling Objects	
	12.4	Automatic Extraction of Statistical Features	
	12.5	Open System-Level Modeling Issues 12-16	
13	Mic	ro-Architectural Power Estimation and Optimization	
		o Macii, Renu Mehra, and Massimo Poncino1	
	13.1	Introduction	
	13.2	Background	
	13.3	Architectural Template	
	13.4	Micro-Architectural Power Modeling and Estimation	
	13.5	Micro-Architectural Power Optimization	
	13.6	Conclusions	
14	Desi	gn Planning	
		14-1 14 -1	
	14.1	Introduction	
	14.2	Floorplans	
	14.2	•	
		Wireplans	
	14.4	A Formal System For Trade-Offs 14-17	

SECTION IV Logical Verification

15	Design and Verification Languages	
	Stephen A. Edwards1	5-1
	15.1 Introduction	5-1
	15.2 History	5-2
	15.3 Design Languages1	5-3
	15.4 Verification Languages15	-16
	15.5 Conclusions	
16	Digital Simulation	
	John Sanguinetti	
	16.1 Introduction	
	16.2 Event- vs. Process-Oriented Simulation1	
	16.3 Logic Simulation Methods and Algorithms	
	16.4 Impact of Languages on Logic Simulation16	
	16.5 Logic Simulation Techniques16	
	16.6 Impact of HVLs on Simulation16	-16
	16.7 Summary	-16
17	Using Transactional-Level Models in an SoC Design Flow	71
	Alain Clouard, Frank Ghenassia, Laurent Maillet-Contoz, and Jean-Philippe Strassen1	
	17.1 Introduction	
	17.2 Related Work	
	17.3 Overview of the System-to-RTL Design Flow	
	17.4 TLM — A Complementary View for the Design Flow	7-6
	17.5 TLM Modeling Application Programming Interface	-11
	17.6 Example of a Multimedia Platform	
	17.7 Design Flow Automation	
	17.8 Conclusion	-17
18	Assertion-Based Verification	
10	Erich Marschner and Harry Foster	8-1
	18.1 Introduction 1 18.2 History 1 <td></td>	
	18.3 State of the Art	0-0
19	Hardware Acceleration and Emulation	
	Ray Turner and Mike Bershteyn	19- 1
	19.1 Introduction	9-1
	19.2 Emulator Architecture Overview	
	19.3 Design Modeling	
	19.4 Debugging	
	19.5 Use Models	
	19.6 The Value of In-Circuit Emulation	
	19.7 Considerations for Successful Emulation 19.7 Considerations for Successful Emulation	
	19.8 Summary	
	17.6 Summary	

20	Formal	Property	Verification
----	--------	----------	--------------

Limor	Fix and Ken McMillan
20.1	Introduction
20.2	Formal Property Verification Methods and Technologies
20.3	Software Formal Verification
20.4	Summary

SECTION V Test

21 Design-For-Test		gn-For-Test
	Bernd	Koenemann
	21.1	Introduction
	21.2	The Objectives of Design-For-Test for Microelectronics Products
	21.3	Overview of Chip-Level Design-For-Test Techniques
	21.4	Conclusion
22	Auto	matic Test Pattern Generation
	Kwan	z-Ting (Tim) Cheng and Li-C. Wang
	22.1	Introduction
	22.2	Combinational ATPG
	22.3	Sequential ATPG
	22.4	ATPG and SAT
	22.5	Applications of ATPG
	22.6	High-Level ATPG
23	Anal	og and Mixed Signal Test
		a Kaminska
	23.1	Introduction
	23.2	Analog Circuits and Analog Specifications
	23.3	Testability Analysis
	23.4	Fault Modeling and Test Specification
	23.5	Catastrophic Fault Modeling and Simulation
	23.6	Parametric Faults, Worst-Case Tolerance Analysis, and Test Generation
	23.7	Design for Test — An Overview
	23.8	Analog Test Bus Standard
	23.9	Oscillation-Based DFT/BIST
	23.10	PLL, VCO, and Jitter Testing
	23.11	Review of Jitter Measurement Techniques
	23.12	Summary
Ind	ex	