Editorial to Special Issue DAC 2006

This special issue of the ACM *Journal of Emerging Technologies in Computing Systems* is based on papers presented at the 2006 IEEE/ACM Design Automation Conference (DAC). DAC has recently expanded its focus to include emerging technologies for computing and sensing systems. This broadened focus has been motivated in part by the roadblocks that loom ahead for the continued scaling of Silicon CMOS technology. New materials, new device geometries, and further downscaling of device dimensions and supply voltages are together leading to a significant escalation in manufacturing cost as well as unpredictable circuit performance due to process variability. As a result, experts are predicting that CMOS scaling will stop in the near future, perhaps as early as 2015.

Alternative computing technologies being explored today include carbon nanotubes, nanowires, molecular transistors, spin-based and single-electron devices, DNA-based devices, and hybrid circuits made from mainstream CMOS and newer nanodevices. Together with advances in manufacturing techniques, new design paradigms based on these emerging technologies are being explored. Research groups worldwide are addressing various aspects of circuit and system design such as modeling, analysis, defect tolerance, and synthesis.

Another motivation for expanding DAC's focus lies in the recent emergence of electronic systems that integrate MEMS and electrochemical components in sensor systems, biochips, and lab-on-chip devices. Technologies such as microfluidics are now mature enough to allow system integration and system-level design.

A call for papers for the JETC special issue was announced soon after DAC 2006. Full-length journal paper submissions were solicited from authors of papers on emerging technology topics at DAC 2006. All submissions went through the regular review process of JETC. After review and appropriate revisions, four papers were accepted for the special issue.

In the first article of this special issue, Paul et al. provide a device model for ballistic carbon nanotube FETs (CNFETs). The authors provide insights on how the parasitic fringe capacitance in CNFET geometries impacts the overall performance of CNFET circuits. In the second article, Yuh et al. describe a module-placement technique for defect-tolerant microfluidic biochips. A tree-based topological representation is used to model the placement problem. Next, Xu et al. address a design problem that is especially relevant for low-cost disposable biochips. The authors describe how a small number of input pins can be used to control a larger number of electrodes in a microfluidic array for high-throughput bioassays. In the final article of this special issue, Rad and Tehranipoor propose a hybrid FPGA that uses nanoscale clusters based on a crossbar of nanowires and a CMOS interface for intercluster routing. The authors analyze the delay and area of such hybrid FPGAs to traditional CMOS FPGAs.

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We thank the Editor-in-Chief for encouraging us to put together this special issue. We also thank all the authors who responded to the call for papers and the reviewers who submitted insightful reviews in a timely manner. We hope the readers of JETC will find this special issue to be a valuable resource for research on emerging technology topics.

KRISHNENDU CHAKRABARTY AND
SACHIN SAPATNEKAR
Guest Editors