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ABSTRACT

SciMeasure, in collaboration with Emory University and the Jet Propulsion Laboratory (JPL), has developed an extremely versatile CCD controller for use in adaptive optics, optical interferometry, and other applications requiring high-speed readout rates and/or low read noise. The overall architecture of this controller system will be discussed and its performance using both EEV CCD39 and MIT/LL CCID-19 detectors will be presented.

Initially developed for adaptive optics applications, this controller is used in the Palomar Adaptive Optics program (PALAO), the AO system developed by JPL for the 200" Hale telescope at Palomar Mountain. An overview of the PALAO system is discussed and diffraction-limited science results will be shown.

Recently modified under NASA SBIR Phase II funding for use in the Space Interferometry Mission testbeds, this controller is currently in use on the Micro-Arcsecond Metrology testbed at JPL. Details of a new vacuum-compatible remote CCD enclosure and specialized readout sequence programming will also be presented.

Keywords: adaptive optics, CCD, CCD controller, interferometry, PALAO, SIM, wavefront sensor, WFS

1. INTRODUCTION

This controller was first designed primarily by Ray DuVarney and Charlie Bleau in 1992 and built at Georgia Tech Research Institute (GTRI) under the leadership of Jim Beletic. Although the controller has gone through several design improvements, each iteration resulting in improved performance and improved system robustness and reliability, many of the original system design concepts remain unchanged. These include the 1.2 GHz fiber optic data link, the analog processing and correlated double sampling design and the 24 bit easily programmable sequencer. It is also worth noting that SciMeasure served as part of the FIERA controller design team and many of the features of this controller are shared by the FIERA controller[1].

A camera comprising this controller and a MIT/LL CCID19 was selected by JPL for use in the Palomar Adaptive Optics program. The camera forms part of a Shack-Hartmann wavefront sensor along with a 16x16 lenslet array. Wavefront information is used to control both a fast steering mirror for tip-tilt correction and a 349 actuator deformable mirror for higher order corrections. Recent results are reported in several companion papers[2,3,4,5,6,7].

Further development of the controller has been funded by NASA/JPL to provide a platform for the EEV CCD39, primarily to attain better read noise performance at the slower pixel rates required in interferometry. The controller has been developed specifically with the Space Interferometry Mission (SIM) testbeds in mind and is currently in use on the Micro-Arcsecond Metrology (MAM) testbed at JPL. A vacuum-compatible remote CCD enclosure has been developed as well as special sequence programming to allow the simultaneous readout of two quad cells for star tracking and integration and readout of fringes for fringe tracking on a single CCD.

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2. CAMERA SYSTEM OVERVIEW

Figure 1 shows an overview of the system in block diagram format. The system consists of four major components; the camera control unit, the camera head, the CCD enclosure which may be remote from the camera head electronics, and the camera head power supply.
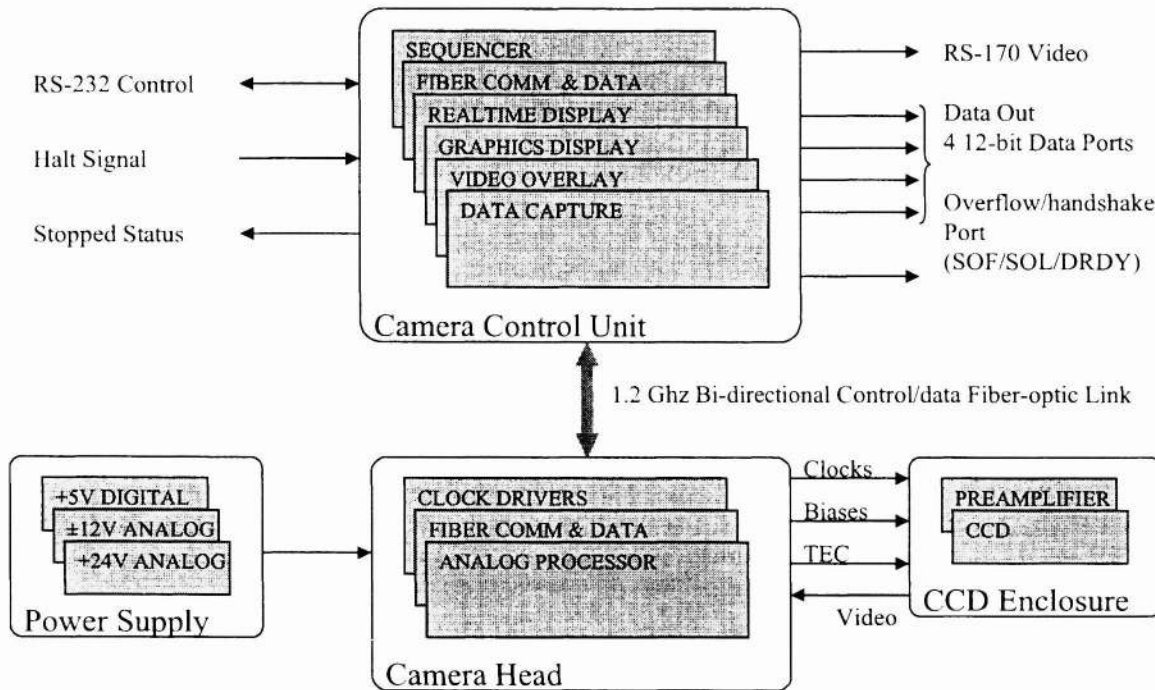

Figure 1. A block diagram showing all components of the camera system.

2.1. The camera control unit

The camera control unit consists of an embedded PC, 50 MHz 24-bit sequencer card, 1.2 GHz fiberoptic duplex communication link combined with a data demutiplexer, real time display card, graphics display card, graphics overlay card and data capture card. The embedded PC provides a backplane for the other cards in the system, an operating system, disk storage, networking, communications and a graphical user interface for operating and programming the controller. All camera control functions such as gain, offset, filter time constant and choice of display options may be controlled via RS-232 serial port.

The fiberoptic transceiver communications card in the control unit and the similar transceiver in the camera head form a synchronous phase-locked duplex communications link. Sequencer data is transmitted up to the camera head on each cycle of the sequencer 50 MHz master clock. On command from the sequencer, camera data from each of the four stripes or quadrants (depending on CCD geometry) is transmitted down from the head, received in the control unit and latched into the four digital data output ports. A fifth port is used for handshaking and data framing and provides a data ready (DRDY) signal in addition to start of frame (SOF) and start of line (SOL) signals.

The data and framing signals that are available at the five output ports on the control unit may also be captured internally by the data capture card. This card will hold just over a million pixel values and is used in conjunction with a suite of diagnostic software packages to evaluate the performance of the CCD and camera system.

The real time display is a scan converter that samples and captures each frame from up to four ports of video data and puts out a standard RGB/Sync RS-170 video signal. This live video signal can be displayed on any RGB video monitor and is overlaid with the virtual control panel graphics display to create a one monitor real time display and control system.

482

2.2. The sequencer

Figure 2 shows a block diagram of the sequencer architecture. It is RAM-based and consists of three banks of RAM, each with its associated address generators and control logic. The sequencer takes a multilevel approach to pattern generation,
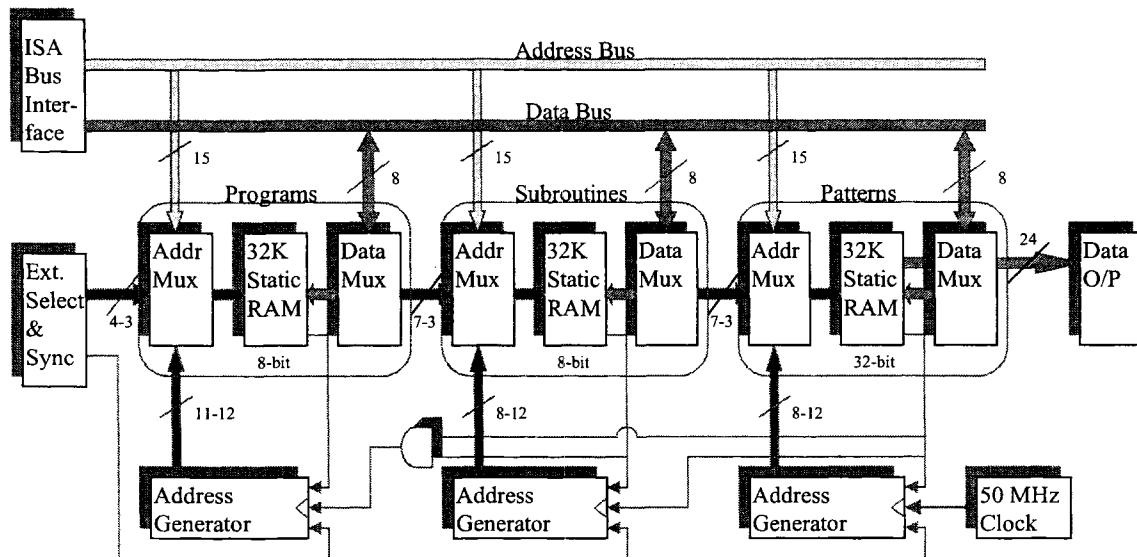

Figure 2. A block diagram of the controller's RAM based sequencer.

utilizing Programs, Subroutines and Patterns. The lowest level bank of RAM contains Patterns and is 32k 32-bit words. This bank takes its low order address bits from the 50MHz counter and its upper address bits from the pattern select or Subroutine bank which is the next bank of RAM. It in turn takes its most significant address bits from the third or Program bank of RAM and the remaining bits from its address generator which is clocked by reserved control bits within the pattern RAM bank that are set by the sequence compiler at sequence compile and load time. As in the case of the other two banks of RAM the Program bank takes its least significant address bits from a counter that is advanced or reset as directed by control bits within the RAM banks. The most significant bits of the Program bank may be externally controlled, allowing an external device or master control system to choose programs and switch between programs at the appropriate times. The sequencer logic also supports an external synchronization system whereby an external control device can halt or hold a sequence at a predetermined location within the cycle and then release it when ready.

Figure 3 shows the essential elements of a sequencer program. Programs consist first of all as defined Patterns. These Patterns are the binary zeros and ones that will be written to the very first section of the sequencer and will run the CCD clock phases, clamp, sample and turbo (filter bypass control), and provide operational codes that are decoded in the camera head as well as in the control unit. These codes are, for example, used to latch data, send start of line and send start of frame.

The Pattern that is shown in the figure is used to read a pixel from the serial register on the CCD. This particular Pattern performs a 480 ns read and is one of about a dozen patterns used in this typical program. Once Patterns have been defined and named they may be called from the camera system's simple syntax, high level programming language. Subroutines, which are collections of multiple Pattern calls that are frequently used, may also be defined and named. The Program then consists of a series of Subroutine and/or Pattern calls. An actual ten-line Program which reads the central 64x64 array of pixels on an EEV CCD39 at 1100 frames per second is shown in the figure.

Programs

```
define program 0;# 1100 Hz Nominal

    subroutine start_of_frame;
    repeat 32;
        subroutine read_line;
    end repeat;
    repeat 2;
        subroutine integrate;
    end repeat;
end define;
```

Subroutines

```
define subroutine read_line;

    pattern send_start_of_line 1;
    pattern shift_line       1;
    pattern wait            10;
    pattern shift_pixel     17;
    pattern read_pixel      32;

end define;
```

Patterns

```
define pattern read_pixel;

#
# t = /turbo, c = /clamp, S = sample, V = *DCAV
#      RG IA  BS   OR   xxx t c S CCCC FV xx
#      123 123 123           0123

    0  010 010 010 000 0 1 0 1111 01 00;   #
    0  010 010 010 000 0 1 0 1111 01 00;   #
    1  010 010 010 000 0 1 0 1111 01 00;   #
    0  010 010 010 000 0 1 0 1111 01 00;   #
    0  010 010 010 000 0 0 0 1111 01 00;   #
    0  010 010 010 000 1 0 1 1111 01 00;   #
    0  010 010 010 000 1 0 1 1111 01 00;   #
    0  010 010 010 000 1 0 1 1111 01 00;   #

    0  010 010 001 000 1 0 1 0000 01 00;   #
    0  010 010 001 000 1 0 1 0011 01 00;   #
    0  010 010 001 000 1 0 1 1000 01 00;   #
    0  010 010 001 000 0 0 1 0100 01 00;   #
    0  010 010 001 000 0 0 1 1100 01 00;   #
    0  010 010 001 000 0 0 1 0010 01 00;   #
    0  010 010 001 000 0 0 1 1010 01 00;   #
    0  010 010 100 000 0 0 1 0110 01 00;   #

    0  010 010 100 000 0 0 1 1111 01 00;   #
    0  010 010 100 000 0 0 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #
    0  010 010 100 000 0 1 0 1111 01 00;   #

end define;
```

Figure 3. A typical sequencer pattern and a simple program.

2.3. The camera head

The camera head performs three basic functions. A fiberoptic communication and data multiplexer card communicates with the control unit; a clock driver card drives the various CCD clock phases and reset; and an analog processor card processes and converts the CCD analog output to 12-bit digital data.

The fiberoptic communication and data multiplexer card is the complement of the communications card in the control unit. These cards form the 1.2 GHz phase-locked bi-directional communication link between the control unit and the camera head which operates essentially as a 50 MHz 20-bit virtual ribbon cable. The sequencer provides 4-bit command codes and 16-bit clock patterns which are serialized and sent to the camera head. The command codes are interpreted by the cards that use them, 12 bits of the clock patterns are sent to the clock driver board and 3 bits are sent to the analog processor card and are interpreted as Clamp, Sample and Turbo. The 12-bit digital data, plus an overflow/underflow bit, are received from the analog processor card and are sent back to the control unit along with their corresponding codes. Once per frame an additional 18-bit control word is sent to set gain, offset and filter controls.

The head also contains a clock driver card that has twelve two-level drivers. The lower clock level can be set at any voltage between -11 volts and +11 volts and the span between the upper and lower clock level may be adjusted to any voltage from 0 volts to +16 volts so long as the upper clock level does not exceed +11 volts. The analog processing card provides bias voltages which operate the CCD and receives, amplifies, filters, clamps and baseline restores and then digitizes up to four channels of video signal as received from the CCD or preamplifier. The CCD enclosure houses the CCD in its thermoelectric cooler (TEC) package and the preamplifier board which in addition to the first stage of video signal amplification also holds the bias, clock, and TEC filters. The heat sink for the TEC is brought out to the back of the CCD enclosure and may be either air or liquid cooled. The CCD enclosure may be located remotely from the camera head electronics or attached directly to the camera head electronics box. We have not observed any degradation in low noise performance with the CCD enclosure as far as two meters from the camera head.

Figure 4 shows a block diagram for one of the channels on the analog processor board. The input is terminated in 75 Ohms since the preamplifier is driving the video signal over a 75 Ohm coaxial cable. The system is designed to support four selectable amplifier gains and four selectable filter time constants that can be optimized for any user's specific needs. The clamp and sample scheme is fairly typical. The clamp is implemented with an SD210 high-speed analog switch and the offset for each channel can be varied independently from 0 Volts to –2.55 Volts. The A to D converter is a 12 bit, 10MHz Analog Devices part with an internal sample and hold and a conversion range that is set between plus and minus one volt. An
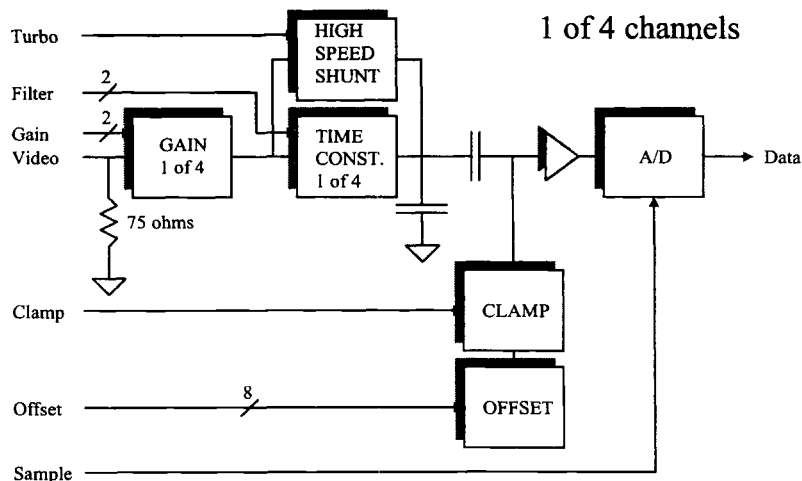
484

Figure 4. A block diagram of one channel of the controller's analog processor.

important feature on this analog processor is the high-speed filter shunt, similar in principle to that described by Solhusvik et al[8]. When enabled by the turbo signal, this device which is placed across the resistor chain that forms the RC time constant, has an effective resistance of about 2 Ohms. This reduces the time constant by approximately two orders of magnitude and allows the signal to come to equilibrium in a few tens of nanoseconds even though the filter time constant may be set for several hundreds of nanoseconds. We use this filter shunt during the reset phase of the pixel read. It eliminates the long wait time one normally needs for the reset pulse feedthrough to relax to equilibrium before the clamp is released and the charge from the next pixel is clocked onto the output gate. Because of this dual time constant capability we can, for any given pixel rate, use a longer time constant for the pixel read and sample portion of the read cycle than we could if that same time constant was operative during the reset phase. This reduces the read noise we would otherwise have for that particular pixel read rate. Conversely, we can achieve a higher pixel rate for a given read noise.

Table 1 shows our performance results for the EEV CCD39 at pixel read rates ranging from 80 thousand pixels/sec/port to 2 million pixels/sec/port. The CCD was mounted in a TEC-cooled housing and the temperature was maintained at –25 degrees Centigrade for all measurements. The frame rate is based on a 64x64 pixel frame size and the noise was calculated from the photon transfer curve. Running at 1.1. Mpixels/sec/port, this camera also achieved noise performance of 4.5 rms electrons with a MIT/LL CCID11 and 5.9 rms electrons with a CCID19. These noise measurements were all performed at an approximate gain of 1 electron/data number with optimal filtration.

Camera Performance

Noise (e-)	Pixel Rate (pixels/sec/port)	Frame Rate (/sec)
3.0	80 kpix	34
3.5	178 kpix	110
5.9	1.14 Mpix	550
7.5	2.00 Mpix	1100

Table 1. Controller noise performance at various read rates for the EEVCCD39.

The responsivity of the EEV CCD39 is approximately 4 microvolts/electron. In order to reduce dark current to an insignificant level the clocking levels were set for substrate inversion clocking and during the integration time two of the three

image array clock phases were held low. To achieve surface substrate inversion in the above mentioned EEV device the low level clock voltages were kept lower than –6 Volts and the substrate was held at 0 Volts. At the lower frame rates it was also necessary to employ dithering to maintain substrate inversion under all clock phases[9,10].

3. PALOMAR ADAPTIVE OPTICS SYSTEM (PALAO)

The camera controllers described above have been used in direct support of the adaptive optics (AO) development program at JPL, where a facility class AO instrument has been designed and built for the 5m diameter Hale Telescope at Palomar Mountain[11,12,13,14,15,16,17].

3.1. PALAO overview

The Palomar Adaptive Optics System mounts at the Cassegrain focus of the telescope and is optimized for scientific use in the infrared (K, H, and J-bands). The PALAO system has at its heart a Xinetics 349 actuator deformable mirror (DM) and utilizes a Shack-Hartmann-based wavefront sensor (WFS). The WFS is based upon the SciMeasure controller, MIT/LL CCID19 detector and a 16 x 16 subaperture lenslet array, within which is inscribed a reduced image of the 5 meter telescope pupil. Initially natural guide star based, the system is designed to accommodate future upgrades without significant modification to the optical design.

An optical layout of the PALAO system is presented in Figure 5. Light, diverging beyond the Cassegrain focus of the telescope is intercepted by fold mirror 1 (FM1) and sent to a collimating off-axis parabolic mirror (OAP1) which forms a
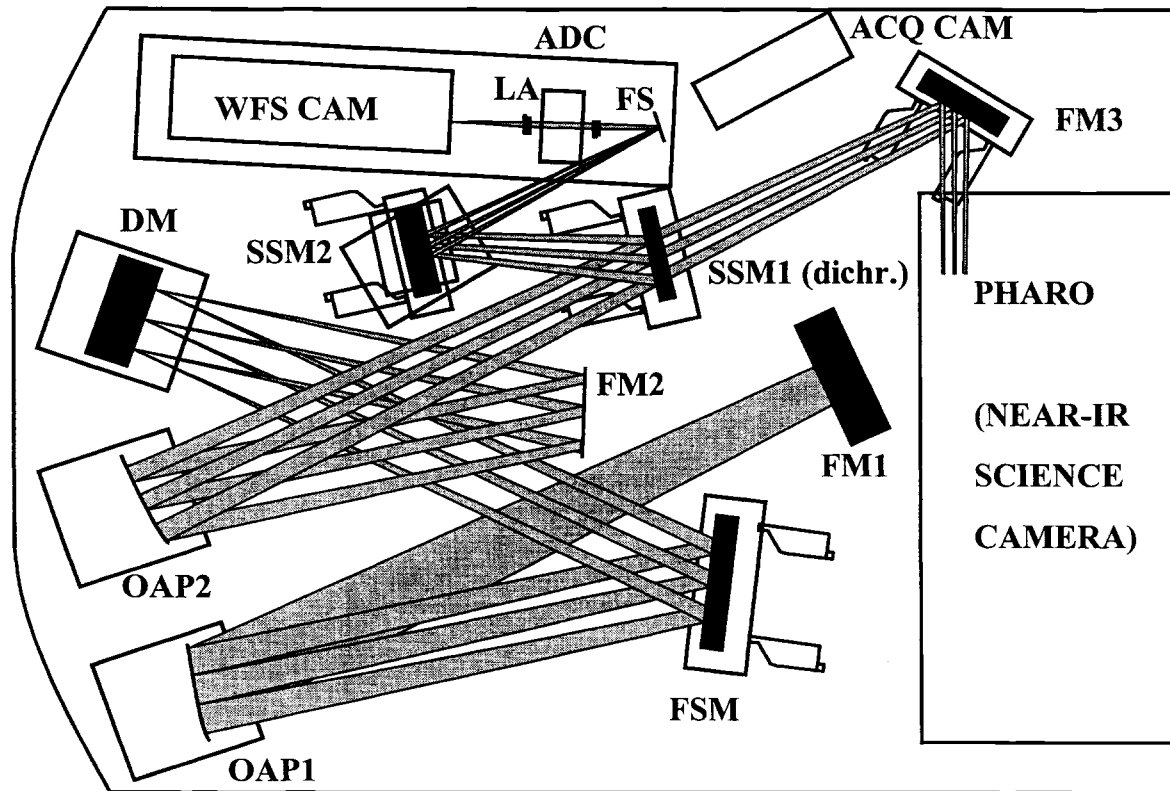

Figure 5. Shows the major components and optical layout of the PALAO system.

relayed image of the telescope pupil at the deformable mirror (DM). A separate fast steering mirror (FSM) is used to control global tip/tilt, based upon the same WFS information as that controlling the DM. The corrected wavefront is reimaged using another off-axis parabola (OAP2). Thereafter, visible light is reflected off a dichroic mirror (SSM1) to the WFS. The guide

486

star is selected using a pair of actuated mirrors (SSM1 and SSM2), used in combination with an acquisition camera (ACQ CAM) and a reflective field stop (FS). Within the WFS, the wavefront is segmented by the lenslet array (LA), then reimaged onto the SciMeasure camera (WFS CAM). Infrared light is transmitted by the dichroic mirror (SSM1) and is directed into the science camera, PHARO.

User control of the PALAO system is implemented through control software running on a Sun workstation, which manages communications between the AO system, the telescope, and the science instrument, currently the Cornell-built PHARO camera[18]. The workstation also communicates with the embedded system controller running on a PowerPC in a VME environment, which in turn communicates with 10 Texas Instruments C40 DSPs on 3 VME boards. The PowerPC processor, running VxWorks, coordinates motor control and system telemetry signals, including video, as well as the wavefront controller high level functions, such as loading reconstruction matrices and control loop filters onto the DSPs. The 10 TI C40 DSPs flat-field the incoming WFS pixel data, calculate the WFS subarray centroid values, reconstruct the wavefront, and generate DM actuator commands, with a typical sample rate of 500 Hz. The interface between the SciMeasure controller and the JPL DSP engine consists of a custom interface board designed to interface the 4 parallel serial port lines (available from the WFS camera PC) to 4 C40 DSP comm ports.

Performance of the SciMeasure camera in the field agrees closely with performance tested in the laboratory. Operating at 550 frames per second or 1.1 Mpix/sec/port, on the telescope, the MIT/LL based camera was found to have 6.1 electrons rms read noise, with a variation of ± 0.1 electrons across the 4 channels of the camera, using an 8' shielded power cable designed by SciMeasure. This compares favorably with the 5.9 electrons rms measured in the laboratory.

3.2. Example PALAO results

An example of the improved image quality provided by the PALAO system is shown in Figure 6. Within this figure, the left-
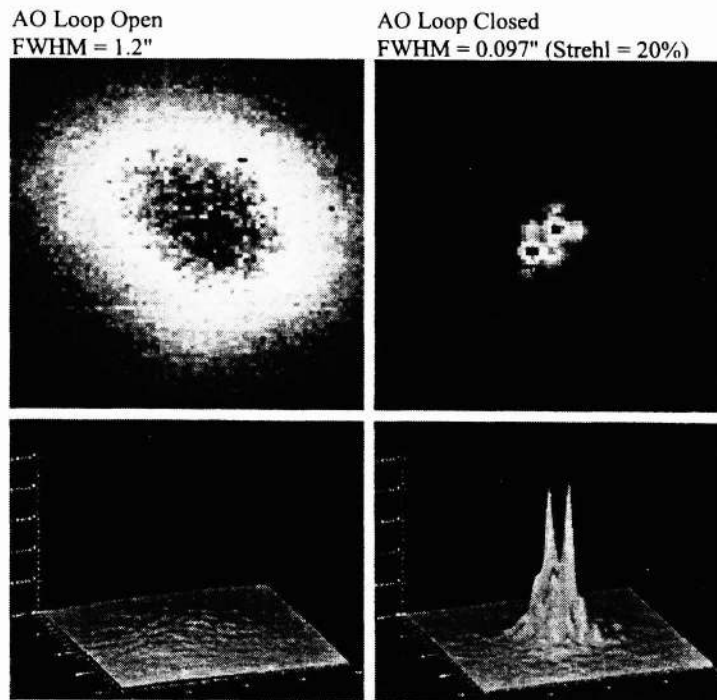

Figure 6. 20 second K-band image comparison with PALAO loop open and closed.

hand two K-band images represent the open-loop grayscale and isometric views of a 20 second exposure image of QS Aql, a known bright binary star pair with 0.185 arcsec separation.

The K-band seeing in this image is approximately 1.2 arcsec FWHM, indicating rather poor seeing for the Palomar site. The right-hand images of the same exposure, obtained with the PALAO system operating. The binary nature of QS Aql is clearly

observed, although due to the poor seeing conditions, the Strehl ratio is only a few percent. More recent observations have achieved Strehl ratios as high as 50% in K-band in better seeing conditions and the science results of these observations can be seen in several companion papers[2,3,4,5,6,7].

4. MICRO-ARCSECOND METROLOGY (MAM) TESTBED

The Space Interferometry Mission (SIM) is a high precision orbiting long-baseline interferometer under development at JPL[19]. SIM relies on high-precision measurement of visible broadband stellar interference fringes to determine the position of a star to a few micro-arcseconds. A laboratory demonstration of this technology is being implemented at JPL in the Micro-Arcsecond Metrology (MAM) testbed[20].

4.1. MAM overview

MAM is a single-baseline interferometer with a 1.6 m baseline. The interferometer is built in a large, vibration isolated, vacuum tank. The vacuum is necessary to eliminate air turbulence and refraction, which would otherwise be limiting factors at the required precision. The MAM artificial star is itself an interferometer in reverse. Two collimated beams originating from the same single-mode point source and capable of moving over a 15 degree field-of-regard are directed toward the MAM interferometer, as illustrated in Figure 7.
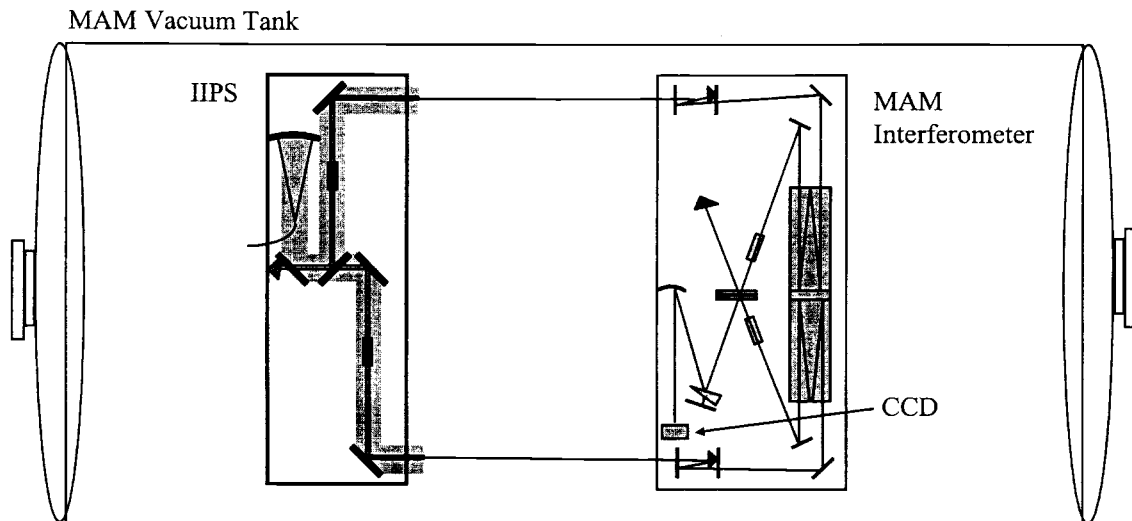

Figure 7. Diagram showing the MAM interferometer and the inverse interferometer pseudo-star inside the MAM vacuum tank.

Each incoming collimated beam is captured by a steerable siderostat that directs the light toward a tip-tilt control mirror. The light is then directed into an optical cat's-eye delay line that adjusts the optical path difference between the two arms to within the coherence length of the interferometer's spectrometer. Upon exiting the delay line, the red and blue components of the light are separated by a dichroic mirror. The red light from one arm will be combined with red light from the other to form dispersed interference fringes, while the blue beams are focused onto the detector to serve as guide-spots for angle tracking. Figure 8 shows how the signals appear on the SciMeasure CCD. A complete description of the optical train can be found in Carlson et al[21].

4.2. CCD readout requirements

The SciMeasure CCD camera serves as both the fringe sensor and the fine-guidance sensor. These functions have complementary requirements. The fringe sensor requires the detection of ~10^9 photo-electrons to achieve the desired signal-to-noise ratio. This is a slow process, requiring ~ 50 exposures, during which time the fringe phase is stabilized using the

488

MAM heterodyne laser metrology system[20]. The fine-guidance sensor function, on the other hand, requires a rapid readout (~ 500 Hz) of relatively few pixels.

The arrangement of the fringes and guide-spot regions on the camera (Figure 8) allows both fringe sensing and fine-guidance functions to operate at independent rates. The camera is operated with three regions-of-interest: two quad-cells for guiding
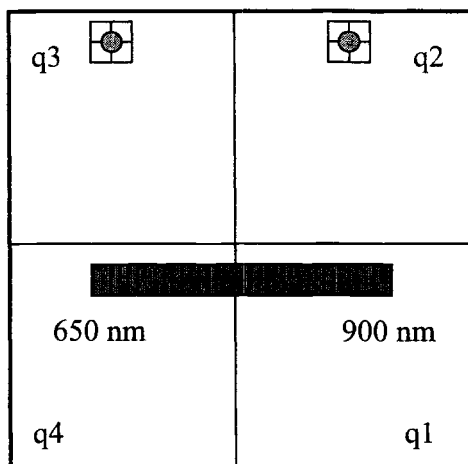

Figure 8. Dispersed fringe and guide spots on the SciMeasure CCD. The dispersion covers 650 - 900 nm across 40 pixels. The diffraction-limited guide spots are formed from f/10 beams and are smaller than a pixel. Thus to serve as guide spots it is necessary to position them over the corners of 4 pixels which are treated as a quad cell.

and one row of pixels for the dispersed fringes. The guide spots are positioned near the upper edge of two quadrants. They are symmetrically placed about the center of the CCD so that the two 2x2 regions are read out simultaneously with a minimum of parallel and serial transfers. The fringe window symmetrically spans the lower two quadrants for the same reason. It can integrate for an arbitrarily long time when simulating a faint star. Additionally, it can be shifted down on the CCD so that a set of dispersed fringes at different optical path positions is recorded in a single long-exposure frame.

The camera software facilitates alignment of all three regions. When performing initial alignment, the camera is switched to full-frame mode. A window on the PC displays boxes around the regions of interest, allowing the user to position the guide spots and dispersed fringes within their designated regions. The camera is then switched to the data mode, in which only the regions of interest are recorded at the low-noise 80 kpix/sec/port rate yielding a rms read noise of 3 electrons/pixel.

In order to accommodate these requirements, three special sequences were developed. The full-frame readout sequence is similar to previously developed full-frame sequences, but has been made to run at standard video rates and include three target rectangles on-screen to facilitate the alignment process. The quad-cell readout sequence is also similar to a standard quad-cell readout sequence, except that it transfers only those rows necessary to read out the quad cells from the image array into the frame store, then transfers the image array back to its initial position to allow the fringe image to continue to integrate. The fringe image continues to integrate while the quad cells are read out of the CCD. Although all the pixels are shifted out of the frame store, blank lines are binned in the serial register, then the serial register is emptied and the pixel values discarded. For the two lines containing the quad-cells, only the two pixels containing the quad cell are converted. The fringe readout sequence is similar to the full-frame readout, except that as for the quad-cell readout the blank lines are binned and discarded and the blank pixels are also discarded.

489

4.3. Vacuum–compatible remote enclosure

To operate in vacuum, the CCD enclosure is separated from the camera head electronics, and the enclosure (which includes the CCD, thermo-electric cooler, and pre-amplifiers) is placed in a vacuum vessel (Figure 9). The vessel is back-filled with Argon gas at room-pressure. Heat from the TEC is removed from the tank using chilled liquid lines that run through the back of the vessel. The distance between the head and the analog electronics is 2 m. There appears to be no degradation in performance in this configuration compared to the standard co-located head/electronics package.
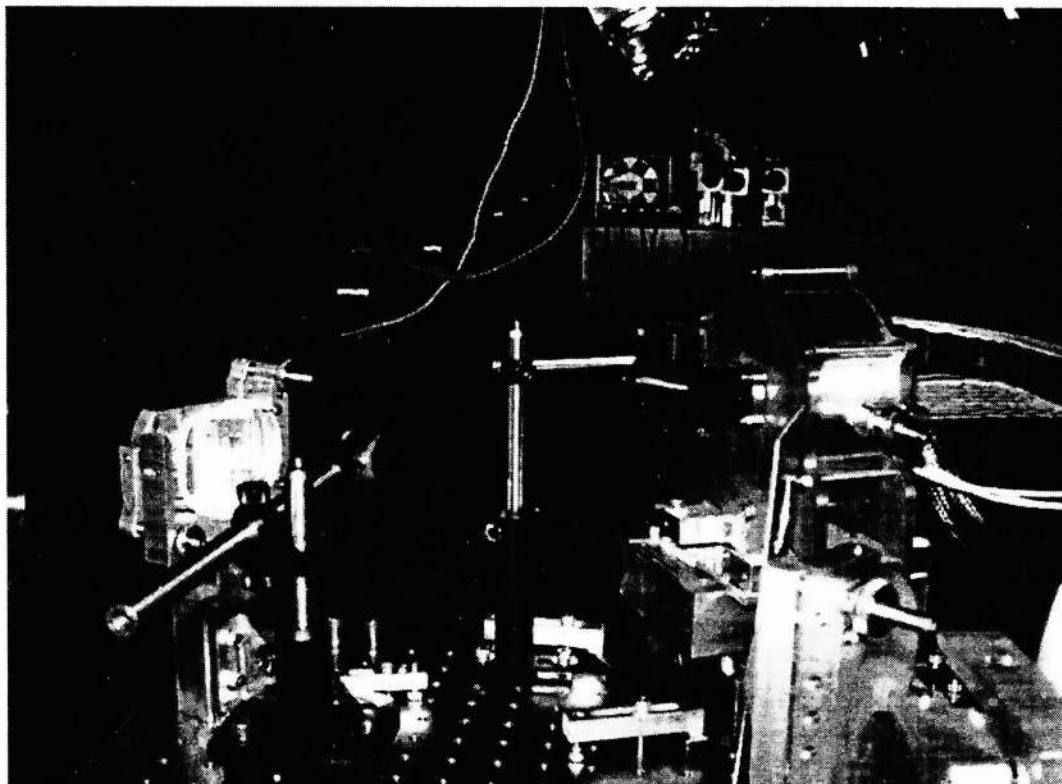

Figure 9. The vacuum-compatible remote CCD head in the MAM interferometer.

5. FUTURE WORK

We are continuing to develop the design of the controller, specifically to reduce volume, mass and power requirements while increasing functionality and flexibility. The next generation design includes such features as 16 CCD clocks, 14-bit and 16-bit A/D converters, a 16-bit data path and a highly modular format based on a 3U 160mm form factor. Tests with switching rather than linear power supplies have been shown to add no noise to the system with the proper filtration.

ACKNOWLEDGEMENTS

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