

# Effect and Utilization of Common Source Inductance in Synchronous Rectification

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**Abstract**---Synchronous rectification is widely used in low voltage high current applications to reduce conduction loss. Common source inductance is the inductance shared by gate driver loop and main power transfer path. Minimization of common source inductance has been accepted as a common design rule for power converters involve power MOSFET. In this paper, the effects of common source inductance for control and sync FET are explored in detail. In contra to traditional belief, common source inductance of sync FET could provide significant benefits. With common source inductance, minimal dead time, shoot through prevention and  $Cdv/dt$  immunity could be achieved for sync FET. Significant improvement on power loss could be achieved for synchronous rectification.

## I. INTRODUCTION

With advanced VLSI technology, digital systems are calling for lower supply voltage and higher current. Low output voltage and high output current DC/DC converter are widely used to power those systems. Synchronous rectification is a must technology for these applications [1][2]. It greatly reduces conduction loss compared with diode rectifier. Two examples of synchronous rectification are shown in Fig.1. Fig.1 (a) shows a synchronous buck converter. Fig.1 (b) shows an isolated half bridge converter with synchronous rectifier.

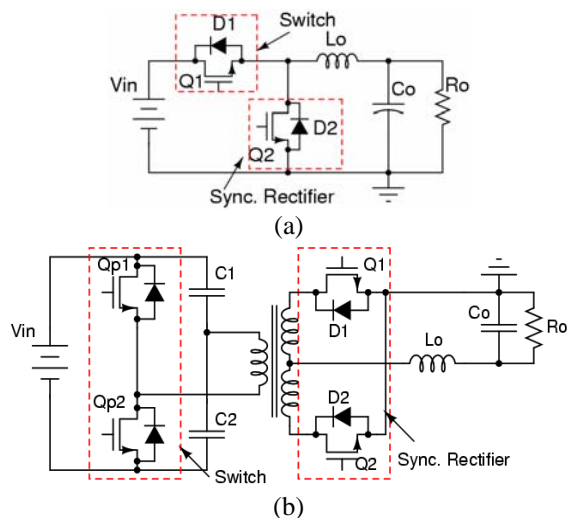


Fig. 1 Two examples of synchronous rectification

Common source inductance is the inductance shared by main current path and gate driver loop as shown in Fig.2.  $L_{CSI}$  will carry the drain source current and the gate charging current. Any voltage induced on  $L_{CSI}$  will show up in the  $V_{GS}$  of MOSFET Q. Because of the importance of  $V_{GS}$  on the switching performance of power MOSFET, common source inductance has very significant impact on the system performance.

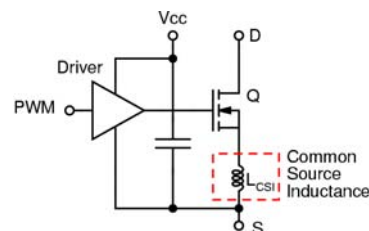


Fig. 2 Common source inductance

In this paper, the impact of common source inductance on the switching performance of power MOSFET will be studied. It is shown that common source inductance has very different impact on the power MOSFET used as active switch or as synchronous rectifier.

For power MOSFET used as active switch, common source inductance will greatly increase the switching loss with extended switching time. For power MOSFET used as synchronous rectifier though, common source inductance could be used to reduce dead time loss, prevent cross conduction, prevent  $Cdv/dt$  induced turn on and reduce body diode reverse recovery loss.

## II. COMMON SOURCE INDUCTANCE EFFECT

In following analysis, synchronous BUCK converter as shown in Fig.1 (a) will be used to demonstrate the concept of common source inductance effect. Because of the similarity of the operation for synchronous rectification in other topologies, the concept will be extended to other type of synchronous rectification applications later.

As shown in Fig.2, The drain source current of power MOSFET Q will flow through  $L_{CSI}$ , while  $L_{CSI}$  is also in the gate driver loop. Change of the drain source current will induce a voltage across common source inductance  $L_{CSI}$ . This

voltage will actively modify the gate source voltage of power MOSFET. The effect will be significant during turn on and turn off of power MOSFET during which  $I_{DS}$  and  $V_{GS}$  make fast changes.

Fig.3 shows the effect of common source inductance during turn on and turn off instance for power MOSFET used as an active switch. Fig.3 (a) shows the effect during turn on of switch Q1. When voltage is applied to turn on Q1, the voltage induced on LCSI is against  $V_{GS}$ . This will slow down the turn on of power MOSFET. Same effect can be observed during turn off of Q1 in Fig.3 (b).

The waveforms are shown in Fig.4, The turn on and off time will be greatly increased by common source inductance. Simulation was performed for a sync BUCK converter with 12V input, 1.3V and 30A output working at 500kHz. The result is shown in Fig.5. As shown, power loss increase dramatically with just 1nH common source inductance.

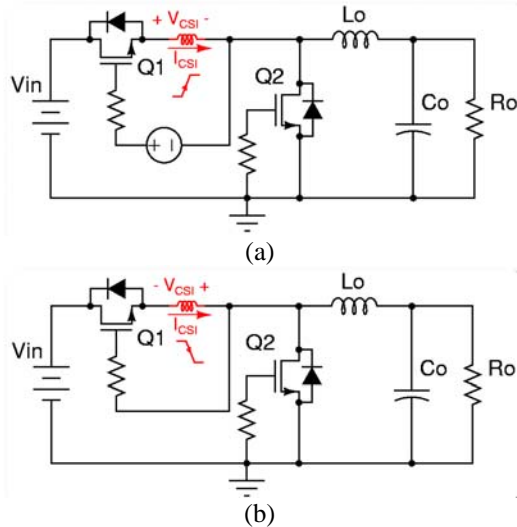


Fig. 3 Impact of commons source inductance during turn on and turn off

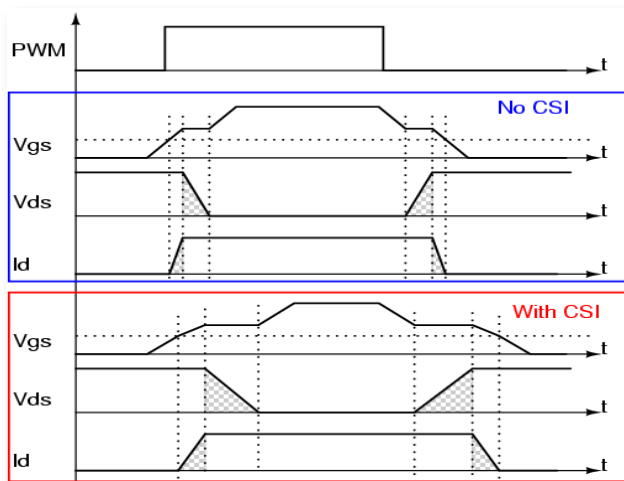


Fig. 4 Waveforms of turn on and turn off for Q1 with and without CSI

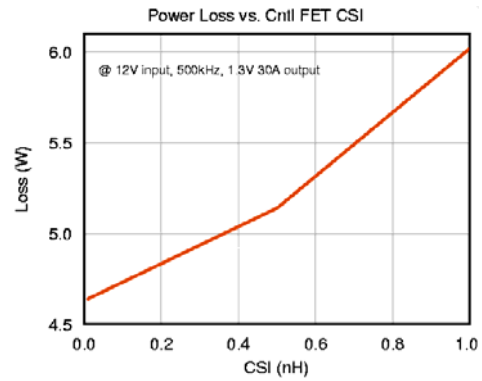


Fig. 5 Impact of common source inductance for power switch

The negative effect of CSI on switching loss is accepted by industry. Layout of power converters is carefully considered to minimize this effect. In fact, this design rule was been extended to all power MOSFET and gate drive layouts include power MOSFET used as synchronous rectifier.

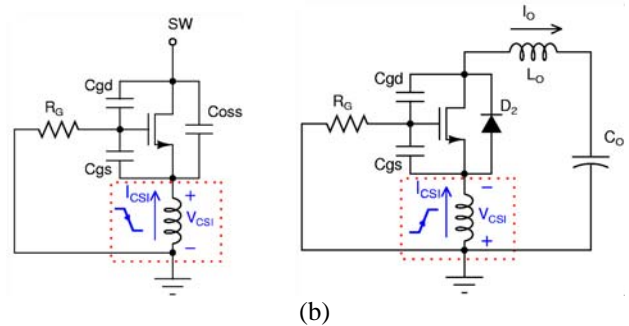
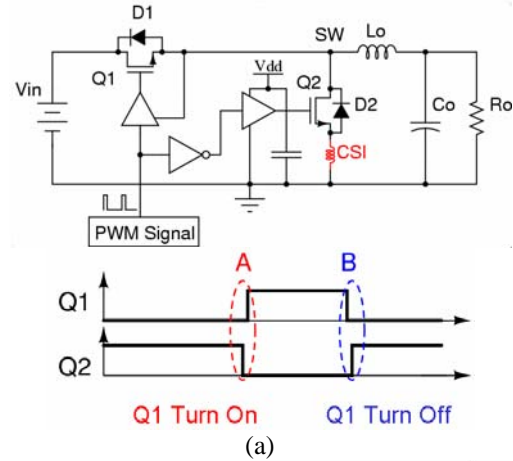


Fig. 6 Common source inductance effect for synchronous rectifier

In contrary to common belief, the effect of common source inductance for sync FET is found to be very different.

For synchronous rectifier, the power MOSFET is used as a diode. The current direction is from source to drain. Because of this difference, the effect of common source inductance on the switching action is very different. Fig.6 shows the impact of sync FET Q2 common source inductance during turn on and turn off of control FET Q1. Since Q2 is used as synchronous rectifier, its gate signal doesn't change the operation mode of converter because the existence of body

diode. The time instances during which common source inductance will affect the operation of the circuit is during turn on and turn off of control FET Q1.

Fig.6 (b) shows those two instances when Q1 is turned on and off. During both instances, Q2 is turned off by connect the gate to ground. At the time when Q1 is turned on, load current will commute from Q2 path to Q1. As current decrease, a voltage will be induced on common source inductance. The effect of this voltage in gate loop of Q2 will charge VGS2 into negative voltage, which will keep Q2 in off stage. When control switch Q1 is turned off, the effect of common source inductance will help to turn synchronous FET Q2 on right when Q1 is turned off. In next section, utilization of these effects will be discussed.

### III. UTILIZATION OF COMMON SOURCE INDUCTANCE IN SYNCHRONOUS RECTIFICATION

From previous discussion, the effects of sync FET common source inductance are as following: when control FET is turned on, common source inductance will help keep sync FET into off state; when control FET is turned off, common source inductance will work to turn sync FET on without any delay. This is exactly what we desired for this circuit to work. In following part, the use of these effects will be explored.

#### *Cdv/dt immunity:*

As discussed in [3][4], high dv/dt on switching node caused by turn on of control FET Q1 will cause false turn on of sync FET Q2 and cause high power loss. With Sync FET common source inductance, this problem can be solved as shown in Fig.7.

When control FET Q1 is turned on, first load current will commute from sync FET branch to Q1 branch. During this transition, sync FET Q2 gate source voltage will be charged to a negative voltage. The values of this voltage can be adjusted by common source inductance. After the whole load current been transferred to Q1, switching node SW will begin to rise with high dv/dt. This dv/dt will cause a change current to Q2 gate through miller capacitor of Q2. Since Q2 gate voltage is already charged to negative, even with Cdv/dt effect, the gate voltage of Q2 will not rise to the threshold voltage.

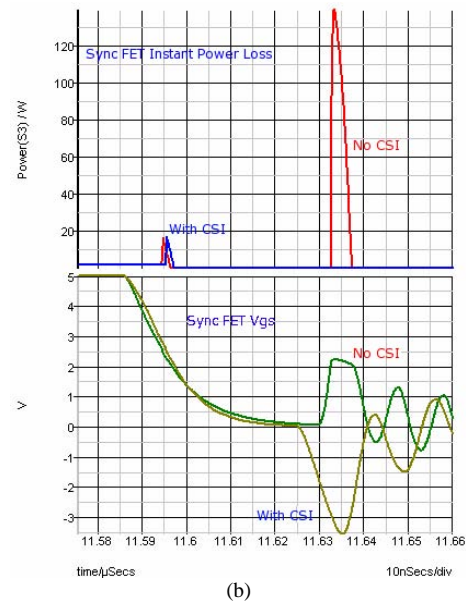
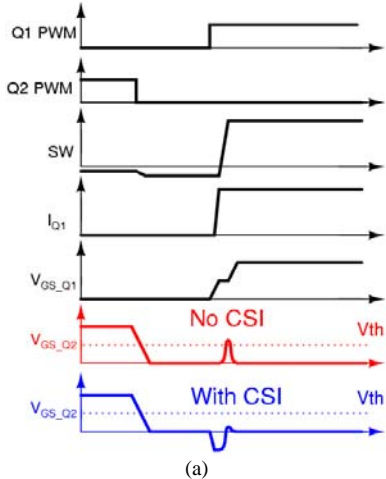


Fig. 7 Cdv/dt immunity with common source inductance

Fig.7 (b) shows the simulation waveform of sync FET gate source voltage and power loss. It is clear that Cdv/dt could cause high power loss in power MOSFET without CSI. Simulation was performed with International Rectifier IRF6618 as sync FET. The power loss of a 1MHz, 12V to 1.2V converter is reduced from 6.04W to 5.62W by using 2.5nH common source inductance.

Another benefit is that without worry about Cdv/dt problem, power MOSFET could be designed with lower Rds(on). This could provide further improvement on sync FET power loss.

#### *Shoot through prevention and Deadtime reduction:*

From previous discussion, common source inductance of sync FET will automatically turn off sync FET when control FET is turned on. On the other side, when control FET is turned off, sync FET will be automatically turned on by common source inductance. This effect provides two benefits. First, even there is a short overlap on control FET and sync FET drive signal; common source inductance will generate voltage to turn sync FET off. This will prevent the damage from shoot through. Another benefit is reduced deadtime.

Deadtime is needed to prevent shoot through as shown in Fig.8. During deadtime, body diode of sync FET will conduct. Since diode has high forward voltage drop, this will cause high power loss. For 1MHz switching frequency, deadtime loss is almost 1/3 of total sync FET loss. As switching frequency goes higher, this will becomes more serious a problem.

Fig. 9 shows the comparison of body diode loss for a synchronous buck converter. With common source inductance, body diode loss is greatly reduced. The power loss of a 500kHz, 12V to 1.2V converter is reduced from 5.26W to 4.78W with reduced deadtime after using 2.5nH common source inductance.

As lower  $R_{dson}$  is required for sync FET, it normally has big area. Turn on and off time is slow. With common source inductance, more overdrive is provided to turn on and off sync FET. The turn on a turn off time could be reduced.

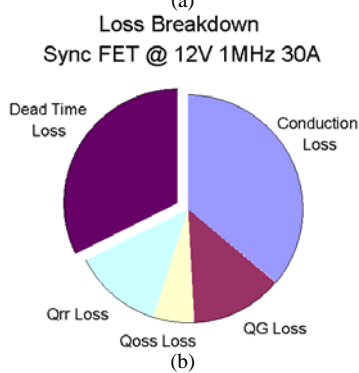
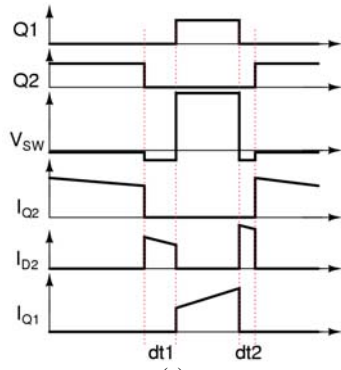


Fig. 8 Deadtime and loss breakdown for sync FET

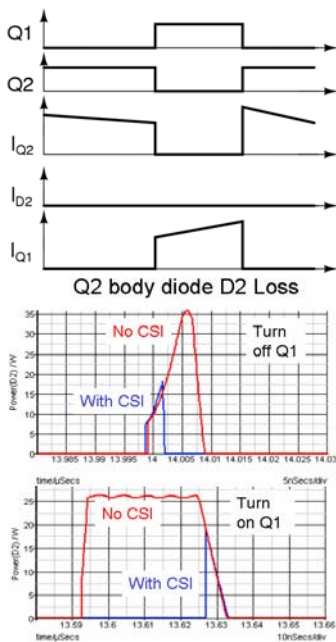


Fig. 9 Comparison of bodydiode loss with and without common source inductance

**Self-driven for synchronous BUCK converter:**

As seen above, common source inductance can help turn on and off sync FET at desired switching instance. The gate driver is less important here for sync FET. For sync FET, its gate source capacitance is normally very big. This gives us opportunity to use self-driven for sync BUCK topology as shown in Fig.10. During turn on of control FET Q1, common source inductance will turn off sync FET Q2, and then big  $C_{gs}$  will hold this voltage until we turn off control FET Q1. At that time, common source inductance will charge sync FET Q2 gate source voltage up and turn Q2 on. This could greatly simplify the driver circuit and reduce the cost.

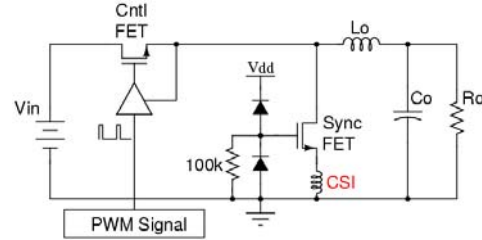


Fig. 10 Self-driven synchronous buck converter

**Extension of the concept:**

Above analysis using synchronous buck converter as an example, in fact, this concept could be extended to other topology too. Implementation of the concept for isolated synchronous rectification applications are shown in Fig.11.

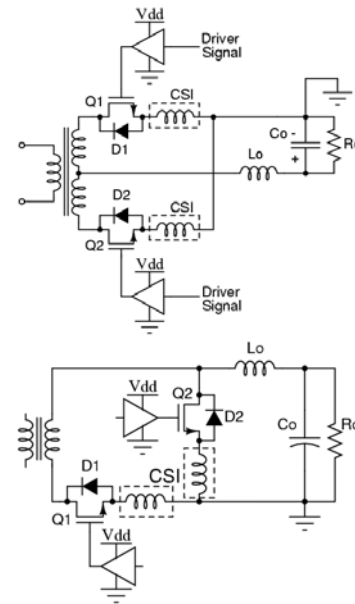


Fig. 11 Common source inductance for isolated applications

IV. SUMMARY

Common source inductance can greatly impact the switching acting of power MOSFET because of its special location. For power MOSFET used as switch, common source inductance could significantly increase switching loss.

For power MOSFET used as synchronous rectifier, common source inductance could help to reduce power loss.

This is because the different current direction in synchronous rectifier compared with switch. With common source inductance,  $Cdv/dt$  immunity and zero deadtime switching could be achieved. It could significantly reduce power loss on synchronous rectifier.

Since only 2 to 3nH inductance is needed to achieve these effect, this inductance could be implemented with parasitic inductance, which include packaging inductance and trace inductance. No extra magnetic component is needed.

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