Effect of ESD on Complex Programmable Logic Device and Field Programmable Gate Arrays

Rajashree Narendra, BNM Institute of Technology, Bangalore, India, rajashree.narendra@gmail.com

M.L.Sudheer, UVCE, Bangalore, India, mlsudheer@indiatimes.com

D.C.Pande, EMI/EMC group, LRDE, Bangalore, India, pande.dc@gmail.com

Abstract— Complex electronics devices are becoming more sensitive to electrostatic discharge (ESD). These components are being developed with higher density (extra memory bits per unit volume) and are becoming faster (MHz, GHz, THz, etc.). These upgrades in technology do not come without a "technological price". By enhancing the products' performance to meet the users' demands and requirements, one drawback is the reduction in the ESD sensitivity voltage levels. Indirect and direct air/contact discharge test has been conducted on the ALS-SDA-CPLD/FPGA trainer kit linked to the digital to analog converter (DAC) module. The Field Programmable Gate Arrays (FPGA) and Complex Programmable Logic Devices (CPLD) are found to be very ESD sensitive. The FPGA 3s50 IC was affected during the contact discharge to the input pin. There was damage to the bond pad as well as the metal top layer was damaged. The DAC ICs were affected during the ESD discharge - one due to direct ESD effects and the other due to indirect ESD effects. There was dielectric breakdown damage observed in the CPLD 9572 IC.

Keywords— System level ESD, FPGA, CPLD, Complex electronics, Indirect discharge, Direct Air/Contact discharge

I. Introduction

Electrostatic Discharge (ESD) is generally recognized as an increasingly important issue for modern integrated circuits. Thinner gate oxides, complex chips with multiple power supplies and/or mixed-signal blocks, larger chip capacitance and faster circuit operation [1-4] all contribute to increased ESD sensitivity of advanced semiconductor products. For instance, you may find that a serial port IC has an ESD withstand voltage of 15KV! By the same token, a Complex Programmable Logic Device (CPLD) and Field Programmable Gate Arrays (FPGA) on the same circuit board have an ESD withstand voltage of only 75 volts!! Knowing that operators can easily generate up to (and exceed) 10kV, the ESD sensitive CPLD and FPGA [5] can be partially destroyed by an operator who is simply not following proper ESD control guidelines. As ESD can occur anywhere from the receiving stage of your operations, to testing, manufacturing, shipping, and field handling of circuit boards & components, it becomes essential to study the effects of ESD so as to minimize the risk of ESD damage.

As IC manufacturers move to smaller geometries, they continue to scale the dimensions of the transistors, interconnections, and the silicon layers in their devices. This decrease results in smaller architectures for higher-speed devices that are more susceptible to breakdown damage at lower energy levels [6, 7]. Silicon layers are more likely to rupture, and metal traces are more likely to open or bridge during an ESD event [8, 9]. Most ICs are designed with limited internal ESD protection that allows them to tolerate from 1 to 2 kV pulses as per the human body model (HBM). While this is sufficient to protect the ICs during PCB assembly, it is not intended to protect the ICs when the systems are shipped to end users. Today's designer must also pay considerable attention to voltage level (clamping voltage) and how much current (residual current) will be seen by the complex electronics. While low capacitance for signal integrity is certainly important, other crucial considerations for signal integrity must be made in regards to layout, capacitance matching, and impedance matching issues.

System level ESD test [10, 11] has been conducted on the FPGA/CPLD trainer kit. The energy associated with a system level ESD strike is much higher than a device-level ESD strike. In order to protect against this excess energy, a more robust design is required. Indirect and direct air and contact discharge test has been conducted on the ALS-SDA-CPLD/FPGA Trainer Kit and the devices are found to be very ESD sensitive. ALS-SDA-CPLD/FPGA Trainer Kit is a commercially available kit. The silicon area required to design system-level ESD protection is much larger than is required for HBM or CDM. This difference in silicon area translates to additional cost for ESD protection. As technology nodes become smaller, it becomes more difficult and costly to integrate robust system-level ESD protection with microcontroller or core chipsets.

II. Programmable Devices

Complex electronics (CE) encompasses programmable and designable complex integrated circuits [12]. "Programmable" logic devices can be programmed by the user and range from simple chips to complex devices capable of being programmed on-the-fly. In the term complex electronics, the complex adjective is used to distinguish between simple devices, such as off-the-shelf ICs and logic gates, and user-creatable devices. A good rule of thumb is, if you can program or design the internal logic of the device and it has more than a few gates and connections, it is probably complex.

Some types of programmable devices are:
- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Arrays (FPGA)
- Application Specific Integrated Circuit (ASIC)
- System-on-chip (SoC)

A. Field Programmable Gate Array

Field programmable simply means that the device can be programmed by the user. An FPGA has a collection of simple, configurable logic blocks arranged in an array with interspersed switches that can rearrange the interconnections between the logic blocks. Each logic block is individually programmed to perform a logic function (such as AND, OR, XOR, etc.) and then the switches are programmed to connect the blocks so that the complete logic functions are implemented. FPGAs vary in size from tens of thousands of logic gates to over a million.

B. Complex Programmable Logic Devices

The building block of a CPLD is the macrocell, which contains logic implementing disjunctive normal form expressions and more specialized logic operations. A CPLD contains a set of simple Programmable Logic Device (PLD) blocks whose inputs and outputs are connected together by a global interconnection matrix. A CPLD has two levels of programmability: each PLD block can be programmed, and then the interconnections between the PLDs can be programmed. A key feature of the CPLD architecture is the arrangement of logic cells on the periphery of a central shared routing resource. CPLDs use EEPROM, SRAM, or Flash memory to hold the interconnect information.

The main distinction between FPGA and CPLD device architectures is that FPGAs are internally based on Look-up tables (LUTs) while CPLDs form the logic functions with sea-of-gates. The main difference between a FPGA and a CPLD is the different functional logic that is used in their design. In the CPLD, the functional logic is called PLD but the functional logic in FPGA is called complex logic block (CLB). The density and size of a CLB is much smaller compare to size and density of a PLD. But inside a FPGA, there is much more CLBs compared to the numbers of PLDs inside the CPLD. These CLBs are distributed across the entire chip and connected through the programmable interconnection.

III. Introduction To ALS-SDA-CPLD/FPGA Trainer Kit

The ALS-SDA-CPLD/FPGA trainer kit [13] is a versatile tool for experimenting with standard FPGA/CPLD with provision to mount a daughter board on the base board. The daughter board comes with various FPGA and CPLD options from XILINX and ALTERA. It also provides test pins to connect Pattern generator and Logic analyser to connect various Inputs and Outputs of the FPGA. Apart from this the base board contains various interface options to readily connect switches and displays like the key matrix, the seven segment display and the liquid crystal display as shown in the Fig. 1.

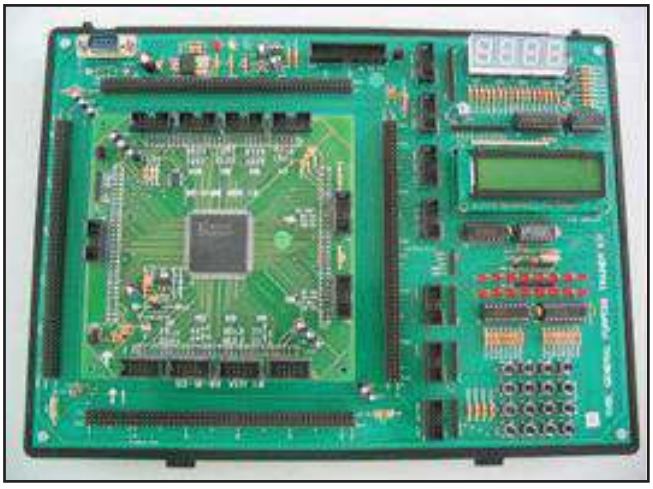

Fig. 1 ALS-SDA-CPLD/FPGA Trainer Kit

The Base Board

- Four sets of 52×3 Berg Male connectors are provided; one row lines from FPGA/CPLD, one Row to V_{CC} and one row to GND. The Berg pins for V_{CC} and GND allows a number of Experiments to be conducted, which requires these inputs. 16 outputs from output ports pin (FPGA/CPLD) are connected to Light emitting diodes (LEDs) through 10 Pin FRC connectors, 16×2 Alpha Numeric Liquid crystal display (LCD) with back-light is connected through 10 Pin FRC connectors to FPGA/CPLD port pins.
- 32 Toggle switches for I/P selection with 32 LEDs to indicate switch status
- 32 LEDs connected to output ports of the FPGA
- Two line × 16 Alpha-Numeric LCD display with back-light
- Four digit 7-segment display connected through 10 Pin FRC connectors to FPGA/CPLD port pins
- 4×4 key matrix connected through 10 Pin FRC connectors to FPGA/CPLD port pins.
- 2 nos. of Push button switches
- On board 10 MHz oscillator
- Onboard multiple DC supply voltage generator with LED indication.
- 10 MHz clock and one of four different frequency clocks (5Mhz, 1Mhz, 500Khz and 100Khz)
- Four sets of 30×2 Male Berg connectors to plug the daughter board.
- 26-pin FRC connector for connecting to standard interface boards like Stepper motor, ADC, DAC, Traffic light controller, Elevator, Printer interface etc
- Four sets of 20×2 female berg connectors to plug the child card

The FPGA Daughter Board

- XILINX XC3S50 - FPGA IC with 1 MB NVROM for stand-alone programming
- Push-button switch to re-initialize the FPGA
- Four sets of 20×2 berg connectors for plugging on to the main board
- Ten 10 Pin FRC connectors around the daughter board for connection to the on board interfaces like 7 segment LCD etc.
- JTAG connector for boundary scan programming
- Mode selection jumpers

The CPLD Daughter Board

- XILINX XC9572PC84 - CPLD IC
- Seven 10 Pin FRC connectors around the daughter
- Four sets of 20×2 berg connectors for plugging on to the main board
- JTAG connector for boundary scan programming

IV. Programming Example

The FPGA daughter board has been programmed to interface the 4×4 key matrix with the 7 segment LED display to display hex numbers, the LCD to display "ALS BANGALORE" and an external Digital to Analog

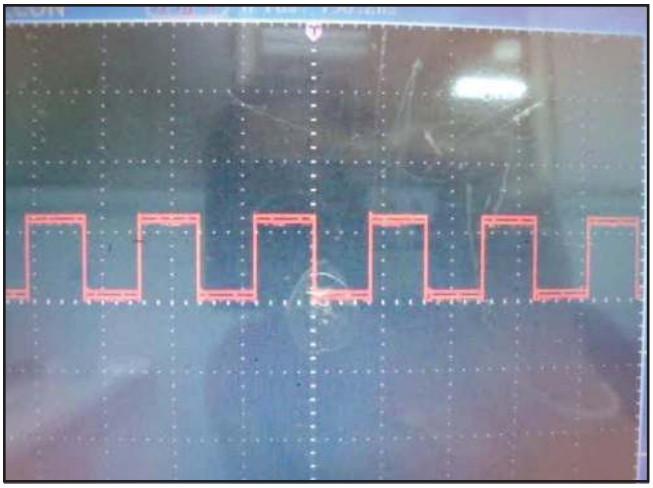

Fig. 2 Initial DAC output

converter (DAC) interface to produce square wave of amplitude 5V and frequency 10kHz as shown in Fig. 2. The CPLD daughter board has been programmed to interface an external DAC to produce square wave and display ALS on the 7 segment LED display.

V. System Level ESD Testing

A. ESD Direct Discharge on FPGA

The initial setup for the ESD testing is shown in the Fig. 3. During the ESD test the oscilloscope and power supply was placed on another table. Direct air discharge was conducted as shown in the Fig. 4 on the insulators in the kit like the seven segment display, the LCD and the FRCs and direct contact discharge on the metal points like the switches, the pins and the mounting screws as shown in Fig. 5.

B. Discharge on Liquid Crystal Display (LCD)

When an air discharge of 2kV and 4kV was applied, the LCD display which was programmed to display "ALS BANGALORE" goes blank and resets on power on. When a discharge of 8kV was applied to the LCD the letters get repeated at the time of occurrence of the discharge pulse i.e., "ALS BANGALOOORE" but resets on power on.

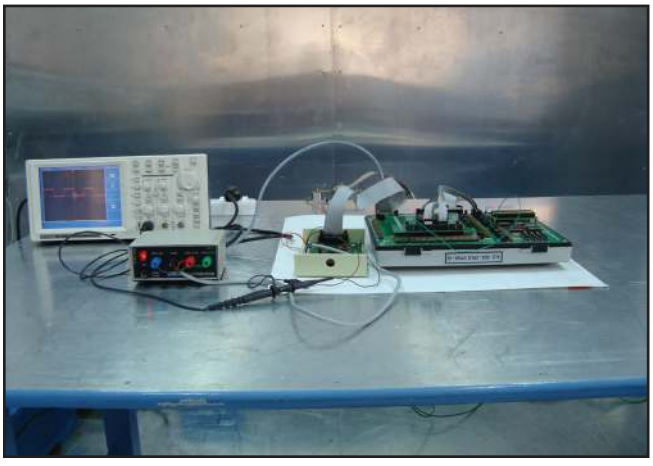

Fig. 3 Initial setup

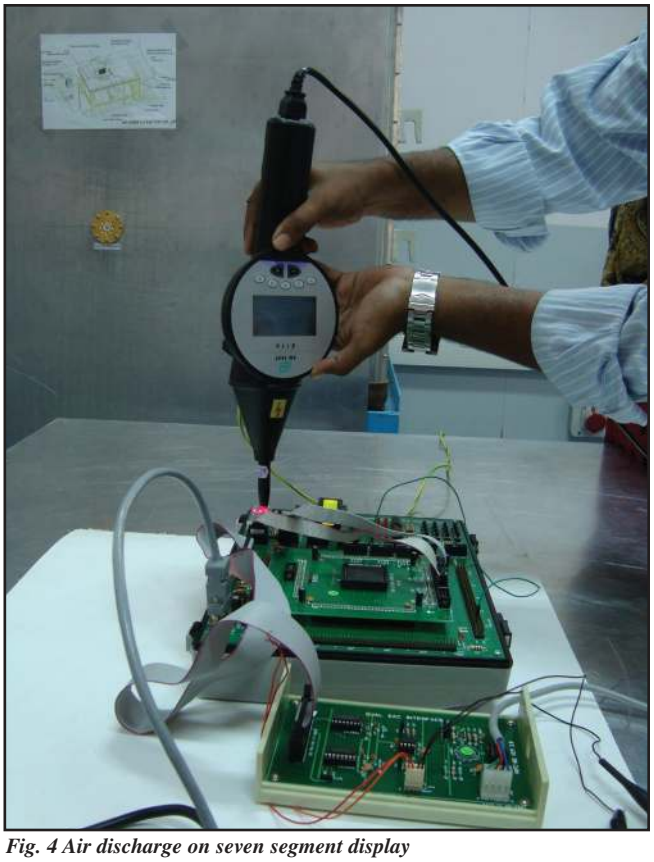

Fig. 4 Air discharge on seven segment display

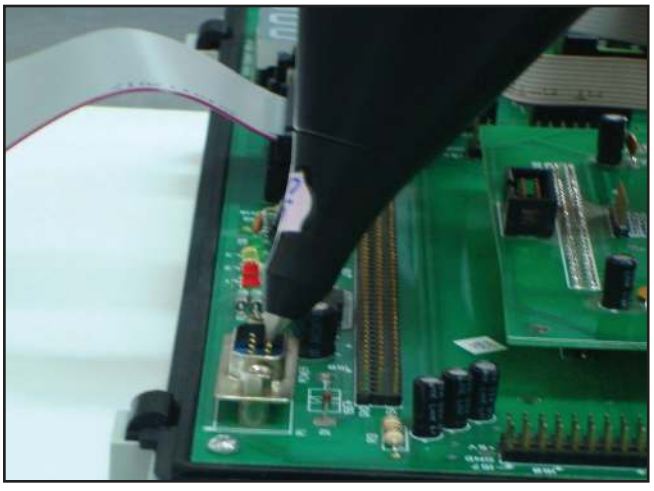

Fig. 5 Contact discharge on DB9 connector

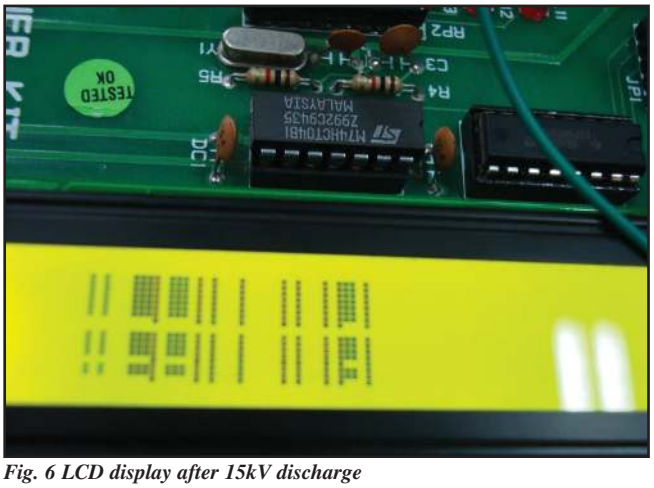

Fig. 6 LCD display after 15kV discharge

An air discharge of 15kV permanently damages the data on the Liquid Crystal Display (LCD), some random lines are seen and the data is not restored on reset as shown in the Fig. 6. A contact discharge of 15kV on the mount hole of the LCD completely damaged the LCD.

C. Discharge On Seven Segment LED Display

The seven segment LED display was programmed along with the 4×4 key matrix shown in Fig. 7 to display from '0' to 'F' according to the key pressed. For an air discharge of 2kV and 4kV no effect was observed.

When an air discharge of 8kV was given to the seven segment display it would reset to 0 every time the discharge was picked. At the time of discharge one of the segments remained off momentarily. When another discharge was applied at 15kV, the seven segment LED display permanently remained at zero. After power on reset the seven segment display was working fine.

For a contact discharge of 2kV and 4kV on the keys no effect of ESD was observed. For a contact discharge of 8kV on the first key, Zero remained intact but instead of displaying 1, 2 and 3 it was displaying 4 and instead of 5, 6 and 7 it was displaying 8 and instead of 9, A and B it was displaying C and also for D, E, F it was displaying zero when the respective keys were pressed after the discharge. The hex keys displayed the wrong output even on reset.

D. Discharge on the FRC

When air discharge of 2kV was given on the DAC FRC no effect was observed. For a 4kV air discharge small transients were seen in the DAC output. For an 8kV air discharge on the FRC connected to seven segment data had no impact on the seven segment output but DAC output had transients. When the 8kV air discharge was given on the DAC FRC huge transients were observed in the DAC output as shown in the Fig. 8.

When 15kV discharge was given on DAC FRC, initially large transients were observed in the DAC output and the amplitude of the DAC output became zero, then recovered to half of its initial value and finally recovered back to original value of 5V as shown in the Fig. 9. When 15kV air discharge was given on the FRC connected to the seven segment display, one of the segments in the display momentarily turned off.

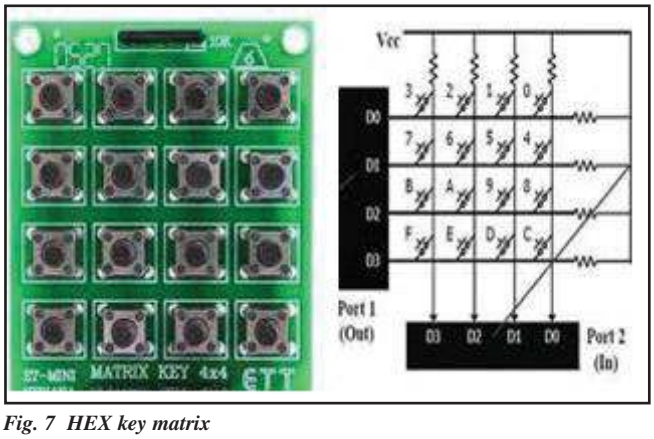

Fig. 7 HEX key matrix

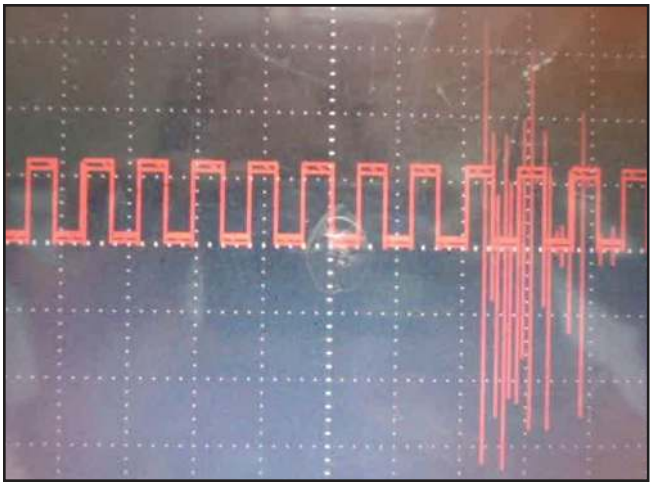

Fig. 8 DAC output for a 8kV discharge

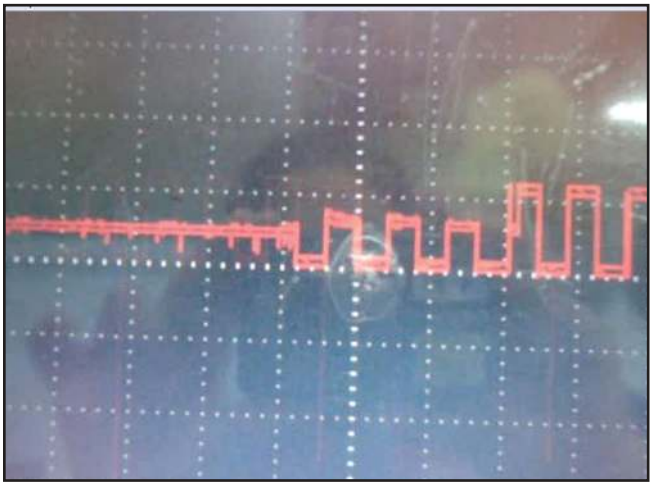

Fig. 9 DAC output for 15kV discharge on FRC

E. Discharge on the Input Pins and Connector Pins

When a discharge of 2kV was given to pin 190 (a0) the DAC output voltage reduced to half of its original value as shown in the Fig. 10 and when the discharge was given to pin 187 the DAC output voltage further reduced. When 2kV discharge was given on the DB9 connector pins no effect was observed.

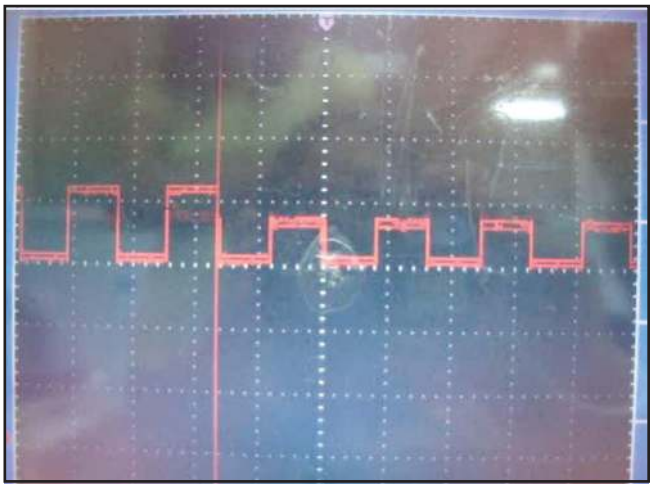

Fig. 10 DAC output when 2kV was given to pin 190

Table 1 : Susceptibility Levels of FPGA Module

Sl. No.	Test Level	Test point	Failure Symptom
1.	2kV and 4kV air discharge	Liquid crystal Display	Display goes blank but resets to normal on power ON
	8kV air discharge		Display letters are repeated but resets to normal on power ON
	15kV air discharge		Random lines are displayed and display is not restored to normal on power ON
	15kV air discharge	LCD mount hole	Effect observed: LCD completely damaged
2.	2kV and 4kV air discharge	Seven segment LED display	No effect
	8kV air discharge		Reset to Zero every time discharged
	15kV air discharge		At discharge Zero is displayed continuously and display is restored to normal on power ON
3.	2kV air discharge	Flat Ribbon Cable connected to seven segment LED display and DAC module	No effect
	4kV air discharge		Small transients seen in DAC output
	8kV air discharge		Large transients seen in DAC output
	15kV air discharge		Large transients, At discharge DAC output becomes LOW One of the segments of LED turned OFF momentarily during discharge
4.	2kV contact discharge	Hex Key Matrix	No effect
	4kV contact discharge		Wrong output data
	8kV contact discharge		Wrong output data. Latency observed - displayed only ZERO when any key is pressed
5.	2 kV contact discharge	Input pin 190	DAC output reduced
		Input pin 180	DAC output further reduced
		Input pin 187	Shorted adjacent pins (pin 186-GND and pin 188-Vcc) Effect observed: FPGA IC damaged
6.	2 kV contact discharge	DB9 connector pins	No effect

Table 2 : Susceptibility Levels of CPLD Module

Sl. No.	Test Level	Test point	Failure Symptom
1.	2kV and 4kV air discharge	Seven segment LED display	No effect
	8kV air discharge		Reset to Zero every time discharged
	15kV air discharge		At discharge Zero is displayed continuously and display is restored to normal on power ON
2.	2kV air discharge	Flat Ribbon Cable connected to seven segment LED display and DAC module	No effect
	4kV air discharge		Small transients seen in DAC output
	8kV air discharge		Large transients seen in DAC output
	15kV air discharge		Large transients, At discharge DAC output remained HIGH but reset to normal on power ON One of the segments of LED turned OFF momentarily during discharge
3.	No contact discharge test conducted		When FPGA module was replaced with CPLD module, there was no DAC output Effect observed: CPLD IC damaged due to stored charges from the damaged power supply capacitor

F. Direct Discharge on CPLD

Air discharge tests on the kit with CPLD module were conducted before the contact discharge tests on the kit with FPGA module. When an air discharge of 2kV was given to the seven segment display and on the DAC FRC no effect was observed. For an air discharge of 4kV on the seven segment display no effect was observed and when discharged on DAC FRC small transients were observed in the DAC output. For an air discharge of 8kV on the FRC for seven segment header, there was no impact on the seven segment output but DAC output had transients. When the 8kV discharge was given on the DAC FRC huge transients were observed in the DAC output. When 15kV discharge was given on DAC FRC and on seven segment header FRC, large transients were observed in the DAC output. For an air discharge of 15kV the DAC output remained at constant high and it resets on power on.

However there was no output waveform observed at the DAC module when we changed from the FPGA module to CPLD module for performing the contact discharge tests. Contact discharge tests were not conducted on the CPLD module as the base board was affected during the FPGA test.

VI. Post Discharge Effects

A. Post Discharge Effects on Dual DAC

There were no discharge tests done on the dual DAC module. Only direct air discharge was carried out on the FRC cables connected to the DAC module. Also direct contact discharge was given to Input/ Output pins 190 and 187 during the FPGA test where the output of the dual DAC was observed. The DAC module is connected to the mother board housing the FPGA/CPLD daughter board. When the dual DAC module is analysed after these discharges it is found that for the DAC IC which was not used to observe the output during discharge the peak voltage had come down from 5V to 3.7V and for the DAC IC which was used to observe the output during discharge the output voltage had reduced from 5V to 2.4V and both the IC's had a dc offset of 0.4V. After two days the latency effects further reduced the DAC output to 0.14 V. The DAC output for the ideal case is a graph of Voltage versus Time with a linear increase and uniform slope for a ramp wave output as shown in Fig. 11. But after the discharge the output was in the form of staircase waveform as shown in the Fig. 12 for the IC which was not programmed which tells us that the filter circuits used to get the uniform slope must have stopped working after the discharge. The output of the DAC IC which was programmed and after the discharge was tested for a ramp waveform whose output looked as shown in the Fig. 13.

When both the DAC IC's in the module were replaced with new IC's the dual DAC was working fine which implied that the opamp in the dual DAC module was functioning fine after the discharge and the DAC output voltage now changed from 0.14V to 5V confirming damage of the earlier ICs on the module.

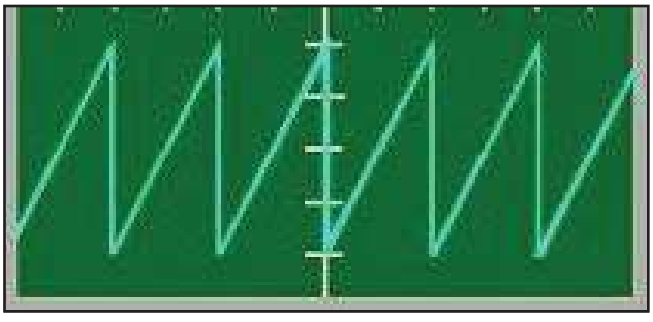

Fig. 11 DAC output before discharge

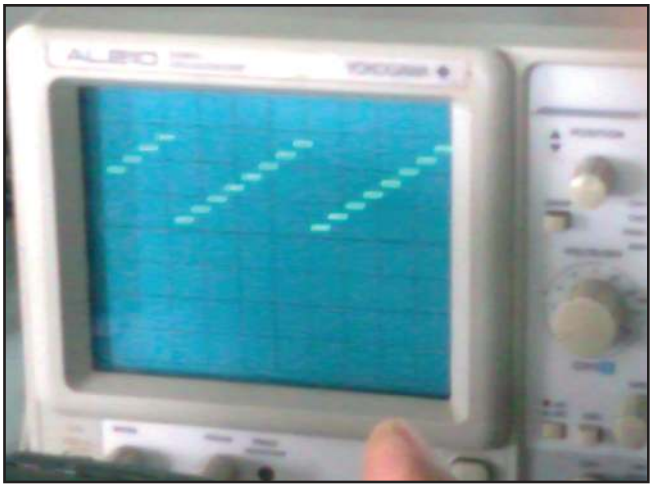

Fig. 12 The output of the not used DAC IC after discharge

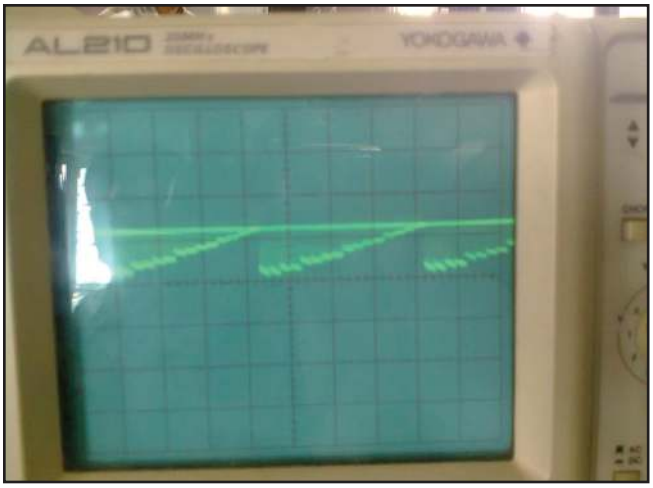

Fig. 13 The output of the used DAC IC after discharge

B. Post Discharge Effects on CPLD

The CPLD board did not go through the contact discharge test and since it did not offer any DAC output, the CPLD daughter board was reprogrammed so as to confirm if any discharge had affected the CPLD module. The DAC output voltage was observed to be 3V after reprogramming but the ground reference level had shifted to 2.5V instead of being at 0V. Some amount of damage has occurred after we have replaced the FPGA daughter board with the CPLD daughter board for conducting the contact discharge test. When the CPLD was reprogrammed for the second time the DAC output showed 5V with a dc offset of 0.4V. When reprogrammed the second time the program was now being assigned to different macro cells. Hence earlier when the affected macro cells were assigned the output was also affected. This implied that the code used to program DAC was also corrupted after the discharge. The seven segment display was working fine before and after reprogramming. The latency effects must have further damaged the CPLD IC because when the entire trainer kit was sent to the company for repair they reported that the CPLD IC was damaged and needed to be replaced.

C. Post Discharge Effects on FPGA

The latency effects came into picture after the initial discharge. After a day when the display is tested the seven segment display always displays a zero upon pressing any key in the key matrix. The LCD is completely spoilt. The DAC output is at zero voltage. When reprogrammed the code gets successfully loaded on to the FPGA board but the DAC, seven segment display, keypad and LCD are not functioning. Hence the FPGA3s50 daughter board is not working properly and when sent for repair the company confirmed that the FPGA IC is damaged. But the mother board is working fine as it could be used for reprogramming the daughter boards.

D. Discharge Effect on the power supply

The power supply was connected to the trainer kit and the DAC module was connected to the trainer kit through 26 pin FRC. There was no discharge done on the power supply but after the ESD testing was carried out the SMPS power supply which was used to

power up the trainer kit was not functioning properly. Two days later, the post discharge tests needed to be conducted and when the DAC output was connected to the CRO probes, the fuse of the power supply blew. Upon analysing the ALS PS11 power supply it was known that the 0.001µF, 1kV ceramic capacitor placed between tny268 IC and transformer was malfunctioning. Once this capacitor was replaced the power supply was functioning properly.

VII. Failure Analysis of the Damaged ICS

The post discharge effects revealed that the FPGA 3s50 IC [14] and CPLD 9572 IC [15] were damaged and when these two were replaced then the FPGA and CPLD daughter board were functioning well. So the integrated circuits were sent for decapping and the failure mechanisms were investigated. The full view of the damaged decapped FPGA 3s50 IC and CPLD 9572 IC are shown in Fig. 14 and Fig. 15.

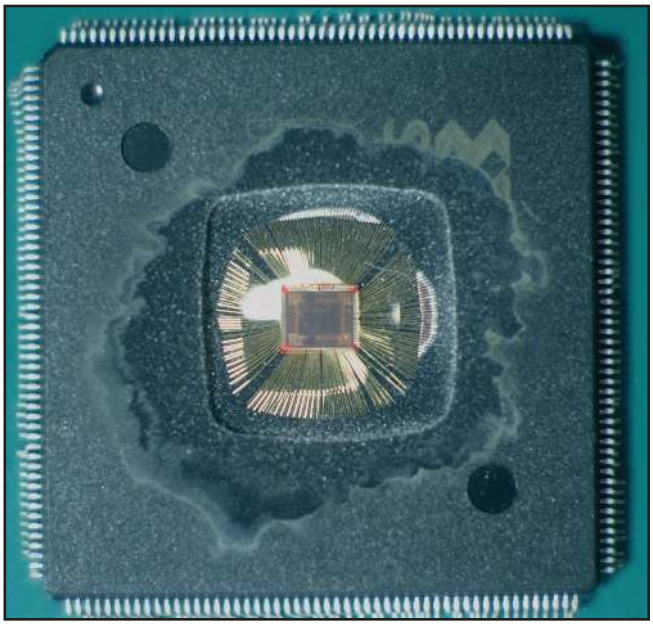

Fig. 14 Full view of FPGA 3s50 IC

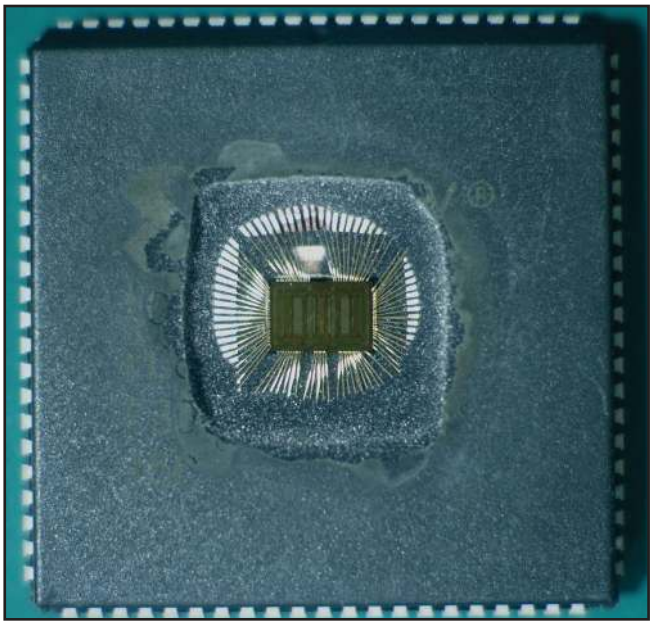

Fig. 15 Full view of CPLD 9572 IC

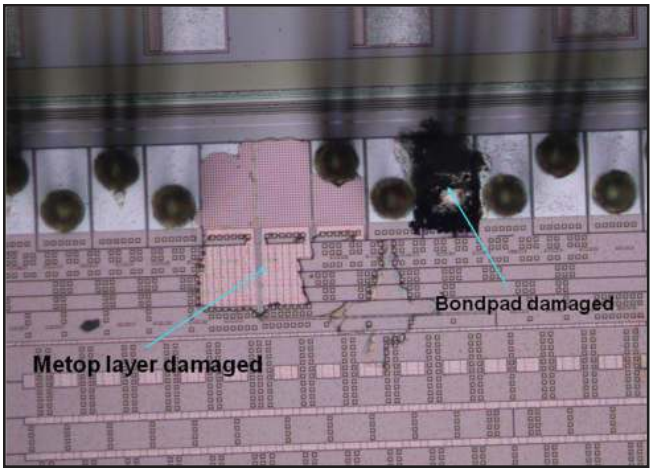

Fig. 16 Optical micrograph of the failure of FPGA 3s50 IC

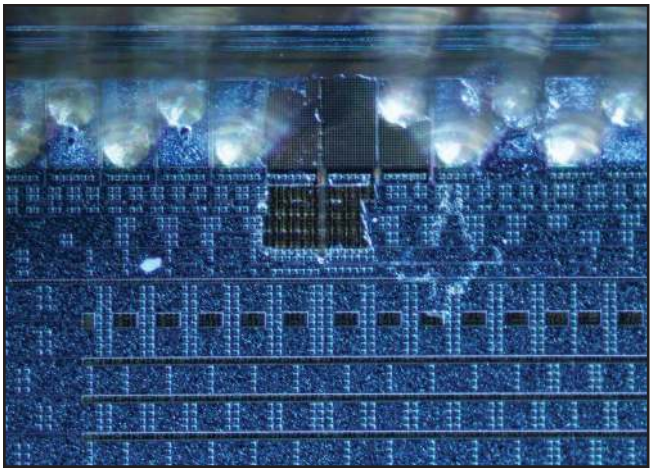

Fig. 17 Dark field image of the damaged FPGA 3s50 IC

The contact discharge of 2kV to pin 187 has shorted the adjacent pins which are pin 186 (GND) and pin 188 (Vcc) and this discharge has gone to the SMPS power supply and damaged the 0.001µF/1kV capacitor and the discharge in turn has taken a return path through pin 179 (GND) to pin 180 (I/O) of the FPGA 3s50 IC resulting in the bond pad of pin 180 being damaged and the ESD transient discharge has also damaged the inner layers of the IC. This is shown in Fig. 16. The ESD discharge has also gone through pin 186 (GND) to the pin 185 (I/O/Vref) and has damaged the metal top layer. This ESD discharge back to the FPGA IC has come from the damaged capacitor from the power supply. The dark field image shown in Fig. 17 accentuates the metal top layer damage.

Failure analysis of the CPLD 9572 IC shown in Fig. 18 revealed that there was oxide break down near pin 6 and pin 7 in the CPLD 9572 IC which was the reason the CPLD module was not functioning. There was no direct ESD test performed on the CPLD module. The damage to the CPLD 9572 IC may have been due to the stored charges from the damaged capacitor of the power supply. These stored charges may have found a path to CPLD IC and damaged it when the FPGA module was being replaced by CPLD module.

Mitigation techniques were not proposed to the FPGA/CPLD kit used as it was a commercial available product and we did not have access to the schematics and line diagrams of this kit. However based on the ESD test on self designed and custom built 32 bit microcontroller board with interfaces such as Liquid crystal

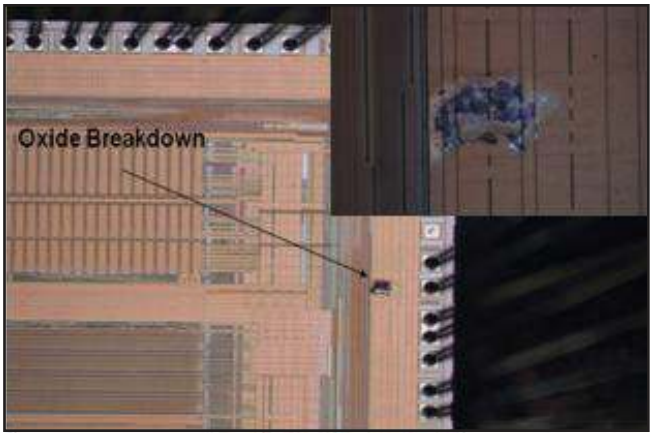

Fig. 18 Optical micrograph of the failure of CPLD 9572 IC

display, switch matrix, UART and audio processor, it is necessary to use TVS diodes at the LCD data input points and the input point of the key matrix. TVS diodes UCLAMP3301D used had a standoff voltage VR of 3.3V, clamping voltage VC of 9.5V and peak pulse current IPP of 10A and LCD display with these TVS diodes could withstand an air discharge of 15kV with minor upsets.

Most of the IO pins accessible to user are always covered by metal shell which takes care of incoming ESD. A contact discharge of 2kV (which is minimum test level) on I/O pins was carried out to assess whether any protection is needed in case of ESD discharge to the pins. The failure analysis of the FPGA/CPLD ICs reveals that it is important to provide for mitigation techniques at off chip or on-board level. It becomes necessary to have TVS diodes at input/output points of the complex electronics ICs and also necessary to provide power supply decoupling by using decoupling capacitors at all Vcc points and also use Ferrite beads in series with the supply line to provide for complete board level protection to the FPGA/CPLD ICs.

VIII. Conclusion

An air discharge of 8 kV on the Liquid Crystal Display distorts the data but resets on Power ON and an air discharge of 15kV damages the data which cannot be restored on reset. The LCD display used in this setup can withstand only a maximum of 8kV air discharge voltage. An air discharge of 2 kV and 4 kV has no effect whereas an air discharge of 8 kV and 15 kV distorted the output on the seven segment display but the display resets on power ON. The seven segment LED display can withstand the stress voltages defined as per the IEC standard. A contact discharge of 2 kV and 4kV on the keys feeding the data to seven segment display has no effect but a contact discharge of 8 kV spoilt the keys which distorted the display data. The Hex key matrix is damaged by 8kV contact discharge.

Huge transients are observed when air discharge is carried out on the FRC cables connected to the DAC module. Because of the ESD discharge in the surrounding and the pins of the VHDL kit, the ceramic capacitor in the SMPS power supply connected to the kit is found to be affected. This was an after-effect observed. This capacitor may also have been affected by the contact discharge on the input/output pins. It turns out that the ESD event found a path through this affected capacitor and damaged the FPGA and CPLD ICs.

When a contact discharge of 2 kV was given on the input pins of the mother baseboard the DAC output voltage reduced. The FPGA 3s50 IC was affected during this contact discharge. There was damage to the bond pad as well as the metal top layer was damaged. The DAC ICs are affected during the contact discharge on I/O pins and air discharge on FRC cables. CPLD 9572 IC is also affected by the discharge from the affected power supply capacitor during the FPGA discharge test. There is dielectric breakdown damage observed in CPLD 9572 IC.

It is observed that the FPGA module which is damaged by ESD has created a defect in the power supply that resulted in an immediately observable failure in the CPLD module as well as change in the part performance. It is also possible that such an event has created latent damage that would worsen with time, such as a metal open or short, or a gate oxide defect. However, ESD damage is currently seen in the I/O pin bond pad damage, damage of the metatop layer in FPGA IC and dielectric breakdown in CPLD IC.

It can be concluded that the Field Programmable Gate Arrays and Complex Programmable Logic Devices are found to be highly susceptible to ESD and protection design needs to be looked into based on the ESD effects reported. FPGA 3s50 IC is affected during the contact discharge to the input pin. There is damage to the bond pad as well as the metal top layer is damaged. There is dielectric breakdown damage observed in CPLD 9572 IC. The DAC ICs are also affected during the ESD discharge.

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X. Acknowledgement

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XI. Biographies

Rajashree Narendra *completed her Bachelors degree in Electronics and Communication Engineering from University of Mysore, India in 1988 and Masters degree in the area of Optical Fiber Communication at University of Alberta, Edmonton, Canada in 1992. She is currently persuing her Doctoral program in the area of EMI/EMC in Electronics and Communication Engineering at UVCE, Bangalore University, India.*

Major field of study is Integrated Optical Devices, Electrostatic discharge and EMI/EMC. She has about 24 years of research and teaching experience. She worked as a Research Engineer at TR Laboratories, Edmonton, Canada. She worked as Scientist at CEERI, CSIR Labs, Pilani, India. She is currently Professor and Head, Department of Telecommunication, BNM Institute of Technology, Bangalore. She has published and presented papers in IEEE Transactions, Photonics Technology Letters, SPIE, IEEE–LEOS International Conference, Saratov Fall Meet at Russia, Asia Pacific Symposium on EMC, China, PIERS–KL,Malaysia, IEEE AEMC-Kolkata and INCEMIC-Bangalore.

Dr. M.L. Sudheer *received his BE degree in Electrical Engineering from UVCE, Bangalore University in 1980 & M.Tech in Industrial Electronics from NIT-K, Suratkal and Ph.D from CEDT, Indian Institute of Science, Bangalore in 2000. He is presently working as Professor in the Department of Electronics & Communication, UVCE, Bangalore University, India.*

His research interests are Electromagnetic Interference (EMI) & Electromagnetic compatibility (EMC), Power Electronics and Low voltage Transients. He has published papers in conferences and journals.

Dr D.C. Pande *received his Ph.D. in 1982 from University of Allahabad. Since November 1981, he is with LRDE, where he is involved in Design & Development of Electromagnetic Interference Control Techniques for Ground Based, Airborne and Shipborne equipments and systems. He is one of the pioneer scientists who had started research activities in the field of NEMP and High Power Microwave (HPM) in India.*

Presently he is involved in design, development and evaluation of various types of antennas for different Radar programs. He is a founder Life Member of SEMCE (I); at present he is the Chairman of the Society. He was a member for the Department of Electronics Committee for evolving National Standards regarding Electromagnetic Emissions. He was awarded Certificate of Achievements by SUMMA Foundation, USA, Commendable Certificate by IGMDP Program in 1990, Megha Nath Saha Memorial Award of IETE in 1994, EMC Engineer of the Year 1998 of SEMCE (I) and Lab Scientist of the Year 2003 by DRDO, National Science Day Award 2004 and DRDO Scientist of the Year Award 2005. Presently he is Scientist H, Outstanding Scientist and Director (Technologies) in Electronics and Radar Development Establishment.