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# Effect of Grain Boundary Protrusion on Electrical Performance of Low Temperature Polycrystalline Silicon Thin Film Transistors

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**ABSTRACT** We studied the impact of grain boundary (GB) protrusion on the electrical properties of low temperature polycrystalline silicon thin film transistors. The analysis of atomic force microscopy and transmission electron microscopy images indicate the grain size of ∼350 nm and a protrusion height of ∼35 nm. The transfer and output characteristics are well fitted by technology computer-aided design using two different density of states for poly-Si grain and GB, respectively. From 2-D contour mapping, a drastic reduction of hole concentration ($\sim 5 \times 10^{16}$ cm$^{-3}$) at GB protrusion site was obtained as compared to the grain ($\sim 3 \times 10^{18}$ cm$^{-3}$). Trapping concentration at GB is much higher, which leads to the reduction in the mobility.

**INDEX TERMS** Low temperature polycrystalline silicon (LTPS), thin-film transistors (TFTs), technology computer-aided design (TCAD).

## I. INTRODUCTION

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been widely used for pixel switching and driving TFTs of active-matrix organic light emitting diode (AMOLED) displays [1]. When compared to a-Si, oxide and organic TFTs, LTPS TFTs are the best choice for high-speed CMOS circuits because of higher mobility ($\mu_{FE}$ : 40∼100 $cm^2/V \cdot s$) and excellent stability [2]–[4]. Despite of many advantages of excimer laser annealing (ELA) LTPS TFTs, the process complexity, smaller grain size (100 ∼ 500 nm), GB protrusion, high manufacturing cost are the main issues to overcome [5]–[8].

Several groups reported the numerical simulations of LTPS TFTs including grain size variation [9], GB position dependency inside the semiconductor layer [10], and electric field/carrier concentration simulation without taking account of the protrusion [5]. It is highly important to estimate the amount of charge trapping at GB region while extending the GB height towards protrusion peak, however, there is no report on such an important phenomenon.

In this paper, we systematically investigated the effect of GB protrusion on the electrical performance of LTPS TFTs. We measured the grain and protrusion dimension by atomic force microscopy (AFM) and transmission electron microscopy (TEM) micrographs. Based on technology computer-aided design (TCAD) simulation, we realized the exact TFT dimension and fitted the experimental I-V characteristics using the density of states (DOS) model. A drastically reduced carrier concentration ($\sim 5 \times 10^{16}$ $cm^{-3}$) had been found at GB protrusion region by contour mapping which might be due to carrier trapping at GBs.

## II. FABRICATION AND EXPERIMENT

Fig. 1 (a)-(b) shows the schematic cross-sectional view and optical image of the fabricated LTPS TFTs on glass. The fabrication process of the p-channel LTPS TFT is as follows: First, a stack buffer layer of 260 nm $SiO_2$ and

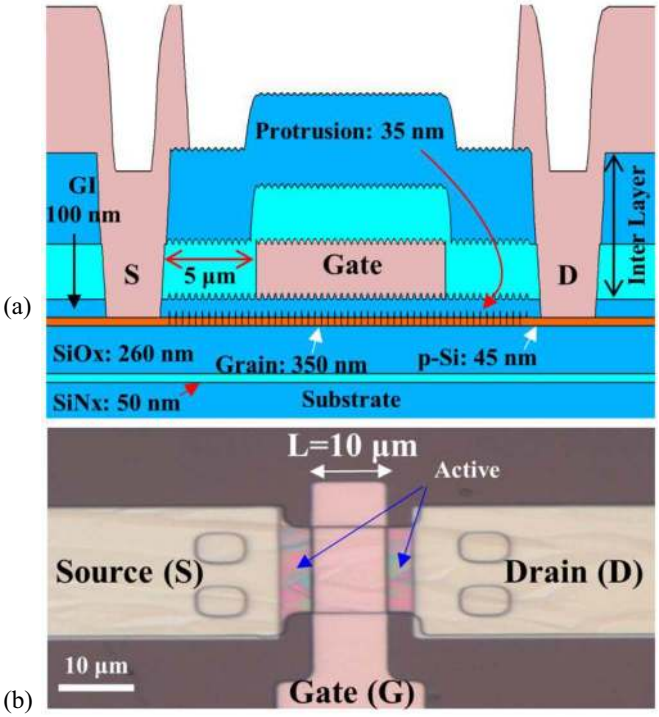


**FIGURE 1.** **(a) Schematic cross section of a LTPS TFT by excimer laser annealing (ELA) process. (b) Optical image of the fabricated TFT with channel length (L) of 10 μm and channel width (W) of 40 μm, respectively.**

50 nm $SiN_X$ was deposited by plasma enhanced chemical vapor deposition (PECVD) at 450°C, followed by 45 nm a-Si deposition by PECVD at 420°C and subsequent dehydrogenation. The a-Si layer was crystallized by ELA and patterned to form active islands. A 100 nm thick $SiO_2$ layer was deposited as the gate insulator (GI) by PECVD at 360°C. A 300 nm chromium (Cr) gate electrode was deposited by physical vapor deposition (PVD). The gate metal and GI layers were patterned, followed by the $p^+$ implantation at source/drain (S/D) region. The activation of dopant was performed at 360°C in vacuum for 1 h. An interlayer dielectric (ILD) of $SiN_X/SiO_2$ stack layer of 300 nm / 300 nm was deposited by PECVD at 360°C, followed by the via hole opening process for S/D contacts. A thermal activation was performed in vacuum at 425°C for 1 h after the deposition of 250 nm thick Cr layer by PVD as S/D electrodes.

The electrical characteristics of the fabricated TFTs were measured at room temperature using an Agilent 4156C semiconductor analyzer. The TFT field effect mobility ($\mu_{FE}$) was obtained from the transconductance ($\partial I_D/\partial V_G$), where $I_D$ is the drain current and $V_G$ represents gate bias. The threshold voltage ($V_{Th}$) was obtained as the $V_G$ from giving the constant $I_D$ of W/L×100 pA at drain bias ($V_D$) = −0.1V. The subthreshold swing, SS was taken as $(\partial Log I_D/\partial V_G)^{-1}$ over the range of 100 pA ≤ $I_D$ ≤ 1 nA, with $V_D = -0.1$V. The fabricated TFT has W/L of 40 $\mu$m/10 $\mu$m.

**TABLE 1.** **TCAD DOS parameters for simulation.**

| No. | Material and Device Properties | Symbol/value/unit | | |
|---|---|---|---|---|
| 1. | Thickness of Polycrystalline silicon | $t_{ACT}$ | 45 | nm |
| 2. | Bandgap of silicon at 300 K | $E_g$ | 1.1 | eV |
| 3. | Dielectric Constant of gate insulator | | 3.9 | |
| 4. | Thickness of gate insulator (GI) | $t_{GI}$ | 100 | |
| 5. | Lateral grain size | $L_{Grain}$ | 350 | nm |
| 6. | Lateral grain boundary (GB) size | $L_{GB}$ | 1 | |
| 7. | Source/Drain (S/D) doping density | | $10^{20}$ | $cm^{-3}$ |
| 8. | Field effect mobility (PMOS, hole) | $\mu_{FE}$ | 70 | $cm^2/V \cdot s$ |
| 9. | Protrusion height | $H_P$ | 35 | nm |
| 10. | TFT channel width/length | W/L | 40/10 | μm/ μm |
| | **Density of States (DOS) for Grain** | | | |
| 11. | Density of donor-like tail states | $N_{TD}$ | $3 \times 10^{18}$ | $cm^{-3}eV^{-1}$ |
| 12. | Density of acceptor-like tail states | $N_{TA}$ | $5 \times 10^{19}$ | |
| 13. | Density of donor-like Gaussian states | $N_{GD}$ | $2 \times 10^{17}$ | |
| 14. | Density of acceptor-like Gaussian states | $N_{GA}$ | $8 \times 10^{16}$ | |
| 15. | Slope of donor-like tail states | $W_{TD}$ | 0.30 | $eV^{-1}$ |
| 16. | Slope of acceptor-like tail states | $W_{TA}$ | 0.015 | |
| 17. | Width of donor-like Gaussian states | $W_{GD}$ | 0.13 | |
| 18. | Width of acceptor-like Gaussian states | $W_{GA}$ | 0.30 | |
| 19. | Peak energy position of donor-like Gaussian states | $E_{GD}$ | 0.3 | $eV$ |
| 20. | Peak energy position of acceptor-like Gaussian states | $E_{GA}$ | 0.8 | |
| | **Density of States (DOS) for Grain Boundary (GB)** | | | |
| 21. | Density of donor-like tail states | $N_{TD}$ | $6 \times 10^{19}$ | $cm^{-3}eV^{-1}$ |
| 22. | Density of acceptor-like tail states | $N_{TA}$ | $1 \times 10^{20}$ | |
| 23. | Density of donor-like Gaussian states | $N_{GD}$ | $5 \times 10^{17}$ | |
| 24. | Density of acceptor-like Gaussian states | $N_{GA}$ | $2 \times 10^{17}$ | |
| 25. | Slope of donor-like tail states | $W_{TD}$ | 0.50 | $eV^{-1}$ |
| 26. | Slope of acceptor-like tail states | $W_{TA}$ | 0.03 | |
| 27. | Width of donor-like Gaussian states | $W_{GD}$ | 0.33 | |
| 28. | Width of acceptor-like Gaussian states | $W_{GA}$ | 0.35 | |
| 29. | Peak energy position of donor-like Gaussian states | $E_{GD}$ | 0.4 | $eV$ |
| 30. | Peak energy position of acceptor-like Gaussian states | $E_{GA}$ | 0.8 | |

Numerical simulation of LTPS TFT was performed by TCAD from Silvaco [11]. The representing device parameters were obtained from optical micrographs. The density of states (DOS, $cm^{-3}eV^{-1}$) in the gap was adopted independently for both the poly-Si grain and GB in order to fit the experimental I-V data. The summary for LTPS TFT simulation parameters are shown in TABLE-1.

## III. PROTRUSION IN LTPS TFT

Fig. 2 (a) shows the atomic force microscopy (AFM) image of ELA poly-Si layer over an area of 2 ×2 μm$^2$. Sequential formation of poly-Si grain has been found with an average grain size of ∼350 nm. The transmission electron microscopy (TEM) image in Fig. 2(b) shows the poly-Si layer with surface protrusion height of ∼35 nm. The total height of the poly-Si layer at grain boundary (GB) regions is ∼80 nm with 45 nm poly-Si in the grain.

The formation of protrusion is due to the difference in mass densities between liquid and solid silicon. This induces the formation of protrusion at the GB during the cooling process to form poly-Si after laser crystallization [12]. This difference in silicon density by phase transformation accumulates liquid silicon in the last solidified area which

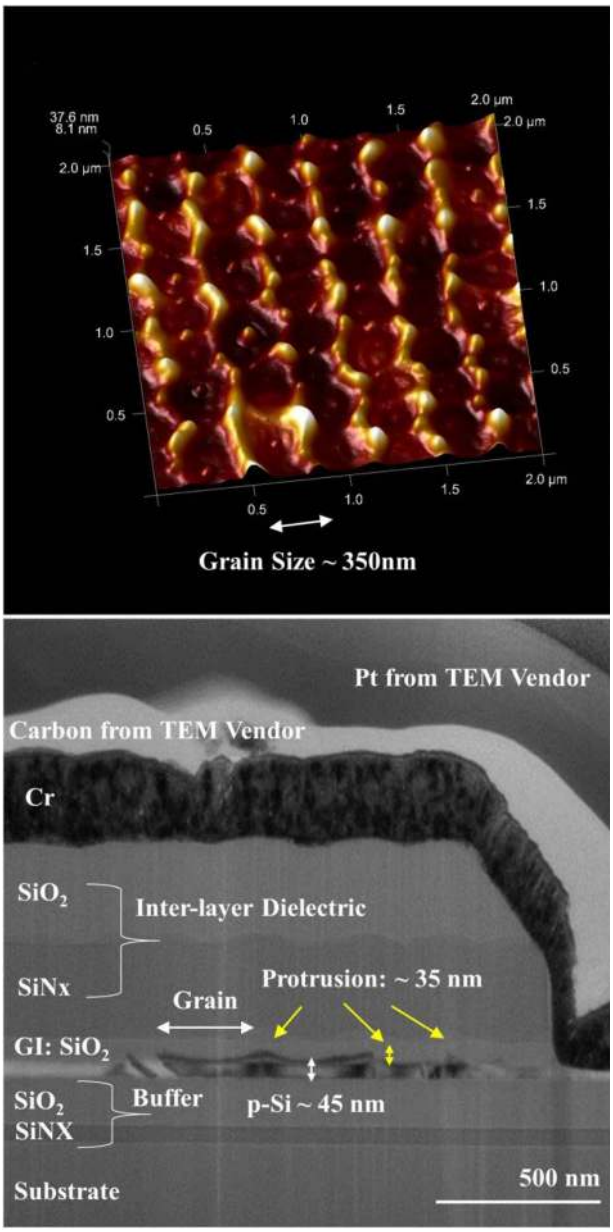


**FIGURE 2. (a) AFM image of ELA poly-Si surface and (b) TEM cross-sectional view of a LTPS TFT. The size of grain and height of protrusion are ~350 nm and 35 nm, respectively.**

results in the formation of redundant uprising silicon volume (protrusion) at GB regions [13]. High surface roughness as a result of protrusion at GB regions is an inherent problem of laser-based crystallization of poly-Si film [6].

There are several reports describing the impacts of GB protrusion on the electrical performance of poly-Si TFTs. Protrusion results in poor device performance, uniformity and reliability issues because of high surface roughness. This is dominant when scaling of channel length and gate insulator of LTPS TFT for high pixel density display applications [13]. Chen *et al.* reported the mechanical bending stress effect on flexible ELA LTPS TFTs [12]. A non-uniform stress distribution due to protrusion had been reported near poly-Si/GI interface and this phenomenon is more pronounced near GB protrusion [12]. The defect/trapping model is used to explain the TFT performance/reliability degradation, which is related to the protrusion in ELA LTPS TFTs [12]. A systematic study on the effect of GB protrusion on the electrical performance using the density of states modeling for grain and GB is highly required, especially for the displays using short channel TFTs.

A possible alternative approach to overcome protrusion effect is the planarization process but the additional polishing process is needed [13]. To get flattened poly-Si surface, chemical mechanical polishing (CMP) after the ELA process is the most widely adopted one [6], [14]–[15]. CMP reduces the surface roughness to ~30 Å, however, this process is not suitable for the large glass substrate. Therefore, a-Si TFTs and metal oxide semiconductor TFTs are the most popular choices for large size glass substrate process for displays [16]–[17]. It has been identified that the laser energy intensity plays the vital role in the formation of the protrusion and the increase of laser energy for crystallization results in a taller protrusion on the GB [12]. Another alternative approach is to increase the grain size (less number of GB, and hence, less number of protrusion peaks) for better transistor performance, and the relationship between grain size and protrusion height had been demonstrated [6]. Blue laser annealing (BLA) can be one of the most suitable alternatives where the grain size can be over 10 μm and hence, channel length scaling over several micron ranges can be possible without having GB/protrusion inside the TFT channel with $\mu_{FE}$ over 100 $cm^2/\mathrm{V}\cdot\mathrm{s}$ [18].

## IV. DENSITY OF STATES (DOS)

Fig. 3(a)-(b) shows the transfer and output characteristics of the fabricated ELA LTPS TFT, respectively. The solid lines are the experimental data for the TFTs with channel dimensions, W/L of 40 μm / 10 μm and dashed lines are the TCAD fitting using the density of states (DOS) model for both the grain and GB. A good fitting has been observed. The electrical characteristics include $\mu_{FE} = 67.6\ cm^2/\mathrm{V}\cdot\mathrm{s}$, $V_{Th}(\mathrm{V}) = -4.5$ V, and SS = 0.46 V/dec.

Transfer characteristics of the fabricated TFTs exhibited large leakage current/off current under reverse bias at higher $V_D$ which might be attributed to the field-enhanced leakage current phenomenon and might be associated to band-to-band tunneling (BBT) via GB trapping states near the drain electrode [19]–[21]. By implementing BBT model parameters with Poole-Frenkel effect [22] in the TCAD simulation, the fitting I-V curves exhibited the similar experimental off current trend. Moreover, the output characteristics of the fabricated TFTs exhibited small kink effect at higher $V_D$ which might be originated by impact ionization at the drain end of the poly-Si channel due to the large drain field when the device is operating in saturation [23]–[24]. By implementing impact ionization model parameters in the

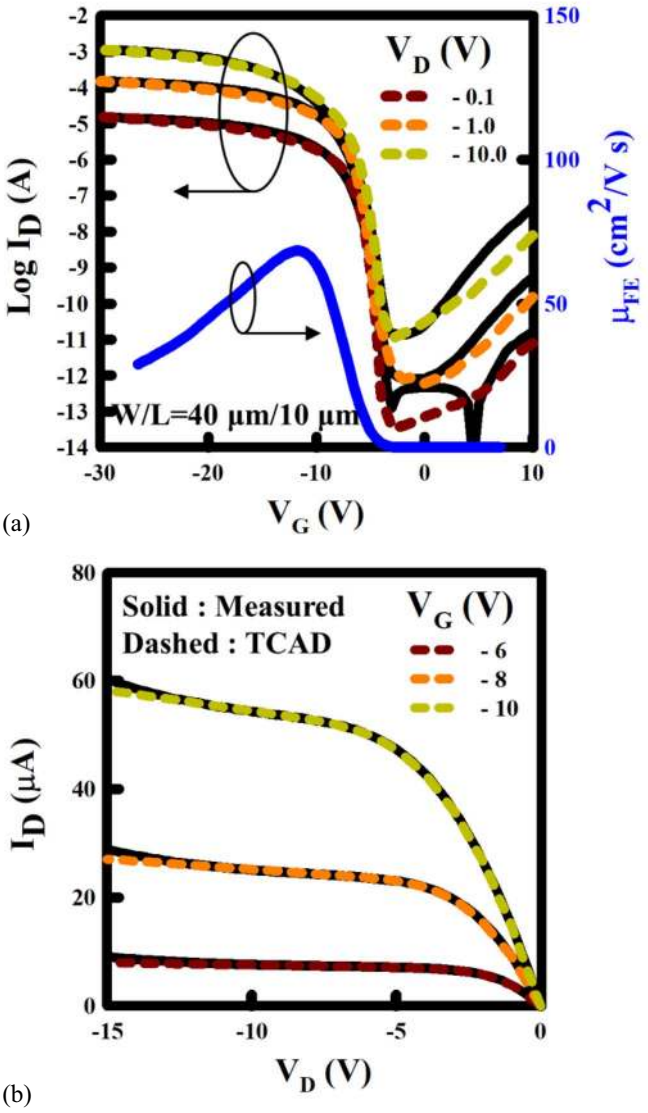


**FIGURE 3.** **(a)-(b) Transfer and output characteristics with TCAD fitting of the measured LTPS TFT having the W/L=40 μm/10 μm. Solid lines represent measurement data and dashed lines are TCAD fitting, respectively, considering 35 nm protrusion effect.**

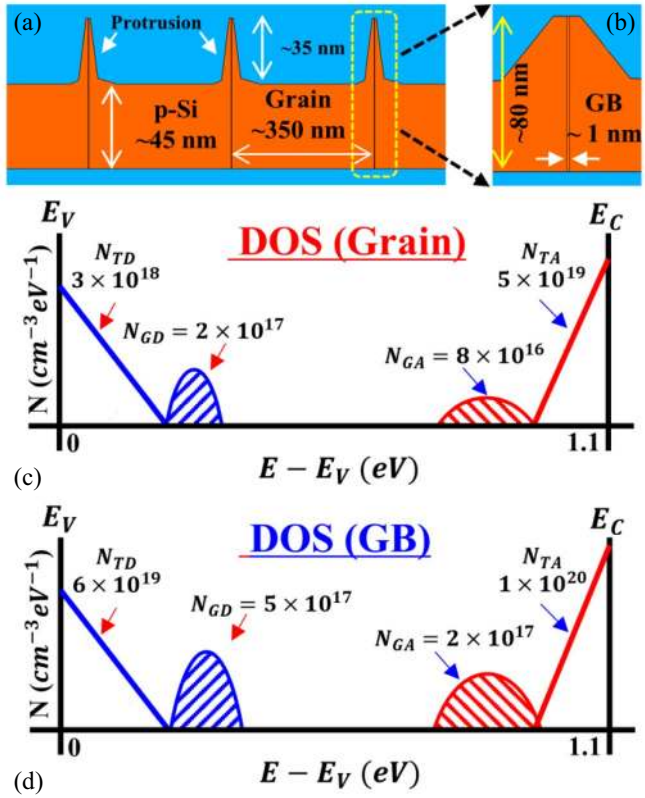


**FIGURE 4.** **(a)-(b) TCAD contour mapping of grain, GB, protrusion height, respectively. (c)-(d) TCAD density of states (DOS, $cm^{-3}eV^{-1}$) model for grain and GB to fit the experimental data.**

TCAD simulation, the simulated output I-V curves exhibited excellent fitting with experimental $I_D$ at saturation (higher $V_D$).

The distribution of potential profiles at the vicinity of GB of LTPS TFTs was demonstrated in an earlier report [25]. The influence of the GB on electrical performance has been investigated by considering the traps either at the GBs or uniformly distributed throughout the poly-Si [26]. Localized traps at the GB are found to be responsible for the kink effect in ELA LTPS TFTs [27]. It is assumed that the GB exists in poly-Si and extends towards the protrusion peak. However, the previous reports did not consider the amount of carrier traps at the GB protrusion which was clearly under-estimated numerical approaches [28]. Dimitriadis and Tassis reported a two-dimensional (2-D) numerical simulation approach where a continuous distribution of carrier traps in the energy gap consisting a broad peak close to midgap and an exponential band tail [29]. Herein, for the first time, we consider two separate DOSs (one for poly-Si grain and the other for GB with protrusion) for the better estimation of GB protrusion effect.

Fig. 4(a) shows the simulated contour mapping of poly-Si grain and GB, and (b) shows a GB having a width of 1 nm. The grain and GB dimensions and protrusion height can be achieved from the experiment, which is used for the simulation of the electrical performance of the ELA LTPS TFTs. DOS parameters such as valance and conduction band tail states at the band edges ($N_{TD}$, $cm^{-3}eV^{-1}$ and $N_{TA}$, $cm^{-3}eV^{-1}$), tail state slopes ($W_{TD}$, $eV^{-1}$ and $W_{TA}$, $eV^{-1}$), and donor-like and acceptor-like states with Gaussian distributions ($N_{GD}$, $cm^{-3}eV^{-1}$ and $N_{GA}$, $cm^{-3}eV^{-1}$) along with their full width at half maximums ($W_{GD}$, $eV^{-1}$ and $W_{GA}$, $eV^{-1}$) were varied in order to fit the TFT measurement data at different $V_D$ and $V_G$, respectively as shown in Fig. 3(a) and (b). Fig. 4(c)-(d) represents the DOS for poly-Si grain and GB and we summarized the DOS parameters in TABLE-1. We also use the same DOS parameters of poly-Si grain and GB (Fig. 8) to estimate protrusion geometry impacts.

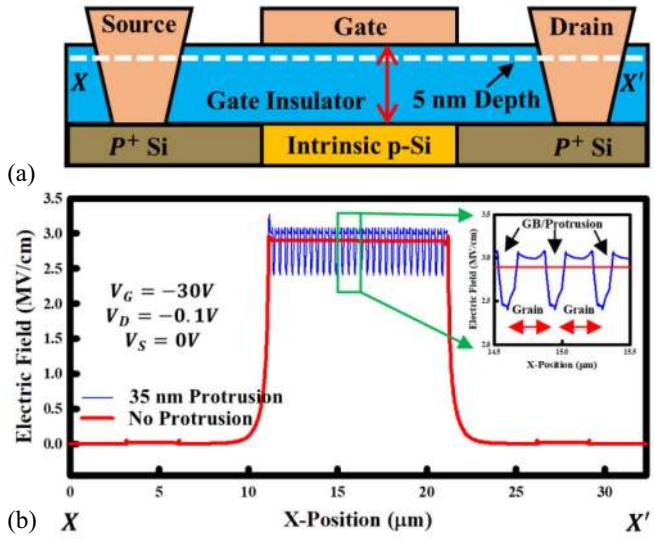


**FIGURE 5.** **(a) Point of intercept, (b) simulated electric field inside TG/GI interface at 5 nm depth inside $SiO_2$ (inset: zoom-in electric field between consecutive poly-Si grains/GBs). An electric field fluctuation has been observed due to 35 nm protrusion at GB.**

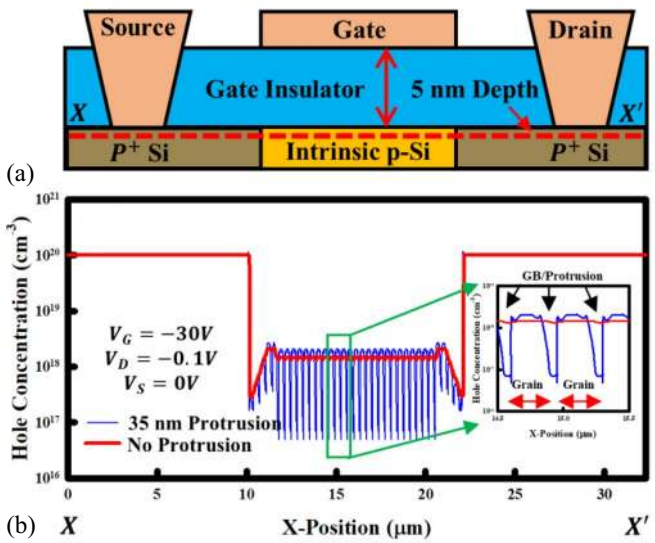


**FIGURE 6.** **(a) Point of intercept, (b) simulated hole concentration of the LTPS TFT at GI/silicon interface at 5 nm depth inside poly-Si. (inset: zoom-in hole concentration between consecutive poly-Si grains/GBs). A hole carrier reduction has been observed due to 35 nm protrusion effect at GB.**

## V. RESULTS AND DISCUSSION

Fig. 5 (a) shows the schematic cross-section of ELA LTPS TFT in order to analyze the LTPS protrusion effect. We consider a 5 nm lateral depth line ($XX'$) inside GI underneith from source electrode until the drain electrode. The electric field distribution inside GI is the measure of reliability and sugessts the quality of GI, gate leakage characteristics, and breakdown characterististics of the fabricated devices [30]. To investigate the electric field (V/cm) effective inside the GI, we applied constant biases; $V_G = -30$ V, $V_D = -0.1$ V and $V_S = 0$ V which analytically provides a constant electrical field $\sim 3 \times 10^6$ V/cm underneith the gate electrode.

Fig. 5 (b) compares the simulated electric field inside GI in LTPS TFTs without and with 35 nm protrusion in the poly-Si layer. A critical fluctuation of the electric field has been evident under constant gate bias for the TFTs with the protruded poly-Si layer. However, the stable electric field inside the gate insulator for TFTs without protrusion inside the poly-Si layer suggests a comparatively less or no trapping of fixed charges inside the GI layer [31]. Interestingly, a negligible impact of GBs on electric field distribution in the GI layer has been found for both devices. The reduction of the electric field by the poly-Si protrusion might result in less charge accumulation under the gate bias inside the poly-Si layer and thus, reduction in drain current is expected.

Fig. 6 (a) shows the schematic point of intercept to distinguish the hole carrier concentration ($cm^{-3}$) inside the poly-Si layer in order to analyze the LTPS protrusion effect. We consider a 5 nm lateral depth line ($XX'$) underneith from source electrode until the drain electrode. The hole carrier concentration inside poly-Si is the measure of electrical conductivity of the TFTs which might affect the carrier transport, $\mu_{FE}$ and $I_D$. To estimate hole concentration inside the poly-Si layer, we applied the same biasing conditions which was applied to check the electric field distribution.

Fig. 6 (b) compares the simulated hole concentration in LTPS TFTs without and with 35 nm protrusion in the poly-Si layer. A drastic reduction of hole concentration has been observed ($\sim 5 \times 10^{16}$ $cm^{-3}$) under constant gate bias for the TFTs with protruded poly-Si layer which might be due to the trapping of holes near GB and/or inside protrusion [10], [12]. However, stable hole concentration inside the poly-Si layer for TFT without protrusion suggests a comparatively less or no trapping of the holes inside the active layer. It should be noted that, a negligible impact of GBs on hole concentration in the poly-Si layer has been observed for both devices. The drastically reduced hole concentration due to poly-Si protrusion might be originated from the carrier trappings and larger amounts of traps around the side wall and two sides of the protrusion [32].

In order to estimate the electrical profiles between consecutive grains/GBs, we demonstrated TCAD contour mapping. Fig. 7(a)-(b) shows the zoom-in cutline at the interface between GI/poly-Si layer (5 nm lateral depth line ($XX'$)) for the TFTs without and with 35 nm protrusion. A simulated electric field at poly-Si grain region is found $\sim 1.5 \times 10^5$ V/cm in Fig. 7(c), whereas, a remarkably less electric field of $\sim 3.4 \times 10^4$ V/cm has been achieved ($\sim$75% reduction) at the position of GB protrusion. Similar to electric field distribution, a simulated hole concentration at protrusion GB site has been extracted as $\sim 5 \times 10^{16}$ $cm^{-3}$ in Fig. 7(d), whereas, poly-Si grains exhibit a simulated hole concentration of $\sim 3 \times 10^{18}$ $cm^{-3}$ and suggesting the strong carrier trapping at protrusion site as the origin of TFT performance degradation than the poly-Si TFTs without protrusion.

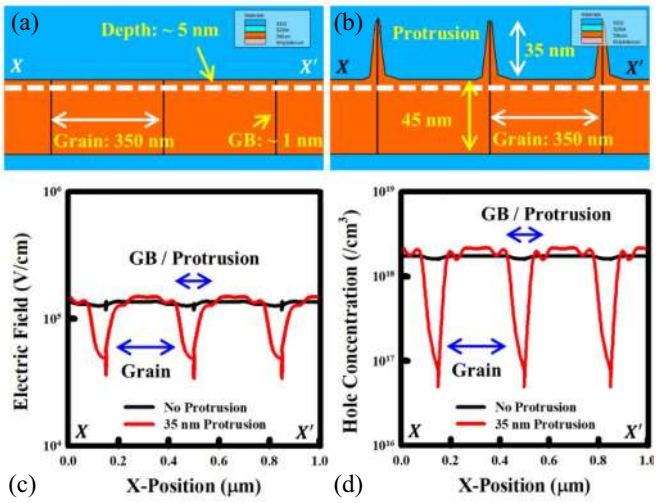


**FIGURE 7.** (a)-(b) Point of intercept, (c) zoom-in simulated electric field, and (d) zoom-in simulated hole concentration of the LTPS TFT at 5 nm depth inside silicon semiconducting layer with and without protrusion using TCAD.

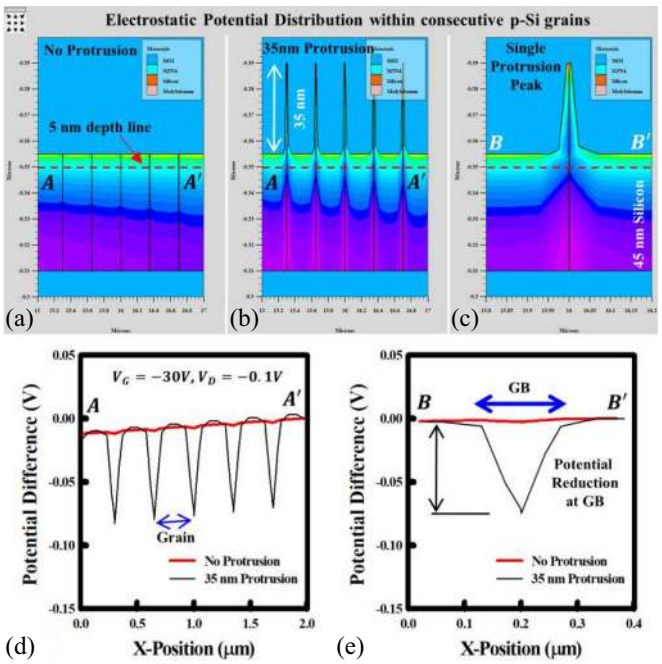


**FIGURE 8.** (a)-(b) Electrostatic potential contour mapping inside the poly-Si layer at 5 nm depth (*AA′*) for no-protrusion, and 35 nm protrusion, respectively, using TCAD simulation. (c) Zoom-in potential contour mapping for a single protrusion peak. (d) Comparison of potential distribution at *AA′* depth line between poly-Si grains without and with protrusion within consecutive grains. (e) Comparison of potential distribution at *BB′* depth line between two poly-Si grains for a single protrusion peak. A drastically reduced electrostatic potential (V) has been observed at protrusion peak as compared to the poly-Si layer without protrusion.

To achieve the dynamics of charge carriers between the poly-Si grains, we need to understand the electrostatic potential distribution. Fig. 8 (a)-(b) show the potential distribution between consecutive grains/GBs using TCAD contour plotting of poly-Si layer without protrusion and with 35 nm

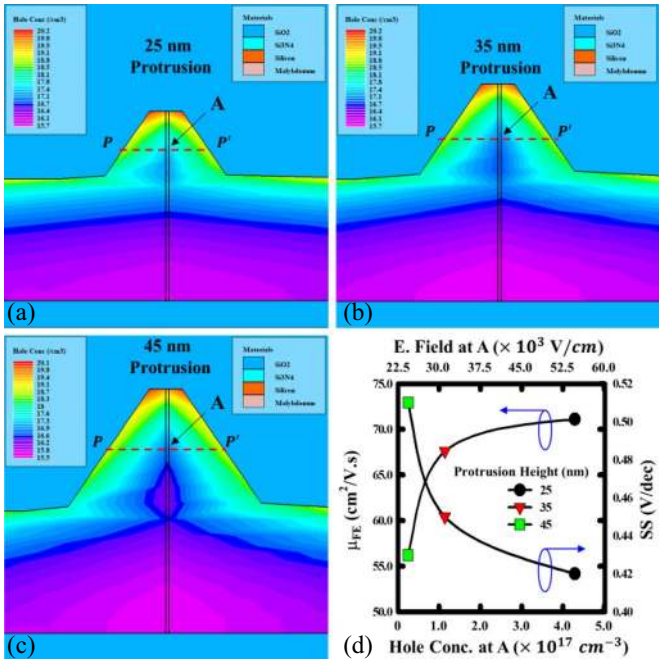


**FIGURE 9.** (a)-(c) Hole concertation contour mapping inside poly-Si protrusion for the heights of 25, 35, 45 nm, respectively, using TCAD simulation. A vertical cutline (*PP′*) at the center of protrusion (*h*(*P*)/2) intersect with GB at "*A*". (d) Comparison of $\mu_{FE}$ and SS for different *h*(*P*) as the function of extracted hole concentration and electric field at "A" on *PP′*. Smaller protrusion height exhibited better electrical performance as compared to the taller protrusion peak at GB.

protrusion at GB, respectively. A 5 nm lateral depth line ($AA'$) at the interface between GI/poly-Si was used to get the potential distribution. Fig. 8 (c) shows zoom-in protrusion peak and we adopted a 5 nm lateral depth line ($BB'$) to evaluate and compare the potential distribution at GB protrusion site. Fig. 8 (d) compares the electrostatic potential distribution between consecutive grains without and with GB protrusion underneath the gate metal. A simulated electrostatic potential at poly-Si grain region is found almost static, however, a drastically reduced potential (Potential difference (V)$\sim -0.07$ eV) at GB protrusion had been obtained. To achieve a more detailed impact of the protrusion on potential distribution at the GB region, we enlarged the contour mapping for a single protrusion peak (Fig. 8(c)) and based on the $BB'$ depth line, we compared the potential distribution. Fig. 8 (e) shows that a severe electrostatic potential degradation at the GB region with the protruded poly-Si layer as compared to poly-Si without protrusion. The above-explained results indicate that there might be severe charge trapping at GB/protrusion site than that of poly-Si without protrusion.

Fig. 9 (a)-(c) show the hole concentration contour mapping to achieve the correlation between protrusion height (h(P)) and hole carrier distribution (also, electric field distribution, not shown here) inside protruded poly-Si region at GB. For a detailed analysis purpose, we drew a lateral cutline ($PP'$) at the center of protrusion (h(P)/2) and we also considered

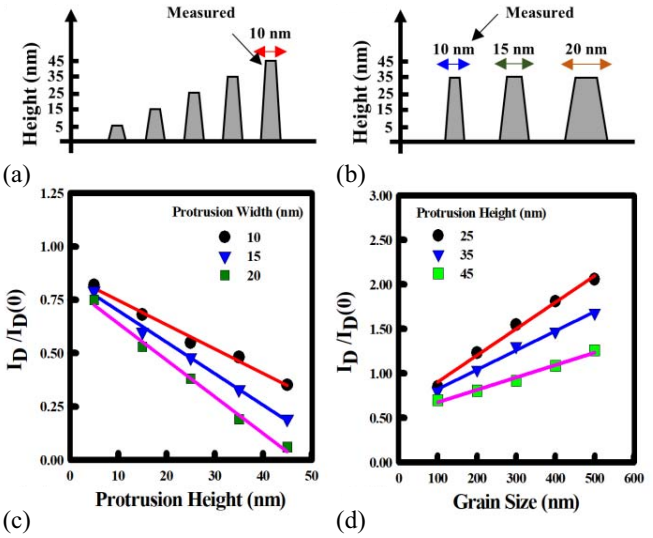


**FIGURE 10.** **(a)-(b) TCAD simulation set-up for $I_D$ analysis under different protrusion heights (nm) and widths (nm). (c) Changes in drain current ($I_D/I_D$ (0)) with respect to protrusion width (nm) and protrusion height (nm). (d) Changes in drain current ($I_D$ /$I_D$ (0)) with respect to grain size (nm) and protrusion height (nm).**

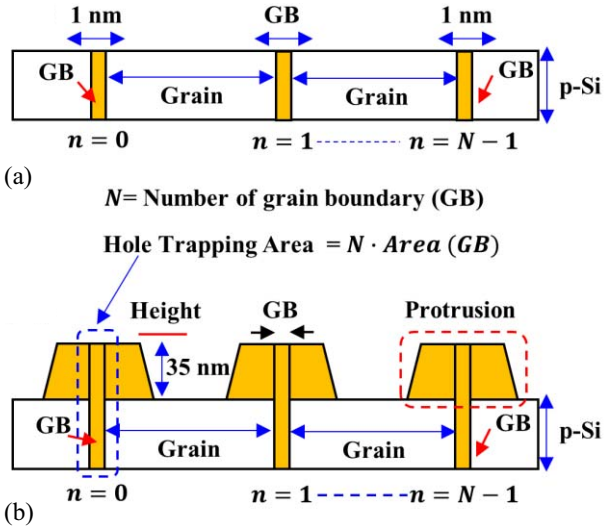


**FIGURE 11.** **Mechanism of protrusion induced $I_D$ variation. (a) Polycrystalline silicon with 350 nm grain and 1 nm grain boundary (GB) without protrusion, and (b) with 35 nm protrusion, respectively. The increased charge trapping area due to protrusion as compared to LTPS without protrusion results in reduction of drain current.**

the point "A" on PP′ (intersect point between GB and PP′) to extract electric field and hole concentration. Using the same DOS listed in TABLE-1 while fitting the experimental data in Fig. 3, we simulated I-V curves for h(P) of 25, 35, and 45 nm, respectively. We plotted the $\mu_{FE}$ and SS as a function of hole concentration ($cm^{-3}$) and also, as a function of electric field (V/cm) at point A. Fig. 9 (d) confirms that a smaller h(P) of 25 nm experience a higher electric field ($\sim 5.62 \times 10^4$ V/cm) at position "A" as compared to a taller h(P) of 45 nm (electric field $2.29 \times 10^4$ V/cm). Therefore, 25 nm protrusion height exhibits higher hole concentration ($4.3 \times 10^{17}$ $cm^{-3}$) as compared to 45 nm height ($2.53 \times 10^{16}$ $cm^{-3}$) which can also verify the better electrical characteristics of LTPS TFTs with a smoother poly-Si surface.

We discussed the simulated protrusion effect on the electrical performance of poly-Si TFTs which was based on experimental GB protrusion geometry with ~35 nm protrusion height, 350 nm lateral grain size and ~ 10 nm protrusion valley width on top of GB regions (Fig. 2). In order to investigate the influence of protrusion geometry on the electrical performance of ELA LTPS TFTs, we varied the protrusion height between 5 nm to 45 nm and also the protrusion valley width of 10 nm, 15 nm, and 20 nm, respectively in Fig. 10(a)-(b). We kept the same DOS (Fig. 4) which was taken while fitting the experimental data in Fig. 3. We plotted the simulated drain current ratio ($I_D/I_D(0)$) as a function of protrusion height in Fig. 10(c) for various protrusion valley widths. We also plotted the simulated drain current ratio ($I_D/I_D(0)$) as a function of poly-Si grain size between 100 nm ~ 500 nm in Fig. 10(d) for various protrusion heights of 25 nm, 35 nm (measured protrusion height) and 45 nm, respectively. $I_D$ is taken at TFT saturation region for $V_G = -30$V, $V_D = -0.1$V, and $V_S = 0$V. $I_D(0)$ is defined as the drain current without protrusion in poly-Si layer. A significant drop of $I_D$ has been observed with increasing protrusion height and widening protrusion valley. Moreover, increasing poly-Si grain size exhibits a linearly increasing dependency with enhanced $I_D$, also, shorter protrusion height exhibits better $I_D$ as compared to taller protrusion peak at GB. These observations are expected using the charge trapping phenomenon which is further verified by the increased DOS at GB plus protruded poly-Si region [10], [12]. It should be noted that we could not find the impact of only GB on electrical profiles. Furthermore, it is difficult to measure the exact GB size, however, the previous reports suggested an approximate GB width between 1 nm ~ 5 nm [5], [10], [25]. It should also be noted that an approximated GB width of 5 nm has very small electrical performance change (by TCAD simulation) as compared to 1 nm (not shown here) and therefore, we considered the minimum GB width of ~1 nm while fitting the experimental data.

Fig. 11 represents a pictorial description of the charge trapping mechanism to explain the impact of GB protrusion on the electrical performance of the fabricated TFT devices using TCAD simulation. Let us assume that the total number of GBs is "N". A device without protrusion has, therefore, an accumulated charge trapping area of ~N·area (GB). In contrast, LTPS TFTs with protrusion height (h(P)) of ~35 nm exhibits a tri-angular areal distribution from TEM images (Fig. 2(b)) on top of GB, and therefore, the accumulated trapped area might not be limited only within GB region, rather it extended a little. Therefore, it is obvious from the above-mentioned illustration that, the protrusion on the GB site drastically captured charged carriers (holes in PMOS LTPS TFTs) and a reduction of $\mu_{FE}$ and $I_D$ is certainly present in the devices.

## VI. CONCLUSION

We studied the effects of GB protrusion on the electrical performance of ELA based PMOS LTPS TFTs. Based on AFM and transmission electron microscopy (TEM) images, we clearly distinguished the GB protrusion geometries (poly-Si grain size, protrusion height, width, etc.). A numerical TFT modeling by Silvaco TCAD software has been performed to fit the experimental results and separate DOSs were assigned for both the grain and GB/protrusion regions. TCAD contour mapping suggests a drastically reduced electric field (∼75% reduction) and hole carriers at the GB protrusion site. From 2-D contour mapping, we observed a significantly reduced hole concentration ($\sim 5 \times 10^{16}\ cm^{-3}$) at GB protrusion site as compared to poly-Si grain ($\sim 3 \times 10^{18}\ cm^{-3}$).

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