PAPER

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Effect of hysteretic and non-hysteretic negative capacitance on tunnel FETs DC performance

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Abstract

This work experimentally demonstrates that the negative capacitance effect can be used to significantly improve the key figures of merit of tunnel field effect transistor (FET) switches. In the proposed approach, a matching condition is fulfilled between a trained-polycrystalline PZT capacitor and the tunnel FET (TFET) gate capacitance fabricated on a strained silicon-nanowire technology. We report a non-hysteretic switch configuration by combining a homojunction TFET and a negative capacitance effect booster, suitable for logic applications, for which the *on*-current is increased by a factor of 100, the transconductance by 2 orders of magnitude, and the low swing region is extended. The operation of a hysteretic negative capacitance TFET, when the matching condition for the negative capacitance is fulfilled only in a limited region of operation, is also reported and discussed. In this late case, a limited improvement in the device performance is observed. Overall, the paper demonstrates the main beneficial effects of negative capacitance on TFETs are the overdrive and transconductance amplification, which exactly address the most limiting performances of current TFETs.

Supplementary material for this article is available online

Keywords: tunnel FET, ferroelectric, negative capacitance, NC-TFET

(Some figures may appear in colour only in the online journal)

1. Introduction

As CMOS technology is continuing its relentless down-scaling, new challenges are encountered to sustain the performance of integrated circuits; among these, the reduction of the threshold voltage and voltage multiply are high priorities of the research community. Among alternative structures, tunnel FETs (TFETs) are the most promising steep-slope switch candidates that are making use of quantum-mechanical band-to-band tunneling (BTBT) [1–3]. The most critical challenge in TFETs is to realize a high *on*-current without compromising the subthreshold swing. The *on*-current of a TFET is the integral of the transmission probability, T_{WKB}, of the interband tunneling barrier over the source-channel junction [4, 5]. This barrier can be approximated by a triangular potential [2], so T_{WKB} can be calculated using the Wentzel–Kramer–Brillouin (WKB) approximation [6]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^{\star}}\sqrt{E_g^3}}{3q\hbar\,(E_g + \Delta\Phi)}\right), \quad (1)$$

where $m^{\star}$ is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length that describes the spatial extent of the transition region at the source-channel interface [4]. In a TFET, at a constant drain voltage (V_d), the increase of the gate voltage (V_g) modulates the device surface potential, which reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$). This means that in the first

approximation, the drain current is a super-exponential function of V_g and a high *on*-current requires a high transparency of the tunneling barrier, thus maximizing T_{WKB} [7].

Recently, it has been suggested that the integration of a ferroelectric material to the gate stack of conventional field effect transistors (FETs) can provide a feasible solution to step up the gate voltage. The underlying idea consists of exploiting the negative capacitance (NC) region of ferroelectric materials, which is defined as $C_{FE} = dQ/dV_{FE}$, where Q and V_{FE} refer to the charge density per unit area and the voltage drop over the ferroelectric, respectively [8–10]. It is well established that the use of a ferroelectric negative capacitor in-series with the gate of a field effect transistor could offer an internal voltage amplification [11–13], which is expected to increase the tunneling probability in TFETs [14, 15].

Previous works on NC tunnel FETs have mainly theoretically investigated the performance of these type of devices [14, 16] and there are a few experimental demonstrations [17], major focus being on the achieved low swing value. Here, we explore and demonstrate the double beneficial effect of negative capacitance on both decreasing the subthreshold swing and improving the overdrive. Despite the fact that the used experimental devices are homojunction silicon TFETs with relatively modest performance, the overdrive improvements obtained by connections with ferroelectric capacitors fulfilling the negative capacitance matching are the best reported to date. In addition, we experimentally show that a hysteresis-free behavior of NC-TFETs can be achieved only under a matching condition between the ferroelectric NC and the gate capacitance of the baseline TFET. A non-hysteretic switch configuration using a homojunction silicon-based TFET and an NC booster is also investigated. The improvement of the performance of the non-hysteretic NC-TFET is compared with a hysteretic one, showing a limited gain when the matching condition is not fully satisfied. Overall, the paper demonstrates that the negative capacitance can be indeed employed as an efficient booster of tunneling field effect transistors to simultaneously enhance the overdrive current (which is the main disadvantage of TFETs compared to MOSFETs) and extend the low slope region.

2. Theory

The NC-TFET structure and its operation principle are schematically depicted in figure 1. The gate stack of a conventional TFET is replaced by a series combination of a ferroelectric and a linear dielectric [18]. The use of an intermediate metallic film has the advantage to avoid any non-uniform potential profile along the source-drain direction [10]. The NC region of ferroelectric materials is unstable and exhibits hysteretic jumps in the polarization. However, it can be stabilized if a series capacitance, such the one formed by a conventional oxide and a semiconductor in an MOS structure, is placed in-series with a ferroelectric negative capacitor (figure 1(b)). The challenges of using BTBT together with the NC in a single device are related to the matched design of capacitances (ferroelectric and in-series stabilizing MOS capacitance) in a regime of operation where a significant boosting of TFET electrical performance can be achieved [12, 19]. In order to have a non-hysteretic NC switch, the total capacitance of the structure looking into the gate needs to be positive in the whole range of operation [18, 20]. Accordingly, the matching condition of the NC-TFET to have a sufficient amplification in the non-hysteretic operation of the device can express as it follows [21, 22]:

$$C_{total} = (C_{FE}^{-1} + C_{int}^{-1})^{-1} > 0, \tag{2}$$

$$\beta = \frac{\partial V_{int}}{\partial V_g} = \frac{C_{FE}}{C_{FE} + C_{int}} \gg 1, \tag{3}$$

where β is the amplification factor due to the differential amplification of NC, C_{int} and C_{total} represent the equivalent capacitance of the baseline TFET and NC-TFET, respectively (figure 1(d)). The amplification factor, β, is introduced as the derivative of the internal voltage with respect to the gate voltage and its rather a differential voltage gain [12, 22]. The absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and C_{int} need to be relatively close, while the total capacitance of the structure should remain positive in the whole gate voltage range [12]. Using the amplification factor, β, the subthreshold swing (SS) and transconductance (g_m) of an NC switch can be indicated as

$$SS_{NC} = \left(\frac{\partial \log I_d}{\partial V_g}\right)^{-1} = \frac{\partial V_{int}}{\partial \log I_d} \times \frac{\partial V_g}{\partial V_{int}} = \frac{SS_{ref}}{\beta}, \tag{4}$$

$$g_{m-NC} = \frac{\partial I_d}{\partial V_g} = \frac{\partial I_d}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial V_g} = g_{m-ref} \times \beta. \tag{5}$$

In the region where the ferroelectric provides an effective negative capacitance, $\beta > 1$ and the *on*-current will be boosted. Nevertheless, a direct analytical expression that quantitatively links β to the total drain current of the NC-TFET cannot be provided as the tunneling current depends on the surface potential near the tunneling junction in a complex way.

3. Experiments

The employed experimental configuration of the NC-TFET in this work is depicted in figure 2(a) where a PZT capacitor is externally connected to the gate of a strained silicon-nanowire (Si-NW) array TFET. Such external electrical connection offers the flexibility of testing tens to hundreds of PZT capacitor values until the best matching, according to equations (2) and (3) is obtained. The employed configuration corresponds to a metal–ferroelectric–metal–insulator–semiconductor structure that is commonly used for the experimental configuration of

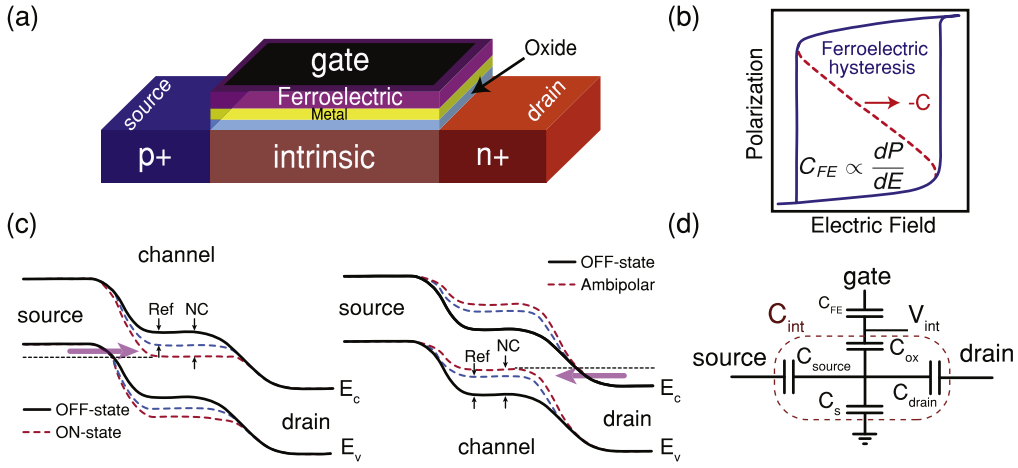

Figure 1. NC-TFET structure and operation principle. (a) Cross-section schematic of an *n*-type NC-TFET. (b) *P*–*E* characteristic of ferroelectric materials that can be stabilized and provide an effective NC if it placed in-series with a positive capacitor. (c) Band diagram of the NC-TFET which is presented for $V_g > 0$ (left) and $V_g < 0$ (right) corresponding to the normal operation and ambipolar behavior of the *n*-type NC-TFET. The amplified gate voltage reduces the energetic difference between the conduction band in the source and valence band of the channel that results in an enhanced tunneling current. (d) Simplified capacitance model of the NC-TFET where C_{source} and C_{drain} represent the gate overlapping capacitance with source and drain, respectively. The ferroelectric, oxide, and semiconductor capacitances are expressed as C_{FE}, C_{ox}, and C_s.

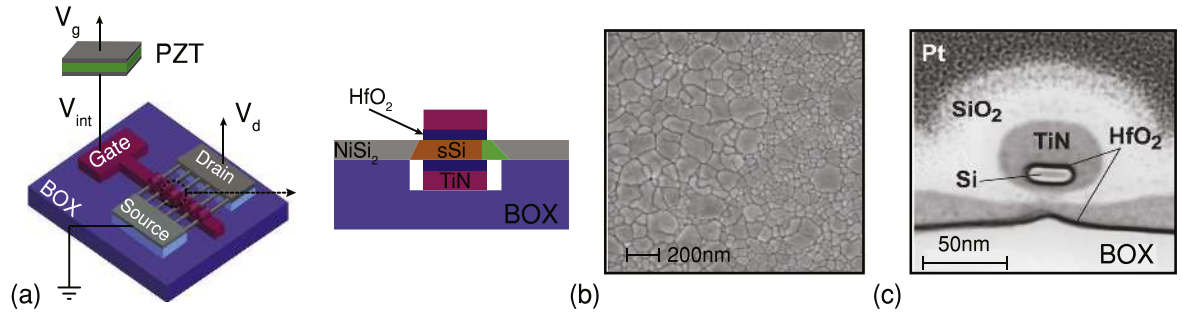

Figure 2. (a) Experimental configuration of investigated NC-TFETs, where the gate of a Si-NW array TFET is loaded by a PZT capacitor. (b) SEM analysis of the PZT indicating the polycrystalline nature of the film. (c) TEM image of the silicon-nanowire TFET. The nanowire array TFETs have a cross-section of $6 \times 30\,nm^2$ and a gate length of 350 nm.

negative capacitance field effect transistors [10]. For this study, 46 ± 3 nm of $Pb(Zr_{43},Ti_{57})O_3$ (PZT) ferroelectric film has been grown via the chemical solution deposition root on a Pt-coated silicon wafer. The polycrystalline PZT film has a dense columnar grain structure with a grain size of 200 ± 100 nm (figure 2(b)). The fabrication process and the electrical characterization of the PZT thin film are extensively discussed in the supplementary materials, which are available online at stacks.iop.org/NANO/29/095202/mmedia. The nanowire array TFETs have a cross-section of $6 \times 30\,nm^2$ with a gate length of 350 nm (figure 2(c)). The structural data and the fabrication procedure of reference TFETs are also explained in detail in supplementary materials.

Generally, high-quality epitaxial ferroelectric layers are considered suitable for NC devices as they are more likely to form a mono-domain state characterized by a simple coercive field [23]. This is in contrast with the typical behavior of polycrystalline films, which tend to form complicated poly-domain patterns with a broad distribution of nucleation energies and coercive fields [24–26]. Here, we show that this behavior can be changed dramatically by a repetitive bipolar voltage stress, known as the training procedure of ferroelectric. It should be noted that the training procedure of ferroelectric is different from the well-known wake-up phenomena. The wake-up effect corresponds to the increase of existing remanent polarization after a large number of switching cycles ($>10^3$) [27, 28]. Here, we are raising the point that by applying a limited number of bipolar voltage stress, dipoles can be aligned in the same direction which leads to a mono-domain-like behavior of the polycrystalline ferroelectric. Figure 3 depicts the piezoelectric response measured on a PZT capacitor before (figure 3(a)) and after (figure 3(b)) the training. Piezoelectric loops measured through the top electrode of the PZT capacitor after 20 cycles at ± 7 V, represent a sharp switching and nearly constant piezoelectric response within the voltage range from -2 to 1 V (or from 2 to -1 V). This behavior suggests that the poled polycrystalline ferroelectric layer approaches the

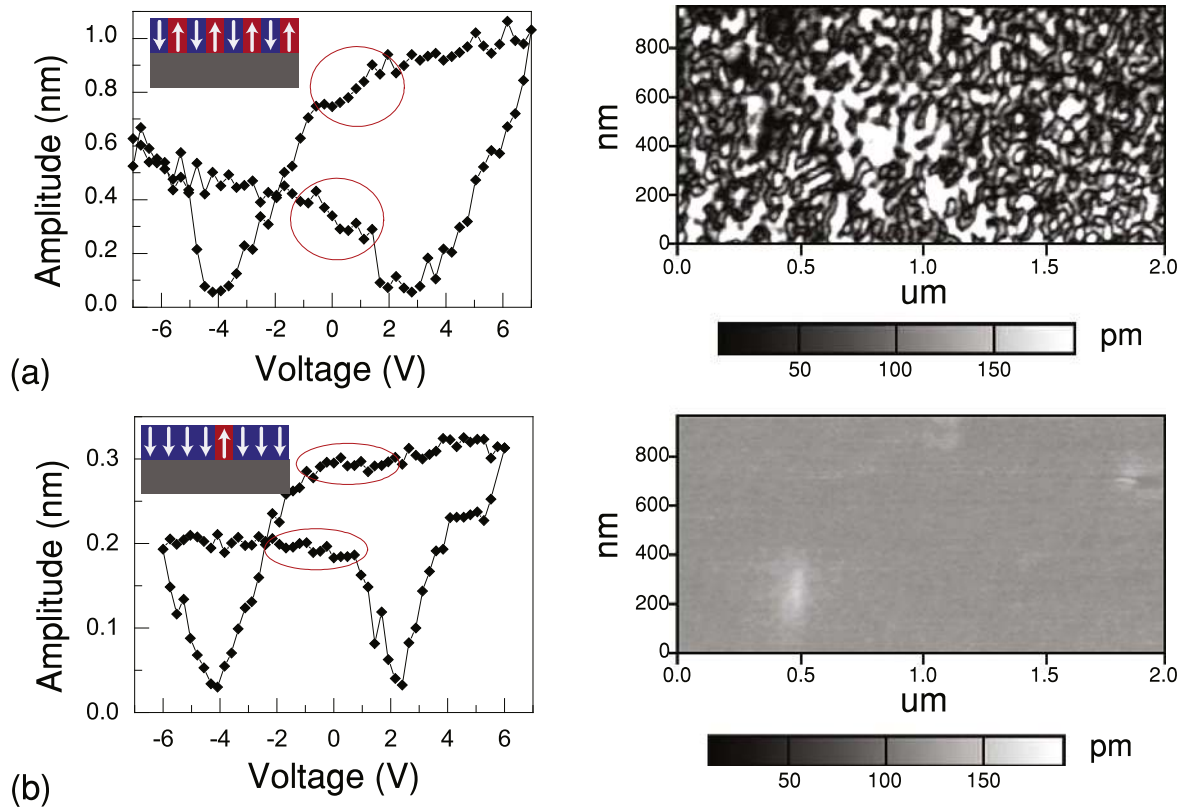

Figure 3. Piezoelectric response of the employed PZT thin film. Results are measured before (a) and after (b) the training procedure of ferroelectric. (a) Illustrates the broad distribution of nucleation energies and coercive fields while (b) represents the mono-domain like behavior of the poled PZT after 20 cycles at ±7 V.

mono-domain behavior and does not switch at least at low DC voltages [23]. Note that the piezoelectric loops collected on the as-fabricated capacitors without any training reveal different behavior typical for region-by-region poly-domain switching expected from a polycrystalline film. Consequently, the demonstration of the NC effect using a polycrystalline ferroelectric layer constitutes a significant step towards the integration of NC gates in CMOS technology [23]. In fact, fabrication of epitaxial perovskite layers on silicon is an extremely challenging task, whereas polycrystalline ferroelectrics such as PZT can be integrated, as shown in previous reports [29, 30].

4. Results and discussions

Figure 4 reports experimental transfer characteristics data measured on *n*-type Si-NW array TFETs with and without connecting a PZT capacitor. The reference homojunction TFETs have $I_{on} \sim 0.1\ \mu$A at $V_{gs\_eff} = 0.9$ V and $V_{ds} = 0.5$ V (where $V_{gs\_eff} = V_{gs} - V_{th}$ and the constant current method at $I_d = 10^{-7}$ A is employed for threshold voltage extraction) with a swing in the order of 100–150 mV dec^{-1} and show ambipolar behavior. The performance of baseline TFETs corresponds to moderate silicon-based tunnel FETs [2, 31, 32]. It should be noted that although TFETs have been proposed to realize sub-60 mV dec^{-1} swing, however, the experimental demonstration of a sub-thermal swing in silicon TFETs is extremely challenging. Besides that, high current values compromise the subthreshold swing [2]. The presented characteristics in figure 4 belong to structures with different reference TFETs which are not totally identical due to the process variation. The gate current of TFETs is very low and negligible compared to the drain current over the whole operation range. A significant double improvement in subthreshold slope and overdrive of the TFET is shown in figure 4(a) when the ferroelectric and the gate capacitances are matched so that a non-hysteretic NC operation is achieved. The I_{on} is boosted over the whole range of operation, enhanced up to 100 times of its original value at the maximum gate voltage. This is explained by the fact that the NC effect behaves as an efficient electrical booster of the surface potential (ψ_s) and the body factor (m) of the TFET in the region following the barrier narrowing. This is fundamentally reflected into a body factor reduction less than 1, acting as a performance booster where the *on*-current of TFETs would otherwise start to have a sloppy dependence on the gate voltage [2, 4]. It should be remarked that the surface potential boosting of NC effect not only increases the tunneling probability but also improves the region over which the tunneling current is integrated. In addition to, considering Landau–Khalatnikov equation, high order terms of the

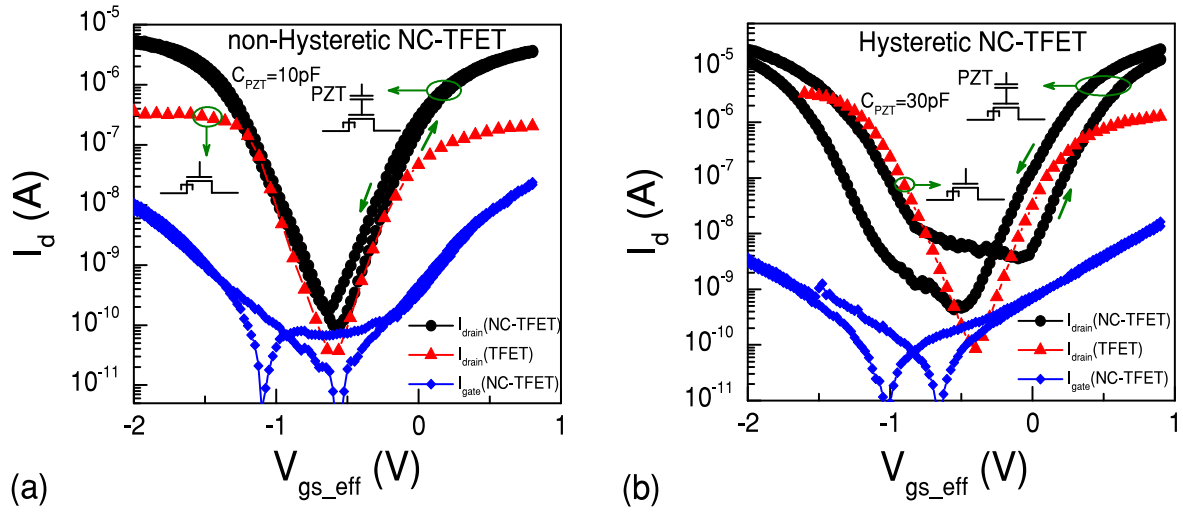

Figure 4. Transfer characteristics of a non-hysteretic and a hysteretic NC-TFET where the negative capacitance matching condition is fulfilled in the entire range of the operation (a) and in a limited range of the gate voltage (b). The reference devices correspond to Si-NW array *n*-type TFETs with a drain voltage of 0.5 V.

ferroelectric charge cannot be neglected at high gate voltages that result in an enhanced negative capacitance effect [33]. The NC effect acts as the TFET performance booster near subthreshold and for the overdrive region. Therefore, the gate voltage can be reduced by 65% maintaining the same level of the output current. Although the reported NC-TFET here do not exhibit a sub-thermal swing like other state of the art heterojunction tunnel FETs [34, 35], the reported experimental characteristics show two remarkable facts: (i) the highest overdrive and transconductance improvements reported today with NC as technology booster, (ii) the extension of the minimum subthreshold region for higher current values [36, 37]. Additionally, our results fully demonstrate that negative capacitance can be used based on an additive strategy with other TFET performance boosters so that improvements are cumulative.

Another device architecture with a different PZT capacitor and TFET, matching the condition of NC only in a limited region (at high gate voltages) is reported in figure 4(b). In this late case, the NC-TFET operation is fully hysteretic and the performance boosting is narrowed down to a reduced region. All measurements have been carried out at the low drain voltage of 0.5 V due to the fact that high values of the drain voltage provide a non-uniform potential profile that will change the negative capacitance condition [22]. Both figures 4(a) and (b) report the recorded gate leakage current in all range of experiments, proving that its level is systematically lower than the I_{on} and, then, that leakage and charge trapping mechanisms can be neglected in the reported effects. Moreover, this hysteretic leakage presents the typical signature of the ferroelectricity of PZT capacitors. The obtained enhancement in the TFET performance should not be mistaken with the effect of the ferroelectric polarization switching that always occurs with a huge hysteresis. The reported non-hysteretic improvement in the current and conductance can be only achieved in a well-designed negative capacitance transistor.

In figure 5, we report the improvement induced by the use of the negative capacitance on TFET transconductance and subthreshold slope, in non-hysteretic and hysteretic modes of operation. Double sweep measurements with a negligible hysteresis for a device that fulfills the analytical condition of the non-hysteretic negative capacitance (corresponds to the presented device in figure 4(a)) are reported in figures 5(a) and (b). In this case, the ferroelectric is stabilized and provides an effective NC in the whole range of the gate voltage which results in an amplification factor above unity ($\beta > 1$) in both subthreshold and overdrive regions. Figure 5(a) represents the transconductance boosting by a factor of 10–100 compared to the reference TFET. The largest improvement (higher β value) occurs in the overdrive region due to the surface potential amplification, caused by the NC effect where g_m is increased up to two orders of magnitude. This evidences that the negative capacitance provides a very strong performance boosting effect in TFETs. Figure 5(b) illustrates a smaller, yet clear improvement of the subthreshold swing by the NC effect, in agreement with the recently reported theoretical results [38, 39]. As a consequence of the subthreshold slope and overdrive enhancement, the *on*-current is boosted over the whole operation range.

Figures 5(c) and (d) summarize the effect of the PZT negative capacitance booster on DC electrical performance of the hysteretic NC-TFET (figure 4(b)) fulfilling the NC matching condition in a limited region. The transconductance is boosted for high gate voltages, reaching a factor of 10 at the maximum gate voltage (figure 5(c)). The subthreshold slope shows no considerable enhancement (figure 5(d)) as the NC matching condition is not fulfilled for low gate voltages. It is remarkable that from variously tested devices, only for the ones that closely verifying the NC stability condition,

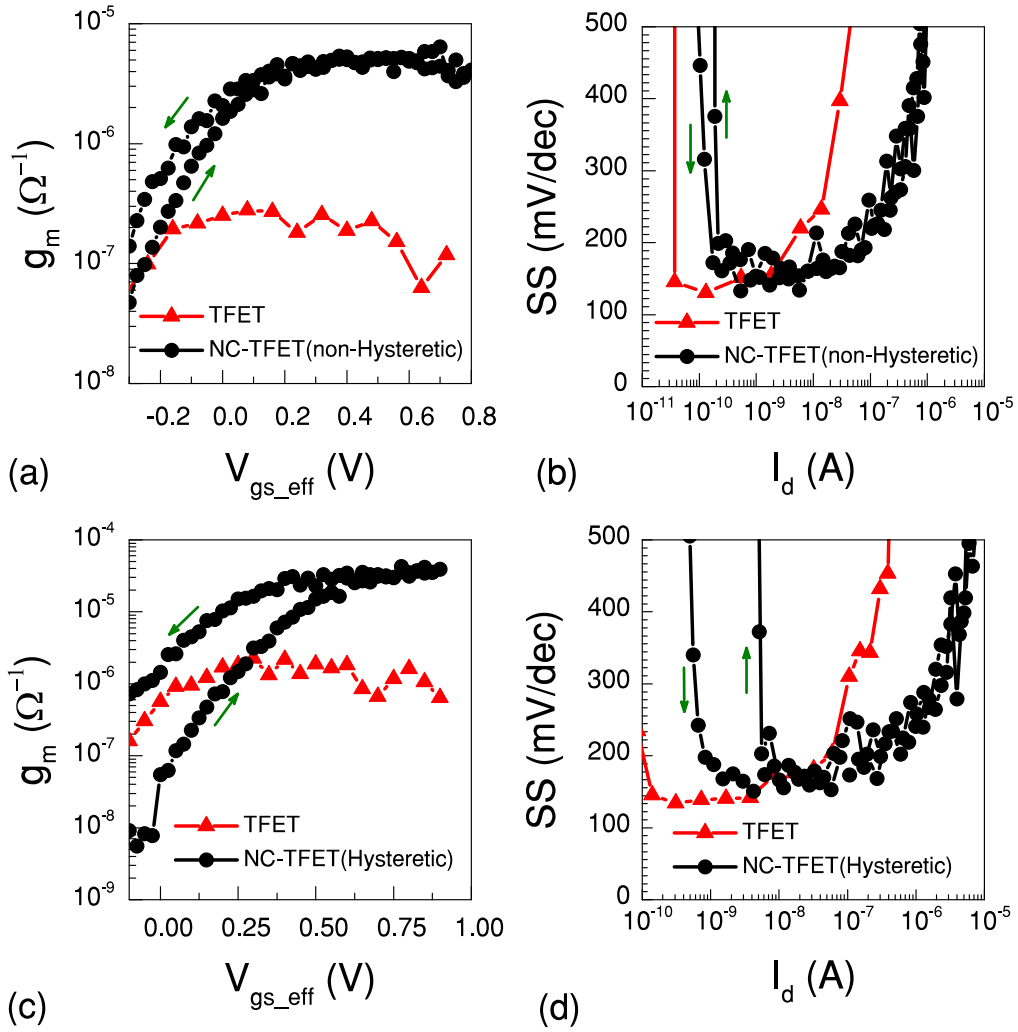

Figure 5. Experimental performance improvement of non-hysteretic and hysteretic NC-TFETs corresponding to the presented devices in figures 4(a) and (b). The transconductance is boosted up to 100 times of its original value (a) and the low slope region is extended over 2 decades of current (b) in the case of the non-hysteretic NC-TFET. A more limited enhancement is obtained in the transconductance of the hysteretic NC-TFET (c) without any boosting in the subthreshold slope (d).

such a performance boosting is observed. Otherwise, a ferroelectric capacitor out of the range of the stability condition in-series with the gate of a TFET would provide a hysteresis without performance boosting. This type of device could be a proper candidate for hysteretic low power logic or for one transistor (1T) Fe-TFET memory applications [39].

Conclusion

In short, it has been reported that the negative capacitance effect can be efficiently utilized to significantly improve the most limiting performances of tunnel FETs: *on*-current, transconductance, and overdrive. It was demonstrated that by properly designing the ferroelectric gate stack, fulfilling the condition for the non-hysteretic NC-TFET, the conduction performance can be improved by many orders of magnitude and a significant overdrive current can be obtained. This strong effect is explained by the voltage amplification caused due to the negative capacitance effect. By its insights and reported experiments, this study proposes a new path to the adoption of both homojunction and heterojunction TFETs with an improved performance, while a negative capacitance booster is properly designed and additively integrated into their gate stack.

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