Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide

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Results of capacitance–voltage measurements are reported for metal–oxide–semiconductor capacitors fabricated using the 4H polytype of silicon carbide doped with either nitrogen (n) or aluminum (p). Annealing in nitric oxide after a standard oxidation/reoxidation process results in a slight increase in the defect state density in the lower portion of the band gap for p-SiC and a significant decrease in the density of states in the upper half of the gap for n-SiC. Theoretical calculations provide an explanation for these results in terms of N passivating C and C clusters at the oxide–semiconductor interface. © *2000 American Institute of Physics.*
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Silicon carbide is a promising material for power electronics because of its wide band gap and high thermal conductivity. Additionally, the material is attractive because, like Si, its native oxide is SiO_2. However, the development of SiC metal–oxide–semiconductor field effect transistors (MOSFETs) has been impeded by the low effective carrier mobility in the FET channel. The low mobilities are directly linked to interface defects that either trap or scatter carriers. For SiO_2/SiC, such defects are present in much higher concentrations compared to the corresponding SiO_2/Si interface. N-channel inversion mode MOSFETs have been demonstrated for both the 4H and 6H polytypes of SiC; however, channel mobility is noticeably lower for 4H–SiC compared to 6H. This is an unexpected result, since 4H–SiC has a higher bulk carrier mobility. Schorner *et al.*[1] attributed the lower 4H inversion channel mobility to the presence of a large and broad interface state density fixed in both polytypes at approximately 2.9 eV above the valence band edge. The majority of these states lie in the conduction band for 6H–SiC($E_g \sim 3$ eV) and hence do not affect carrier mobility in the inversion layer. However, a substantial fraction of these states may lie within the band gap for 4H–SiC($E_g \sim 3.3$ eV), so that in inversion, channel mobility is substantially reduced by field termination, carrier (electron) trapping, and Coulomb scattering.

Afanasev *et al.*[2] attributed the presence of interface states in SiO_2/SiC structures to carbon clusters and near-interfacial defects in the oxide layer. Such defects are likely present following the oxidation of both p- and n-epitaxial layers. Therefore following Schorner, we study the interface state density near the conduction band using standard high frequency (1 MHz) and quasistatic capacitance–voltage

($C–V$) techniques applied to oxidized n-4H–SiC epilayers. Herein, we report results that demonstrate that nitric oxide (NO) annealing has a net positive effect on interface traps. Near the valence band in p-SiC, N incorporation causes a small *increase* in the density of interface defects. In contrast, for n-SiC, N incorporation causes a significant *decrease* in the large density of interface states with energy levels in the upper half of the band gap. The total density of interface defects is significantly reduced with the NO treatment, implying that the interface states that degrade mobility are amenable to passivation.

Lightly doped 4H–SiC epitaxial layers [9×10^{16} cm^{-3}(n) and 3×10^{16} cm^{-3}(p)] were cleaned and oxidized using procedures described elsewhere.[3] The oxidation process is a standard procedure that is terminated with a wet reoxidation anneal at 950 °C following oxide layer growth at 1100–1200 °C. The reoxidation process has been shown to reduce the interface state density near midgap for p-SiC,[4–6] but as shown in Fig. 1, the reoxidation process does not reduce D_{it} near the band edges for either p- or n-SiC.

Wet oxidation generally produces higher quality oxide layers for SiC compared to dry oxidation.[7] However, Li *et al.*[8] report that the electrical quality of oxide layers grown on SiC using dry techniques can be improved by postgrowth annealing in NO. We have added NO annealing to our standard oxidation/reoxidation process in an effort to determine the effect of this additional annealing step on the interface state densities near the band edges. Both n- and p-MOS capacitors were characterized with and without an anneal in flowing NO (0.5 l/min/1 atm/1150 °C/1 h). Recent physical analyses from our group[9] and others[10] show that NO annealing results in the accumulation of nitrogen at or near the interface. The results of electrical measurements are shown in Figs. 2 and 3. The interface state density near the valance
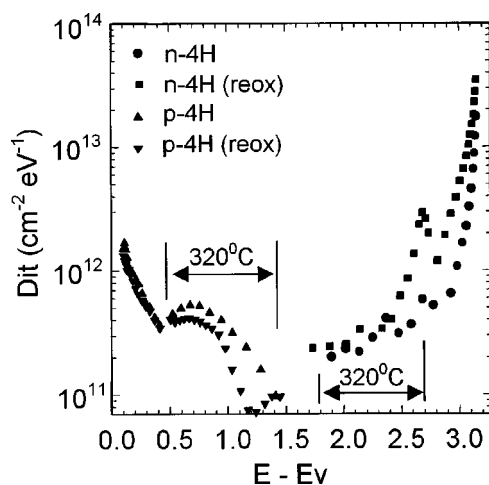
FIG. 1. Interface state densities for *p*- and *n*-4H–SiC oxidized with and without the reoxidation anneal process described in Ref. 3.

band edge [Fig. 2(b)] increases by about a factor of two following the NO anneal; however, near the conduction band edge [Fig. 3(b)], D_{it} is reduced from approximately 1.5×10^{13} to $3.5 \times 10^{12} \, cm^{-2} \, eV^{-1}$.

Attempts to account for the role of N at the SiO_2/SiC interface are hampered by the lack of detailed knowledge of the interface structure. Recent theoretical investigations[11] suggest that a nonstoichiometric interlayer is required to bridge SiC bonding to SiO_2 bonding. This conclusion is supported by spatially resolved electron energy loss spectroscopy.[12] As a result, in addition to dangling bonds, other possible defects at the interface are Si–Si bonds and residual C atoms that may be isolated or in clusters. We have
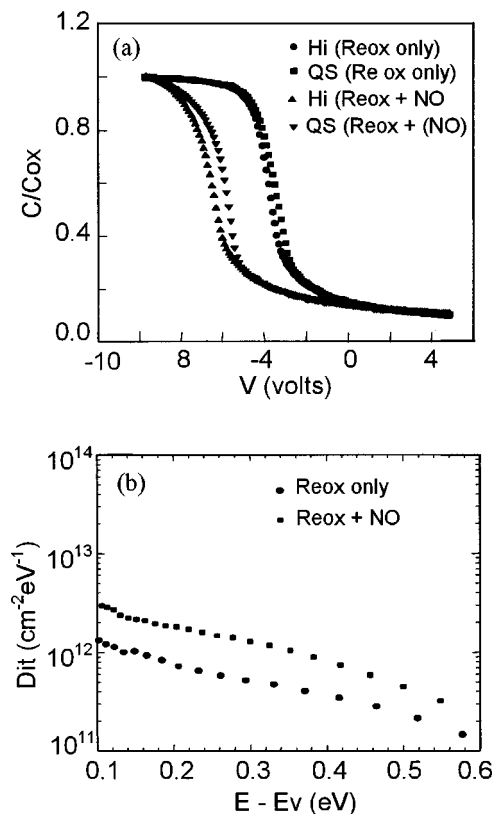

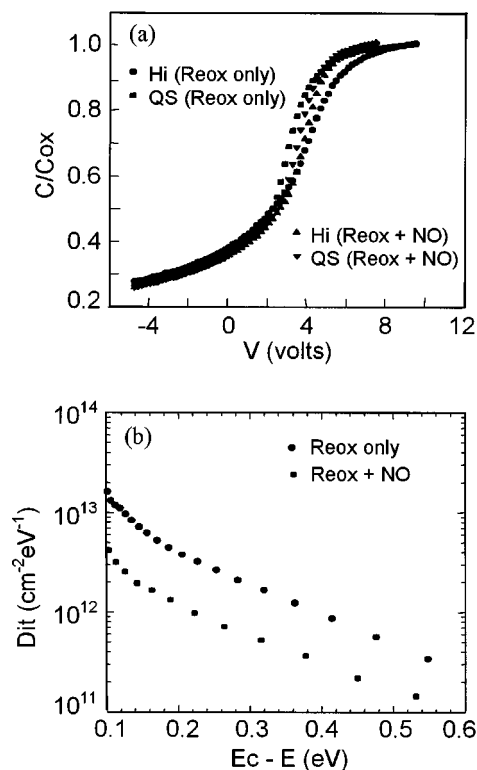FIG. 2. (a) $C-V$ curves and (b) interface state densities near the valence band for *p*-4H–SiC.

FIG. 3. (a) $C-V$ curves and (b) interface state densities near the conduction band for *n*-H–SiC.

performed density-functional calculations[13] to investigate the role of N atoms in passivating C atoms and C clusters. Calculations at the interface are currently not practical; however, using the methodology of Ref. 13, useful information may be derived from model calculations of clustering within SiC. Carbon interstitials rebond within the SiC lattice and cluster with a binding energy of approximately 1 eV per atom. The isolated C interstitial has an energy level in the upper part of the gap, and the level goes slightly higher in energy with each additional C atom added to a cluster [Fig. 4(a)]. Nitrogen atoms passivate the isolated C interstitials entirely; that is, the gap level drops into the valence band [Fig. 4(b)]. For a cluster of two C interstitials, the gap level drops to about the valence band edge, and for larger clusters, the gap levels drop below midgap. We suggest that this effect persists when C atoms cluster as interstitials at the interface. Such a phenomenon accounts for observations that N eliminates states in the upper part of the gap for *n*-SiC and increases the density of defect states in the lower portion of the gap for
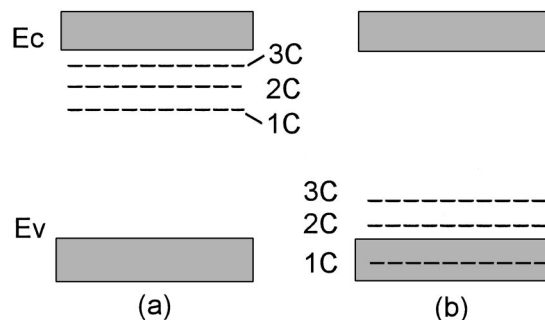

FIG. 4. (a) Energy levels for interstitial C and C clusters in SiC. (b) C and C cluster states in SiC following N passivation.

p-SiC. Gap states with energies that remain unchanged may be due to other defects such as Si–Si bonds. Simple considerations of bonding/antibonding splitting of Si–Si and Si–C bonds suggest that Si–Si bonds at the interface induce symmetric defect states at the two band edges.

In conclusion, we have shown that a standard oxidation/reoxidation process, followed by NO annealing, results in a significant reduction in the interface state density near E_c for SiO_2/n-4H–SiC MOS capacitors. A possible explanation of the passivation effect in terms of N atoms bonding with C atoms and C clusters has been proposed. Nevertheless, it is still important to establish that results near the conduction band edge for *n*-SiC are applicable near the conduction band in *p*-SiC. Channel mobility for *n*-channel inversion mode 4H–SiC MOSFETs depends critically on the interface density near the conduction band edge in *p*-SiC. Mobility measurements currently underway will determine whether NO annealing is a valuable processing step for actual device fabrication. This report provides direct evidence of $D_{it}(E_c)$ reduction and indicates that innovative interface processing does indeed reduce the interface state density that limits channel mobility, and may eventually lead to significant improvements in 4H–SiC MOSFET processing technology.

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