## Effect of surface free energy in gate dielectric in pentacene thin-film transistors

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The surface free energy of a dielectric has a strong influence on the performance of pentacene thin-film transistors. Research shows that by matching surface free energy in the interface of the dielectric and the orthorhombic thin-film phase of pentacene film, the field-effect mobility of transistors is enhanced reaching above 2.0 cm<sup>2</sup>/V s. The authors suggested that a more complete first monolayer of pentacene was formed upon the gate dielectric surface with almost identical surface free energy, *benefiting* carrier transportation. The research also discusses the mechanism of surface free energy effects on the crystalline size and structural disorder in pentacene film. © 2006 American Institute of Physics. [DOI: 10.1063/1.2354426]

Recent research trends draw much attention to organic semiconductor-based thin-film transistors (TFTs) due to dramatic performance improvements observed in this technological domain. Pentacene-based TFTs represent particular interest as one of the most promising technologies.<sup>1,2</sup> The performance of organic TFTs (OTFTs) depends on the use of semiconductors and dielectrics. Surface properties, i.e., surface energy and surface roughness, of a dielectric layer represent distinctive factors which determine potential improvements in electric characteristics of OTFTs.<sup>3–5</sup> In cases where pentacene is grown upon dielectrics with surface-induced morphology, the structure of the first few monolayers is expected to have a strong impact on mobility.<sup>4,6</sup> At the same time, it is possible to improve performance by manipulating charge transport qualities in aforementioned devices. It is therefore important to establish precise interfacial control between organic semiconductors/dielectrics in order to achieve higher performance in OTFTs.

Most studies on OTFTs utilize inorganic silicon dioxide  $(SiO_2)$  as the gate dielectric layer. Typically, the mobility of pentacene-based TFTs featuring  $SiO_2$  dielectric is around  $0.01 \sim 0.5 \text{ cm}^2/\text{V s.}^{1,7,8}$  Researchers indicate that a modification layer, such as octadecyltrichlorosilane, placed between the SiO<sub>2</sub> gate dielectric and the pentacene active layer is an effective method allowing to achieve mobility above  $1.0 \text{ cm}^2/\text{V s.}^{7,8}$  The greatest research effort, by far, has been focused on the polymeric materials that have been used as a surface modification layer and/or dielectric layer in OTFTs.<sup>9</sup> For instance, Kelley et al. have reported high performance pentacene TFTs using polymeric ultrathin films as a surface modification with mobility above 5.0 cm<sup>2</sup>/V s.<sup>9</sup> In the report, researchers did not observe direct correlation between the surface morphology and resulting mobility. It is widely believed that the carrier transport efficiency is increased through the presence of well-ordered crystalline structure and/or the large grain size. At the same time, some of the

reported data are not consistent with the observations above.<sup>10-12</sup>

Previously, we have addressed surface-induced orientation of a pentacene film with electrical anisotropic properties using photoalignment polyimide method.<sup>13</sup> In this study, we have used a photosensitive polyimide (PSPI) that served as a modification layer upon SiO<sub>2</sub>. We have learned that *enhancement* of mobility was a combination of three related factors including the surface free energy of PSPI, the crystalline size, and the disorder of the pentacene film. Surface properties of PSPI can be managed by using photopolymer surfacemodifying coating and polarized ultraviolet light exposure. The technique above allows reaching the required nonpolarity that is needed to enhance field-effect mobility of pentacene TFTs. In the research, we also discuss possible origin of higher mobility in pentacene TFTs with PSPI modifications as compared to mobility observed in bare SiO<sub>2</sub>.

The device geometry and the sample fabrication were described previously and shown in Figs. 1(a) and 1(b).<sup>13</sup> *Fabricated* OTFT devices *had* a channel with a length of 120  $\mu$ m and a width of 1920  $\mu$ m. As shown in Fig. 1(a), a 100 nm PSPI (EA8001, Eternal Company) modification layer was deposited by spin coating directly onto a SiO<sub>2</sub> substrate. PSPI was irradiated with polarized ultraviolet (UV) beam with energy of 1 J to form the modification layer. Obtained modification layer featured the best in-plane anisotropic homogeneous liquid crystal (LC) alignment in a LC test cell (not show herein) used for the growth of 70 nm thick pentacene film. The electrical characteristics of TFTs were measured using a Keithley 4200-SCS semiconductor parameter analyzer in a dark chamber.

Several publications state that roughness of the gate dielectric has a distinct influence on the morphology and structural properties of pentacene films.<sup>3,4</sup> *Films* grown on smooth thermal oxide are generally more ordered and have a larger grain size. Table I presents surface roughness of the PSPI and SiO<sub>2</sub> dielectrics measured by atomic force microscope. We can see that the root-mean-square roughness (rms) of SiO<sub>2</sub>

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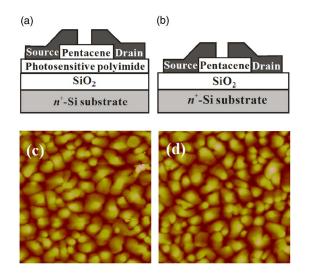


FIG. 1. (Color online) Cross section of OTFTs (a) with PSPI layer and (b) without PSPI layer. Atomic force microscope images of pentacene films deposited on (a) PSPI and (b) SiO<sub>2</sub> dielectrics. Two images are  $2 \times 2 \ \mu m^2$  in size.

surface is superior to the rms of the PSPI surface. The morphology of the pentacene thin films on PSPI and SiO<sub>2</sub> is shown in Figs. 1(c) and 1(d), respectively. The grain size of *both* samples is very similar, even though the PSPI dielectric has inferior roughness compared to the SiO<sub>2</sub> dielectric. This result is different from the previously reported analyses.<sup>3,4</sup> X-ray diffraction (XRD) spectroscopy was performed on the pentacene films to make an in-depth study of the differences in crystal structure between pentacene films grown on PSPI and SiO<sub>2</sub> surfaces. The XRD patterns of the pentacene deposited on the experimental gate dielectrics had five distinctively explicit reflections (00l), including thin-film phase (00l) and triclinic bulk phase (00l'), as shown in Fig. 2. Triclinic bulk phase was much weaker as compared to the thin-film phase observed in pentacene grown on the PSPI surface. Observations suggest that the pentacene grown on the PSPI surface has a better crystalline quality as compared to that grown on the SiO<sub>2</sub> surface. Crystalline parameters of the pentacene films, prepared on PSPI and  $SiO_2$  surfaces, were evaluated from paracrystal theory.<sup>14</sup> The investigated parameters included the size of the crystalline domain  $\overline{L}_{hkl}$ [the mean dimension of the crystallites perpendicular to the plane (hkl) and the degree of structural disorder  $g_{II}$  [the distance fluctuation between successive planes of the family (*hkl*) or second kind of distortions of crystal structure]. The calculated  $\bar{L}_{hkl}$  and  $g_{II}$  values are shown in Table I. Our re-

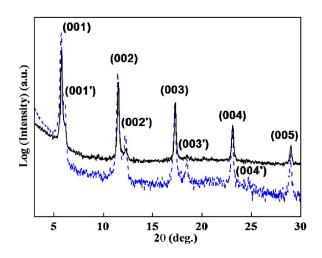


FIG. 2. (Color online) X-ray spectra of pentacene films grown on PSPI (solid line) and  $SiO_2$  (dash line) dielectrics.

sults indicate that the ordering of pentacene molecules increases significantly on the PSPI surface even if the surface has inferior rms roughness.

Figure 3(a) shows the output characteristics  $(I_{DS}-V_{DS})$  of TFTs produced with pentacene films deposited on the PSPI and SiO<sub>2</sub> gate dielectrics. The magnitude of  $I_{DS}$  produced by the devices with PSPI layer was significantly larger than that of the devices only with SiO<sub>2</sub> dielectric. Figure 3(b) shows a plot of the square root of  $I_{DS}$  as a function of  $V_{GS}$  for OTFTs with PSPI and SiO<sub>2</sub> gate dielectrics. Saturation field-effect mobility  $\mu_{sat}$  and threshold voltage  $V_{th}$  are measured for the OTFTs with the PSPI/SiO<sub>2</sub> dual layer and *native* SiO<sub>2</sub> layer by fitting the linear region between -20 and -40 V of  $V_{GS}$ and are *listed* in Table I. As we can see, insertion of the photosensitive layer into the OTFTs resulted in a drastic enhancement in the field-effect mobility and slight decrease of the threshold voltage.

To understand the mechanism driving the enhancement of the *field-effect mobility*, the contact angles (FACE contactangle meter, Kyowa Kaimenkagaku Co.) of two test liquids were measured. Water and di-iodomethane represented the test liquids measured on the surfaces of PSPI and SiO<sub>2</sub>. The contact angles of the test liquids are shown in Table I. Higher contact angle of the water on the PSPI indicates that PSPI's exposure to an appropriate dose of UV light makes the surface of the gate dielectric more nonpolar. Surface free energies of the PSPI and SiO<sub>2</sub> dielectrics obtained in the experiment are listed in Table I.<sup>15</sup> Decrease in the surface free energy on the surface of the PSPI dielectric *significantly* contributes to *enhance* mobility in OTFTs and consequently

TABLE I. Surface properties of gate dielectrics, crystal quality of pentacene films, and the electrical performance of the corresponding pentacene-based OTFTs.

	Surface properties of gate dielectric						Crystal quality of pentacene film		Device performance	
Gate dielectric	Surface roughness (nm)	Conta	act angle (deg)	$\gamma_s^{Pa}$ (mJ/m <sup>2</sup> )	$\gamma_s^{Da}$ (mJ/m <sup>2</sup> )	$\gamma_s^a$ (mJ/m <sup>2</sup> )	Crystalline size (Å)	Disorder (%)	$\mu_{\rm sat}$ (cm <sup>2</sup> /V s)	V <sub>th</sub> (V)
PSPI/SiO <sub>2</sub> SiO <sub>2</sub>	0.75 0.48	89.5 58.5	45.3 46.6	1.4 14.7	36.8 36.2	38.2 50.9	435 343	1.23 1.96	2.05 0.11	-15.3 -19.1

 $a^{a}\gamma_{s}$  is solid surface free energy, and  $\gamma_{s}^{p}$  and  $\gamma_{s}^{D}$  are the polar and dispersion force components of solid surface free energy, respectively. Downloaded 26 Oct 2008 to 140.116.208.46. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

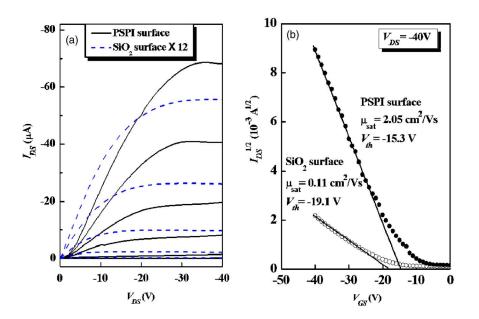


FIG. 3. (Color online) (a) Output characteristics of the pentacene OTFTs with a PSPI/SiO<sub>2</sub> dual-layer gate dielectric (solid line) and a SiO<sub>2</sub> gate dielectric, respectively. (b) The saturated transfer characteristics  $(I_{DS}^{1/2}-V_{GS})$  of pentacene OTFTs at  $V_{DS}$ =-40 V.

slightly decreases the threshold voltage, as discussed below.

Recently, a thickness driven orthorhombic thin-film phase to triclinic bulk phase transformation is suggested in pentacene thin films.<sup>16</sup> In our study, the orthorhombic thinfilm phase crystal structure was grown at low film thickness. As increasing the thickness of pentacene until a critical thickness ( $\sim$ 30 nm) is reached, the triclinic phase starts to form. The surface free energy values were 38 mJ/m<sup>2</sup> for orthorhombic phase and 76 mJ/m<sup>2</sup> for triclinic phase.<sup>16</sup> Interestingly, the surface free energy of PSPI in this study matched the energy of the pentacene orthorhombic thin-film phase. However, the surface free energy of SiO<sub>2</sub> significantly deviated from the value recorded in orthorhombic thin-film phase. Thus, pentacene grown on low surface energy PSPI layer retains the first pentacene layer better and keeps it from some voids and successive incomplete layers over the first case, which limits the transport of carriers near the gate dielectric, consequently resulting in high carrier mobility. These conditions are determinant factor behind large crystalline size and low structural disorder in pentacene film grown on PSPI (see Table I). On the other hand, several publications *refer to* reduction in mobility due to increased surface roughness of the gate dielectric.<sup>3,4,12</sup> However, *in our case*, PSPI has inferior rms roughness and the morphology of the pentacene films grown on these gate dielectrics is rather similar, despite the fact that the surface free energy is different. Yang et al.<sup>5</sup> have reported that the average grain size becomes smaller as the surface free energy of gate dielectrics decreases which are different from our experimental results. Hence, we can exclude the assumptions suggesting that performance of OTFTs is influenced by the surface morphology of the pentacene film and surface roughness in different types of gate dielectrics. In fact, the surface free energy of the PSPI can be manipulated by regulating the dose of UV light exposure. Initially, we came to the conclusion above when the surface energy for the PSPI measured  $38 \text{ mJ/m}^2$ thus matching the surface free energy of the orthorhombic phase pentacene and *resulting* in optimized performance in OTFTs. Further investigation of the mechanism for changing surface free energy in PSPI is underway.

During the experiment we have fabricated high performance pentacene-based OTFTs using the PSPI as a modification layer on gate dielectric. The maximum saturation field-effect mobility was above 2.0 cm<sup>2</sup>/V s. We believe that a gate dielectric with low surface free energy can contribute to enhance carrier mobility in pentacene OTFTs, increase crystalline size, and decrease crystal disorder in pentacene films.

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