


## Article

# Effect of Thickness of InP Nucleation Layer on the Two-Step Growth of InP on Si(001)

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**Abstract:** InP nucleation layers with different thicknesses were grown on Si(001) substrates by gas-source molecular beam epitaxy (GSMBE), and the two-step growth technique was used to overcome the large lattice mismatch (8%) between the InP nucleation layer and Si substrate. The surface morphology and microstructure were investigated by using an atomic force microscope (AFM) and transmission electron microscopy (TEM). High-resolution X-ray diffraction (HR-XRD) measurements were carried out to characterize the crystal quality. It was found that a too thin nucleation layer will lead to an uneven distribution of atoms on the surface, resulting in a poor crystalline quality of the InP epitaxial layer. The thicker the low-temperature nucleation layer is, the better the crystallization quality of the InP high-temperature layer will be.

**Keywords:** InP on Si; two-step growth method; nucleation layer; thickness



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## 1. Introduction

Recently, a growing number of researchers have shown a great interest in tightly combining the superior material properties of compound semiconductor (CS) materials with the integration density of a silicon (Si) complementary metal-oxide semiconductor (CMOS) [1–3]. The main reason is that the circuit performance can be greatly optimized by integrating several III-V functional blocks with Si CMOS transistors or cells on the same silicon substrate and using standard semiconductor on-wafer interconnect processes [4–6].

Due to the highest reported RF figures-of-merit, indium phosphide (InP) based electronic technologies are well suited for signal amplification in the THz frequency regime, which has exhibited more extraordinary superiorities than Silicon-based devices in the microwave and millimeter-wave applications [7–9]. A variety of integration methods for heterogeneous integration of InP HBTs (heterojunction bipolar transistors) with Si CMOS have been used to realize ultrahigh-speed mixed-signal circuits: monolithic integration of InP-based transistors on Si [10], InP epitaxial transfer on top of the CMOS interconnect stack [11], fine-pitch bonding of InP chiplets on CMOS wafers [12]. Although it is easier to implement flip-chip bonding and micro-transfer printing based on the existing technologies, its integration has been greatly limited by interconnect sizes and losses, chip and transfer-layer sizes, and the complexity of manufacture. Compared with these two integrated techniques, direct epitaxial growth has a smaller interconnect size and higher integration and is capable of giving full play to the superiorities of heterogeneous integration [10], which has been regarded as the most integrated promising technique in the future.

However, several fundamental challenges have limited the quality of metamorphic III-V layers on Si, including the large lattice mismatch and thermal expansion coefficients, as well as the growth of polar materials on non-polar substrates [13]. In order to deal with these problems, a two-step growth technique has often been adopted in the growth of highly mismatched heterostructures, in which the nucleation layer grows at a relatively low temperature and is then followed by a higher temperature to grow the

target material. This technique was generally adopted by two methods: one is known as metalorganic chemical vapor deposition (MOCVD) [14], and the other one is molecular beam epitaxy (MBE) [15]. The use of two-step growth in highly mismatched heterostructures (such as GaN/Al<sub>2</sub>O<sub>3</sub> [16,17], GaN/SiC [18], InSb/Si [19], In<sub>0.78</sub>Ga<sub>0.22</sub>As/GaAs [15], InP/GaAs [20], etc.) has a significant influence on surface morphology and crystal quality of the epitaxial layers. Moreover, many pieces of research have paid attention to the effects of growth parameters of V/III sources of Ge [21] or GaAs [22] nucleation layer on Si, or InP nucleation layer on GaAs [23,24] or Si [25] by MOCVD, and MBE systems were also increasingly applied in the heterogeneous epitaxy, finding that the quality of the nucleation layer has a huge effect on the crystallinity of overall hetero-epitaxial layers. Although MBE systems have been increasingly used for the preparation of heterogeneous epitaxy, especially in III–V semiconductors [26–28], the effect of the growth parameter of the InP nucleation layer in the period of growing InP epilayers on Si substrates has not been fully investigated and understood.

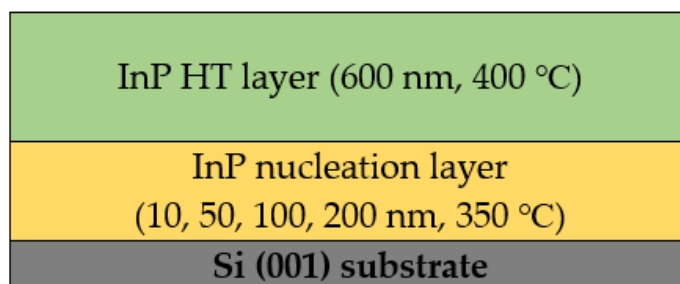
In our previous works, the two-step technique had been demonstrated to be effective for the InP/Si growth, and we had experimentally studied the optimum growth temperature of the InP nucleation layer of the epitaxial layer [29], but without further studying on the influence of the thickness of the InP nucleation layer. Therefore, efforts should be made to further investigate the growth parameters of the InP nucleation layer and the mechanism of Si-based InP to realize the high-performance heteroepitaxy integrated circuit of InP HBT and Si CMOS.

In this paper, we grew InP epilayers with different InP nucleation layer thicknesses on Si(001) substrates by using a gas-source MBE (GSMBE) system, and the two-step growth technique was used to overcome the large lattice mismatch (8%) and thermal mismatch (the bulk thermal expansion coefficients of InP and silicon are  $5 \times 10^{-6}/\text{K}$  and  $2.3 \times 10^{-6}/\text{K}$ , respectively) between the InP nucleation layer and Si substrate. The purpose was to analyze how the crystal quality was affected by the nucleation layer thicknesses. The surface morphology and microstructure of the grown InP epilayers were investigated by an atomic force microscope (AFM) and transmission electron microscopy (TEM), and the crystal quality was performed with high-resolution X-ray diffraction (HR-XRD) measurements. The experimental results indicate that the thickness of the InP nucleation layer has a significant effect on both the InP surface morphology and crystal quality of InP epilayers. More details of our work are described in the following sections.

## 2. Experimental Section

All the samples in this study were grown on 2-inch (100)-oriented silicon substrates by using a VG Semicon V90H GSMBE system. The experimental processes are as follows: Initially, the Si(001) substrates were chemically cleaned for 30 s with buffered oxide etch (BOE) solution in which the ratio of HF and NH<sub>4</sub>F is 1:6, whose purpose is to remove the oxide layer before the epitaxial growth. Next, it was rinsed in de-ionized water and then dried with nitrogen, and then, the Si substrates were annealed in the MBE chamber at 625 °C for 30 mins to remove the surface residual oxide, which was monitored by a high energy electron diffraction (RHEED) system. After that, the temperature was reduced to 350 °C for the growth of the low-temperature nucleation layer, and the group V and III sources are Phosphorus (PH<sub>3</sub>) cracking cell and indium, respectively. Then, InP nucleation layers with different thicknesses were grown on Si(001) substrates whose thickness was controlled by the growth time: 1 min 9 s (10 nm), 5 min 47 s (50 nm), 11 min 34 s (100 nm) and 21 min 9 s (200 nm). The growth time was calculated by the growth rate of InP, which is approximately 1.44 Å/s. After these steps, the substrate temperature was increased up to 400 °C at a rate of 0.5 °C/s to growth high temperature (HT) InP layer with the thickness of 600 nm (69 min 26 s). Finally, in order to evaluate the effect of different nucleation layer thickness on the quality of heteroepitaxial layer, we used HR-XRD to investigate the crystal quality, used AFM to examine the microstructure of InP-Si surface, and adopted TEM to

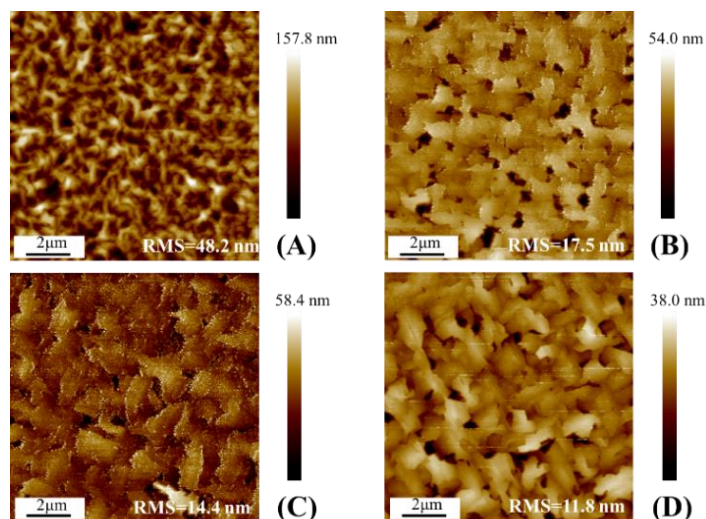
study the distribution of dislocations caused by large lattice mismatch. Figure 1 shows the schematic diagram of InP direct heterogeneous epitaxial growth on Si(001) substrates.



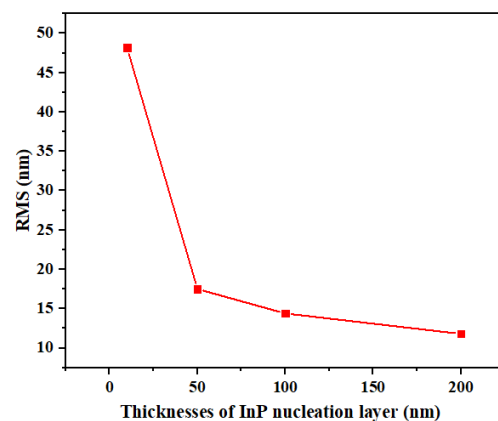
**Figure 1.** Schematic of InP epitaxial structures on Si(001) substrate.

### 3. Results and Discussion

Figure 2 shows the surface morphology images of InP epilayers with different thicknesses of InP nucleation layer grown on Si substrates received from AFM in a  $10 \times 10 \mu\text{m}^2$  scanning area. The InP nucleation layer thickness of four samples was 10 nm, 50 nm, 100 nm, and 200 nm, corresponding to samples A, B, C, and D, respectively. The root-mean-square (RMS) values of the surface roughness are 48.2, 17.5, 14.4, and 11.8 nm for samples A, B, C, and D, respectively, which means that the thickness of the InP nucleation layer is a critical factor determining surface morphology. The RMS results measured by AFM are plotted as a function of the thickness of the InP nucleation layer, which is shown in Figure 3. It can be found that with the InP nucleation layer thicknesses increase, the surface roughness of epitaxial layers decreases, which reveals that the InP nucleation layer grown with 200 nm has the best crystalline quality compared with other samples.

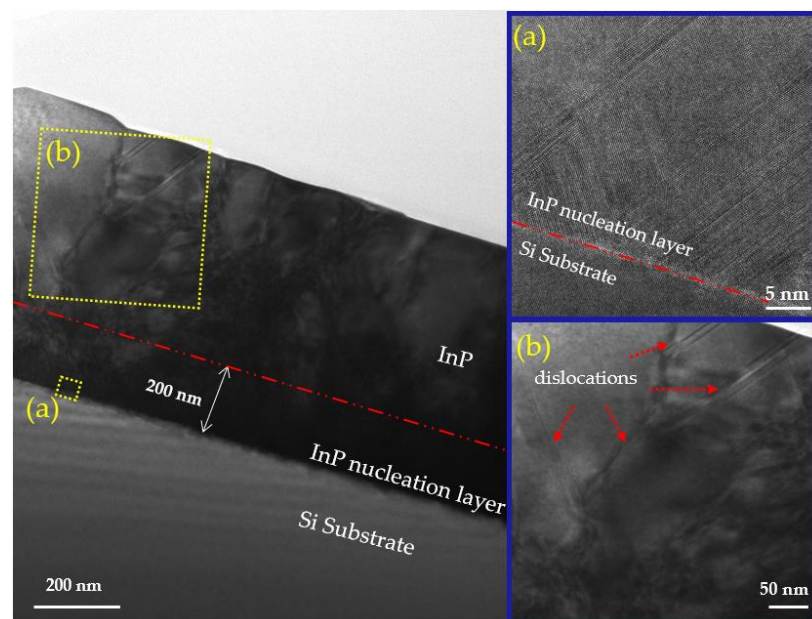


**Figure 2.** AFM images of the different thickness of InP epilayer grown at 350 °C: (A) 10 nm, (B) 50 nm, (C) 100 nm, and (D) 200 nm.



**Figure 3.** Plot of the RMS roughness of InP films versus different thicknesses of InP nucleation layer.

TEM was used to investigate the microstructure of InP epilayers with 200 nm InP nucleation layer thickness. Because of the large lattice mismatch between the InP nucleation layer and Si substrate, it can be found that the InP nucleation layers tend to release the strain energy by an island growth: at the initial growth stage, the morphology of InP epilayers was changed from near-amorphous morphology to large islands with different sizes, and the phenomenon of island merging is obvious in Figure 4a. Meanwhile, many mismatched dislocations were generated in these islands during growth, which propagated to the surface of the material with the growth of the high-temperature InP layer, reducing the material quality of the crystal (Figure 4b).



**Figure 4.** (a,b) Cross-sectional TEM images of the InP nucleation layers grown on Si(001).

The main reason for this phenomenon is that the migration power of the surface atoms is greatly reduced by the excessively low growth temperature, particularly for the indium atoms, which possess a bigger atomic radius and mass. Therefore, a too-thin thickness of the InP nucleation layer will cause an uneven distribution of atoms on the surface, resulting in a large number of island structures. However, as the thickness of the low-temperature nucleation layer increases, the island structure becomes larger and merges, decreasing the number of defects, and the surface morphology gradually becomes smooth. Therefore, the thicker the low-temperature nucleation layer is, the better the crystallization quality of the InP high-temperature layer will be. Moreover, after growing the low-temperature

nucleation layer, it is usually annealed at a high temperature, which is similar to the principle of increasing the growth thickness. Both approaches can decrease the number of defects and make the surface smoother. Therefore, considering the growth time and cost, we believe that it is unnecessary to grow the nucleation layer too thick. After the growth of the nucleating layer, annealing at a high temperature for a period of time can not only improve the crystallization quality by achieving the same effect as increasing the growth thickness but also reduce the growth time and improve the experimental efficiency.

HR-XRD scan curves of different thicknesses of the InP nucleation layer on Si(001) are shown in Figure 5. It is observed that with the InP nucleation layer thickness increased from 10 nm to 200 nm, the peak intensity increased, and the FWHM values decreased, which indicates the crystal quality became better. Furthermore, according to the HR-XRD measurements, the extracted peak intensity and full width at half maximum (FWHM) of four samples are listed in Table 1, and the following formula can be used to describe the relationship between the FWHM and the thread dislocation density (TDD) [30].

$$N_{\text{dis}} = \frac{(\text{FWHM})^2}{9b^2} \quad (1)$$

where  $N_{\text{dis}}$  is dislocation density, FWHM is in radians whose value is summarized in Table 1,  $b$  is Burgers vector of materials. Compared to the other samples, sample D with 200 nm InP nucleation layer shows the smallest FWHM and the minimum TDD value, which provides the best crystalline quality, indicating that the quality of the overall InP film has been significantly influenced by the thickness of the nucleation layer, and as the thickness of nucleation layer increases, the quality of epitaxial layer becomes better.

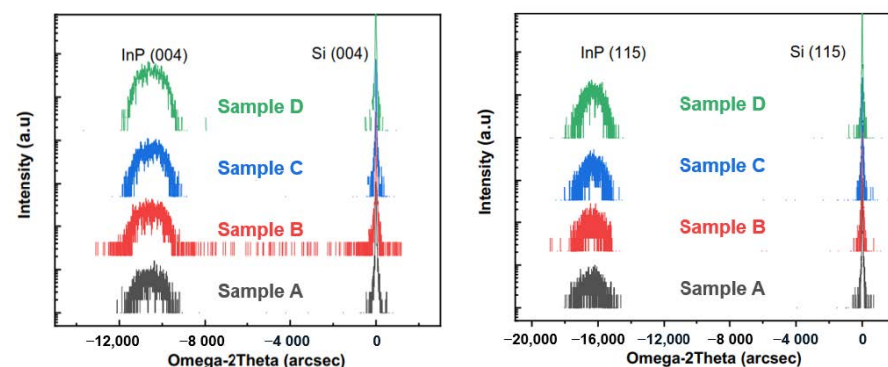


Figure 5. (004) and (115) omega-2theta HR-XRD scan curves for all Samples.

Table 1. Intensity and FWHM of (004) and (115) Bragg peaks for all samples.

Sample	Intensity of 004 (a.u)	FWHM of 004 (arcsec)	Intensity of 115 (a.u)	FWHM of 115 (arcsec)
A	75	1400.76	68	21,619.11
B	138	1353.6	86	1806.8
C	155	1178.28	125	1639.5
D	394	901.44	221	1464.3

#### 4. Conclusions

The InP epilayers with different nucleation layer thicknesses were grown on Si(001) substrates, which were fabricated by using the two-step growth technique. In our experiment, we find that a too thin nucleation layer will lead to an uneven distribution of atoms on the surface, resulting in a poor crystalline quality of the InP epitaxial layer and surface roughness of InP epilayer decreased by increasing the thickness of the InP nucleation layer. The best results are achieved with the nucleation layer thickness of 200 nm, which has the smoothest surface morphology, the biggest intensity, and the minimum FWHM of (004) and

(115) Bragg peaks. Meanwhile, the results of the XRD and AFM analysis all illustrate that: the thicker the low-temperature nucleation layer is, the better the crystallization quality of the InP high-temperature layer will be.

**Author Contributions:** Conceptualization, S.Y. (Silu Yan); Methodology, S.Y. (Silu Yan); Validation, S.Y. (Silu Yan) and S.Y. (Shizheng Yang); Formal analysis, S.Y. (Silu Yan) and S.Y. (Shizheng Yang); Investigation, S.Y. (Silu Yan) and S.Y. (Shizheng Yang); Resources, H.L. and Y.Z.; Data curation, S.Y. (Silu Yan) and S.Y. (Shizheng Yang); Visualization, S.Y. (Silu Yan) and S.Y. (Shizheng Yang); Supervision, H.L. and Y.Z.; Project administration, H.L.; Funding acquisition, H.L. and Y.Z.; Writing—original draft, S.Y. (Silu Yan); Writing—review and editing, H.L. and S.Y. (Shizheng Yang). All authors have read and agreed to the published version of the manuscript.

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