Effect of Valley Switching and Switching-Frequency Limitation on Line-Current Distortions of DCM/CCM Boundary Boost PFC Converters

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***Abstract*—A systematic analysis of line-current distortions of the discontinuous-conduction-mode and the continuous-conduction-mode boundary boost power factor correction converter due to valley switching (VS) and switching-frequency limitation, where VS is either maintained or lost after the onset of switching-frequency limitation, is provided. Closed-form expressions for the line current are derived. It is shown that if the switching frequency is limited and VS is not maintained, the line current is more distorted with voltage-mode control than with current-mode control. The effects of line-current distortions are demonstrated with both simulation and experimental results.**

***Index Terms*—Boost converter, discontinuous conduction mode (DCM)/continuous conduction mode (CCM) boundary, line-current distortion, power factor correction (PFC), single-phase rectifier, switching-frequency limitation, valley switching (VS).**

I. Introduction

IN LOW-POWER offline power supplies, a boost converter (see Fig. 1) operating at the boundary of the discontinuous conduction mode (DCM) and continuous conduction mode (CCM) is a popular topology for implementing the front-end converter with active power factor correction (PFC) [1]–[9]. The major benefit of the DCM/CCM boundary boost converter, compared to the CCM boost converter, is that the reverse recovery losses related to the boost diode are eliminated [12]. In addition, turn-on with zero-voltage switching (ZVS) or near ZVS of the boost switch, also called valley switching (VS), can be easily achieved [9]–[11]. VS is due to the resonance between the parasitic capacitances of the boost switch and boost diode with the boost inductor after the demagnetization of the boost inductor. Neither the CCM nor the DCM boost PFC converter, which operate with a constant switching frequency, can achieve ZVS without an additional active snubber circuit [12]. Other benefits of the DCM/CCM boundary boost PFC converter compared to the constant-switching-frequency DCM boost PFC converter [13], [14] are a lower total harmonic distortion (THD) of the line current and a smaller peak inductor current resulting in lower turn-off switching losses and lower conduction losses. A major drawback of the DCM/CCM boundary boost PFC converter is that its switching frequency, which changes as a function of line and load, varies over a wide range leading to excessive turn-off switching loss of the main switch, as well as excessive core and winding losses of the inductor. This becomes a significant problem at light loads, where most consumer products are required to meet the U.S. Environmental Protection Agency (EPA) Energy Star standards [15] and/or the Climate Savers Computing Initiative program [16]. Generally, switching losses can be controlled by limiting the switching frequency. However, by limiting the switching frequency, the line current becomes distorted resulting in decreased power factor (PF) and increased THD. In addition, ZVS of the main switch can be lost, which degrades the efficiency and leads to excessive electromagnetic interference (EMI) noise, and therefore, additional input filtration is needed.

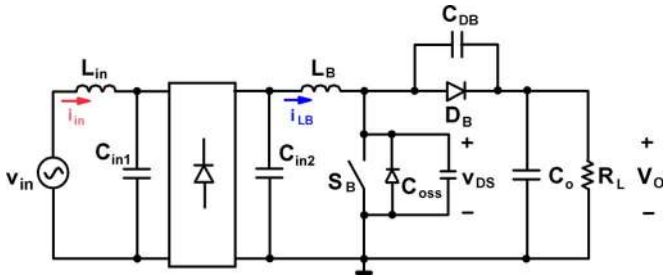

Fig. 1. Simplified circuit diagram of the PFC boost converter.

This paper presents a systematic analysis of the line-current distortions of the DCM/CCM boundary boost PFC converter due to VS and switching-frequency limitation. The effects of line-current distortions are demonstrated with both simulation and experimental results.

II. Analysis of Line-Current Distortions

When the boost converter (see Fig. 1) operates at the DCM/CCM boundary with a constant on-time $T_{\rm ON}$ of boost switch S_B, the line current follows the line voltage. In fact, line current $i_{\rm in}$ can be approximated as inductor current i_{LB} averaged over a switching period $T_{\rm sw}$, i.e.,

$$i_{\rm in}(t) \approx i_{\rm in}(t_k) = \langle i_{LB}(t) \rangle_{T_{{\rm sw},k}} = \frac{v_{\rm in}(t_k) T_{\rm ON}}{2L_B} \qquad (1)$$

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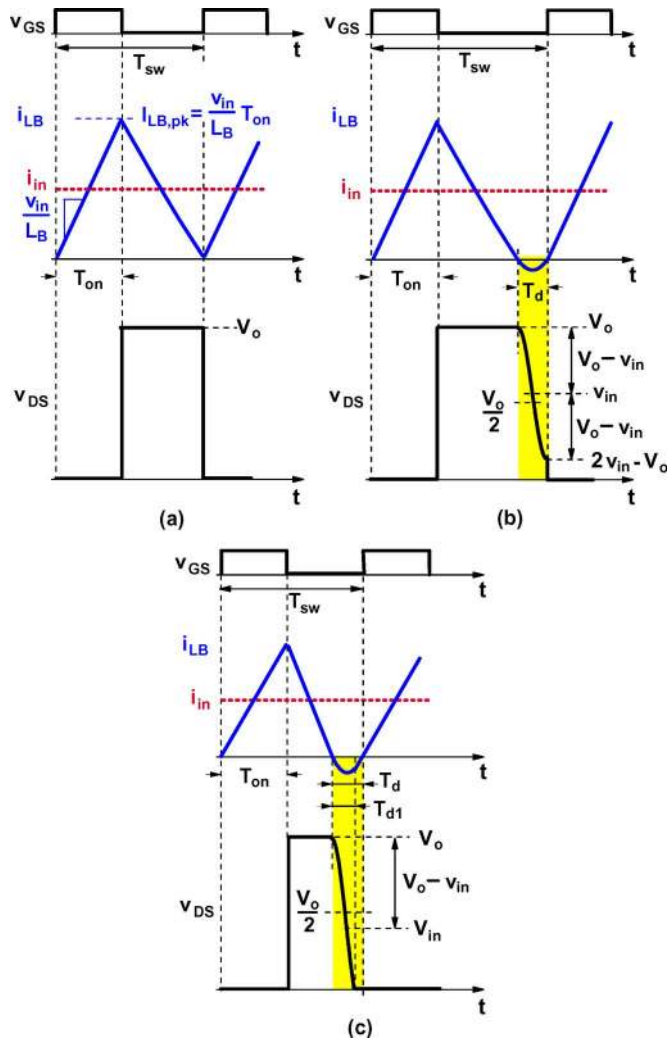

Fig. 2. Key switching waveforms of DCM/CCM boundary operation. (a) Without delay. (b) With delay T_d when $v_{\rm in} > V_o/2$. (c) With delay T_d when $v_{\rm in} < V_o/2$.

where t_k is the sampling instant of the line voltage $v_{\rm in}(t) = \sqrt{2}\,V_{\rm in,rms}\sin(\omega_L t)$ in the kth switching period $T_{{\rm sw},k}$ during a line cycle. As the switching frequency is much larger than the line frequency, the line voltage and the line current can be considered constant over a switching cycle (quasi-static approach). Therefore, for simplicity, subscript k is neglected throughout the remainder of the paper.

In (1), on-time $T_{\rm ON}$ is determined as

$$T_{\rm ON} = \frac{2L_B P_o}{\eta V_{\rm in,rms}^2} \tag{2}$$

where $\eta = P_o/P_{\rm in}$.

However, operating at the DCM/CCM boundary, boost switch S_B turns on with hard switching, as shown in Fig. 2(a), resulting in elevated turn-on losses. The turn-on losses can be significantly reduced or even completely eliminated if the turn-on instant of switch S_B is delayed until its drain–source voltage v_{DS} resonates down to a valley (when $v_{\rm in} > V_o/2$) or to zero (when $v_{\rm in} < V_o/2$), as shown in Fig. 2(b) and (c), respectively. This additional delay T_d is due to the parasitic capacitances of the boost switch $C_{\rm oss}$ and boost diode C_{DB}, resonating with boost inductor L_B. As follows from Fig. 2(b), delay T_d is determined as one-half of the resonant period, i.e.,

$$T_d = \pi\sqrt{L_B\,(C_{\rm oss} + C_{DB})}. \tag{3}$$

It should be noted that delay T_d does not depend on filter capacitance $C_{\rm in2}$ and the parasitic capacitance of the full-bridge diodes. In fact, since capacitance $C_{\rm in2}$, which is located at the output of the full-bridge rectifier as shown in Fig. 1, is much larger than the parasitic capacitance of the bridge diodes, the effect of the parasitic capacitance of the bridge diodes can be neglected in the resonant circuit. Furthermore, since capacitance $C_{\rm in2}$ is connected in series with the parasitic capacitances of the boost switch and boost diode and $C_{\rm in2} \gg (C_{\rm oss} + C_{DB})$, its effect on the resonant period can be neglected.

This additional delay T_d increases the turn-off time of the switch and introduces line-current distortions, i.e.,

$$i_{\rm in}(t) = \frac{v_{\rm in}(t)T_{\rm ON}}{2L_B}\,\frac{1}{1 + (T_d/T_{\rm ON})\,[1 - (v_{\rm in}(t)/V_o)]}. \tag{4}$$

The expression for the line current in (4) is obtained by neglecting the negative portion of the boost inductor current during interval T_d. If the negative portion of the boost inductor current is not negligible, the line current is more distorted, i.e., as shown in (5) at the bottom of this page, where

$$k_{Td}(t) = \frac{[(2/\pi)(T_d/T_{\rm ON})\,(1 - (v_{\rm in}(t)/V_o))]^2}{v_{\rm in}(t)/V_o}, \quad \text{when } v_{\rm in}(t) \geq \frac{V_o}{2} \tag{6}$$

and

$$k_{Td}(t) = \left(\frac{T_d}{T_{\rm ON}}\right)^2 \frac{1 - [v_{\rm in}(t)/V_o]}{[v_{\rm in}(t)/V_o]}\left[\frac{2}{\pi^2} + \left(1 - \frac{T_{d1}(t)}{T_d}\right) \times \left(\sqrt{1 - 2\frac{v_{\rm in}(t)}{V_o}} - \frac{v_{\rm in}(t)}{V_o}\left(1 - \frac{T_{d1}(t)}{T_d}\right)\right)\right], \quad \text{when } v_{\rm in}(t) < \frac{V_o}{2} \tag{7}$$

where

$$\frac{T_{d1}(t)}{T_d} = \frac{1}{\pi}\,{\rm acos}\left(\frac{v_{\rm in}(t)/V_o}{(v_{\rm in}(t)/V_o) - 1}\right). \tag{8}$$

$$i_{\rm in}(t) = \begin{cases} \dfrac{v_{\rm in}(t)T_{\rm ON}}{2L_B}\,\dfrac{1}{1 + (T_d/T_{\rm ON})\,[1 - (v_{\rm in}(t)/V_o)]}\,(1 - k_{Td}(t)), & \text{if } k_{Td}(t) < 1 \\ 0, & \text{if } k_{Td}(t) \geq 1 \end{cases} \tag{5}$$

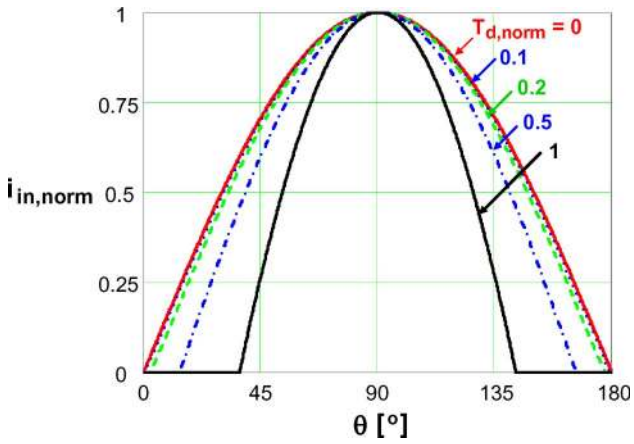

Fig. 3. Normalized line current waveforms as a function of normalized delay time $T_{d,\mathrm{norm}}$ at 115-$\mathrm{V_{rms}}$ line voltage and 385-V output voltage.

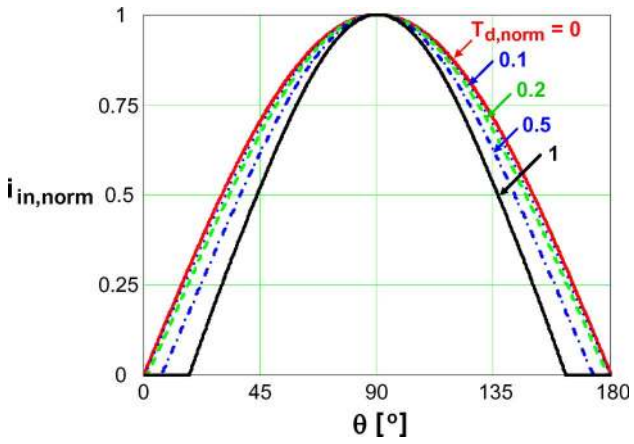

Fig. 4. Normalized line current waveforms as a function of normalized delay time $T_{d,\mathrm{norm}}$ at 230-$\mathrm{V_{rms}}$ line voltage and 385-V output voltage.

Interval T_{d1} in (8) is the resonant interval before the body diode of switch S_B starts to conduct when $v_{\mathrm{in}} < V_o/2$, as shown in Fig. 2(c).

The negative portion of the boost inductor current during interval T_d can be neglected if $k_{Td}(t) \ll 1$. It follows from (6) and (7) that the negative portion of the boost inductor current during T_d is negligible if

$$\frac{T_d}{T_{\mathrm{ON}}} \ll \frac{\pi}{2}\frac{\sqrt{v_{\mathrm{in}}(t)/V_o}}{1-(v_{\mathrm{in}}(t)/V_o)}, \quad \text{when } v_{\mathrm{in}}(t) \geq \frac{V_o}{2} \tag{9}$$

and, as shown (10), at the bottom of this page.

Normalized line current waveforms as a function of the normalized delay time ($T_{d,\mathrm{norm}} = T_d/T_{\mathrm{ON}}$) at 115-$\mathrm{V_{rms}}$ and 230-$\mathrm{V_{rms}}$ line voltages (nominal low and high line voltages), at 385-V output voltage, are presented in Figs. 3 and 4, respectively. It follows from (4)–(10) and Figs. 3 and 4 that delay time T_d related line-current distortions are more pronounced around the zero crossing of the line voltage v_{in} and at light loads where T_{ON} is smaller. Generally, the negative portion of the boost inductor current during T_d can be neglected close to full load.

TABLE I
PF AND THD VERSUS NORMALIZED DELAY TIME AT NOMINAL LOW AND HIGH LINE VOLTAGES ($V_o = 385$ V)

$V_{in,rms}$ [V]	$T_{d,norm} = T_d/T_{on}$	0	0.1	0.2	0.5	1
115	PF	1	0.9999	0.9993	0.9873	0.9062
	THD [%]	0	1.3	3.7	16.1	46.7
230	PF	1	0.9999	0.9994	0.9949	0.9761
	THD [%]	0	1.6	3.4	10.1	22.3

The line-current distortion can be quantitatively expressed by the PF defined as

$$\mathrm{PF} = \frac{P_{\mathrm{in}}}{V_{\mathrm{in,rms}} I_{\mathrm{in,rms}}} \tag{11}$$

and the THD, which is related to PF as

$$\mathrm{THD} = \sqrt{\frac{\cos^2(\theta)}{\mathrm{PF}^2} - 1} \tag{12}$$

where θ is the displacement angle between the line voltage and the fundamental component of the line current. PF and THD values corresponding to the line current waveforms in Figs. 3 and 4 are shown in Table I. It should be noted that in the aforementioned analysis, the phase shift between the line voltage and line current, which is caused by the input filter, is neglected. Therefore, $\cos(\theta) = 1$. It can be concluded from Figs. 3 and 4 and Table I that with the same normalized delay times, line-current distortions are smaller at 230-$\mathrm{V_{rms}}$ line voltage than at 115-$\mathrm{V_{rms}}$ line voltage. However, since at 230-$\mathrm{V_{rms}}$ line voltage, on-time T_{ON} is four times smaller than at 115-$\mathrm{V_{rms}}$ line voltage, as follows from (2), and therefore, the normalized delay time at 230-$\mathrm{V_{rms}}$ line voltage is four times greater than at 115-$\mathrm{V_{rms}}$ line voltage; generally, delay time T_d related line-current distortions are more pronounced at 230-$\mathrm{V_{rms}}$ line voltage than at 115-$\mathrm{V_{rms}}$ line voltage. For example, it can be seen in Figs. 3 and 4 that the line current at 230-$\mathrm{V_{rms}}$ line voltage and $T_{d,\mathrm{norm}} = 0.5$ (dashed–dotted waveform in Fig. 4) is more displaced from the ideal waveform than the corresponding line current at 115-$\mathrm{V_{rms}}$ line voltage and $T_{d,\mathrm{norm}} = 0.125$ (dot waveform in Fig. 3).

When the boost converter operates at the DCM/CCM boundary with constant on-time T_{ON}, the switching frequency changes as

$$f_{\mathrm{sw}} = \frac{1}{T_{\mathrm{ON}}}\left(1 - \frac{v_{\mathrm{in}}}{V_o}\right). \tag{13}$$

Using (2), the switching frequency is determined as

$$f_{\mathrm{sw}} = \eta\frac{V_{\mathrm{in,rms}}^2}{2L_B P_o}\left(1 - \frac{v_{\mathrm{in}}}{V_o}\right). \tag{14}$$

$$\frac{T_d}{T_{\mathrm{ON}}} \ll \sqrt{\frac{1}{(2/\pi^2) + (1-(T_{d1}(t)/T_d))\left(\sqrt{1-2(v_{\mathrm{in}}(t)/V_o)} - (v_{\mathrm{in}}(t)/V_o)(1-(T_{d1}(t)/T_d))\right)}}\frac{(v_{\mathrm{in}}(t)/V_o)}{1-(v_{\mathrm{in}}(t)/V_o)}, \quad \text{when } v_{\mathrm{in}}(t) < \frac{V_o}{2} \tag{10}$$

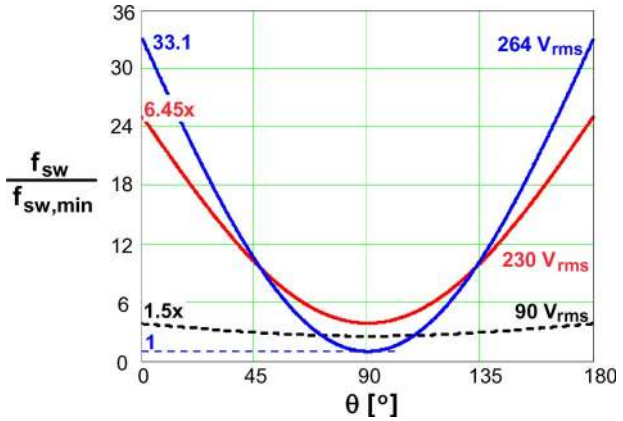

Fig. 5. Switching frequency variation over a half-line cycle at 385-V output voltage and a constant load normalized to the minimum switching frequency.

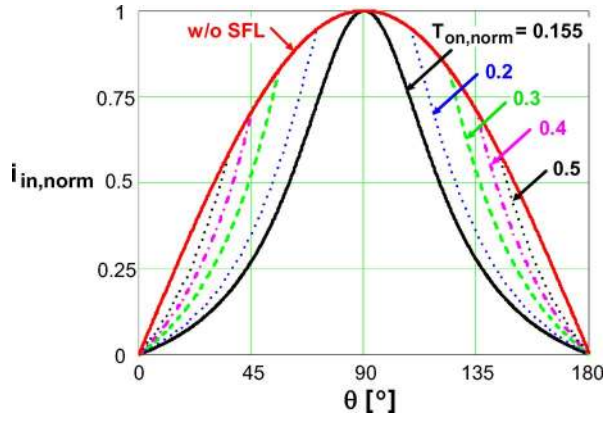

Fig. 6. Normalized line current waveforms for different SFLs, i.e., as a function of normalized on-time $T_{\mathrm{ON,norm}} = T_{\mathrm{ON}} f_{\mathrm{sw,max}}$ at 230-$\mathrm{V_{rms}}$ line voltage and 385-V output voltage.

The switching frequency variation over a half-line cycle at 385-V output voltage and a constant load normalized to the minimum switching frequency, for three rms values of the line voltage, is presented in Fig. 5. It should be noted that the minimum switching frequency is obtained at the peak of the maximum rms line voltage, i.e., $V_{\mathrm{in,rms}} = 264$ V. It follows from Fig. 5 that the switching frequency varies 1.5, 6.45, and 33.1 times at 90-, 230-, and 264-$\mathrm{V_{rms}}$ line voltage, respectively. Therefore, the total variation of the switching frequency in Fig. 5 is equal to its variation at the maximum rms line voltage. Furthermore, a ten times change in load will lead to approximately a ten times change in the switching frequency. At light loads, the switching frequency can become very high, and therefore, it is desirable to limit it in order to decrease the switching losses, which include the boost switch turn-off, and eventually, turn-on losses, gate drive loss, and the inductor core and copper losses.

When operating with a switching frequency limit (SFL), generally, the boost switch can operate with or without VS. If operating with VS, the boost switch can maintain VS, or it can lose VS after the onset of the SFL, depending on the employed control method.

If an SFL is implemented and the boost switch always operates without VS, the line current is determined as

$$i_{\mathrm{in}} = \begin{cases} \dfrac{v_{\mathrm{in}} T_{\mathrm{ON}}}{2L_B}, & \text{if } \dfrac{v_{\mathrm{in}}}{V_o} > 1 - T_{\mathrm{ON}} f_{\mathrm{sw,max}} \\ \dfrac{v_{\mathrm{in}} T_{\mathrm{ON}}}{2L_B} \dfrac{T_{\mathrm{ON}} f_{\mathrm{sw,max}}}{1 - (v_{\mathrm{in}}/V_o)}, & \text{if } \dfrac{v_{\mathrm{in}}}{V_o} \le 1 - T_{\mathrm{ON}} f_{\mathrm{sw,max}}. \end{cases} \tag{15}$$

Normalized line current waveforms as a function of the normalized on-time ($T_{\mathrm{ON,norm}} = T_{\mathrm{ON}} f_{\mathrm{sw,max}}$) at 230-$\mathrm{V_{rms}}$ line voltage and 385-V output voltage are presented in Fig. 6. It should be noted that the switching frequency is typically limited in the high-line-voltage range.

PF and THD values corresponding to the line current waveforms in Fig. 6 are shown in Table II. It can be seen in Table II that in the case where the switching frequency is limited in the entire half-line cycle, PF and THD are limited to 0.9369 and 37.3%, respectively.

TABLE II
PF AND THD VERSUS NORMALIZED ON TIME AT 230-$\mathrm{V_{rms}}$ NOMINAL HIGH LINE VOLTAGE ($V_o = 385$ V)

$T_{on,norm} = T_{on} f_{sw,max}$	≤ 0.155	0.2	0.3	0.4	0.5
PF	0.9369	0.9555	0.9828	0.9937	0.9979
THD [%]	37.3	30.9	18.8	11.3	6.5

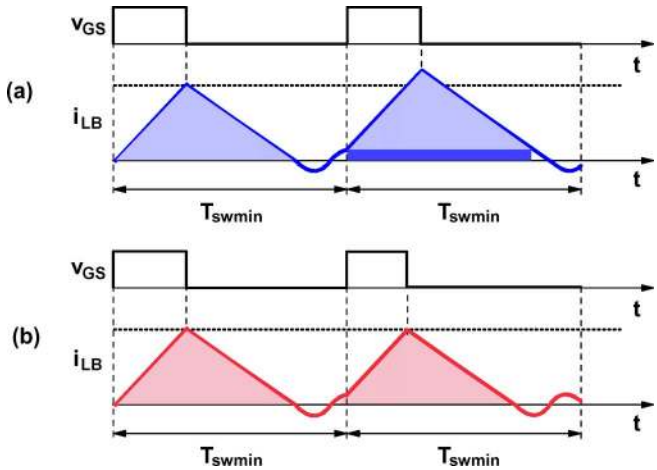

Fig. 7. Key switching waveforms of DCM/CCM boundary boost with SFL operating in (a) voltage-mode control and (b) current-mode control.

The line current expression in (15) is obtained by neglecting the oscillation of the boost inductor current after the reset of the boost inductor. If the oscillation of the boost inductor current is also taken into consideration, it can be easily shown that the line-current distortion depends on the control method used. When voltage-mode control is used, the peak inductor current depends on the initial value of the inductor current during the resonant interval at the moment switch S_B is turned on because on-time T_{ON} is constant, as shown in Fig. 7(a). Therefore, the peak inductor current, and consequently, the average value of the inductor current can change abruptly between two consecutive switching cycles, resulting in significant line-current distortions. As illustrated in Fig. 7(a), the averaged value of the

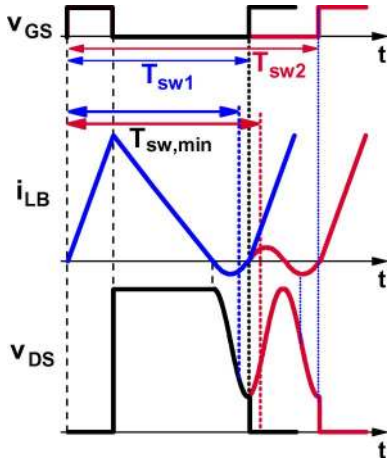

Fig. 8. Key switching waveforms of DCM/CCM boundary boost with SFL and VS.

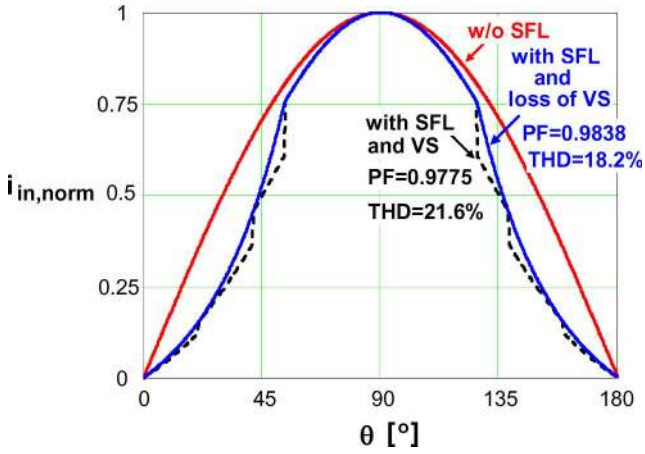

Fig. 9. Normalized line current waveforms for the case without SFL, and for the case with SFL where VS is lost and where it is maintained after the onset of SFL.

inductor current is increased due to the additional rectangular area. When current-mode control is used, the peak inductor current is constant, and instead, on-time $T_{\rm ON}$ changes, but only slightly, resulting in approximately the same averaged value of the inductor current in two consecutive switching cycles, as shown in Fig. 7(b). Consequently, the line current is only slightly distorted. By reducing the amplitude of the resonant current, e.g., by selecting a switch with lower output capacitance, the line-current distortion can be further reduced. Although damping of the resonance is possible using an *RCD* snubber as suggested in [17], the additional power loss due to the snubber is undesirable.

If an SFL is implemented and the boost switch operates with VS until the onset of the SFL, the line current is determined as

$$i_{\rm in}=\begin{cases}\dfrac{v_{\rm in}T_{\rm ON}}{2L_B}\dfrac{1}{1+(T_d/T_{\rm ON})\,(1-(v_{\rm in}/V_o))}, & \text{if } \dfrac{v_{\rm in}}{V_o}>1-A_1\\ \dfrac{v_{\rm in}T_{\rm ON}}{2L_B}\dfrac{T_{\rm ON}f_{\rm sw,max}}{1-(v_{\rm in}/V_o)}, & \text{if } \dfrac{v_{\rm in}}{V_o}\le 1-A_1\end{cases} \tag{16}$$

where

$$A_1=\frac{T_{\rm ON}f_{\rm sw,max}}{1-T_df_{\rm sw,max}}. \tag{17}$$

If an SFL is implemented and VS is always maintained, additional distortions in the line current are introduced, as follows from Fig. 8. In fact, if the first valley in the present switching period occurs just after interval $T_{\rm sw,min}=1/f_{\rm sw,max}$, switch S_B turns on at the first valley; however, if the first valley in the present switching period occurs just before interval $T_{\rm sw,min}$, the turn-on of switch S_B is delayed until the second valley (also called valley skipping), resulting in an abrupt change in the averaged inductor current, and therefore, in an abrupt change in the line current. The line current waveform is determined as

$$i_{\rm in}=\begin{cases}\dfrac{v_{\rm in}T_{\rm ON}}{2L_B}\dfrac{1}{1+(T_d/T_{\rm ON})\,(1-(v_{\rm in}/V_o))}, & \text{if } \dfrac{v_{\rm in}}{V_o}\ge 1-A_1\\ \dfrac{v_{\rm in}T_{\rm ON}}{2L_B}\dfrac{1}{1+k(T_d/T_{\rm ON})\,(1-(v_{\rm in}/V_o))}, & \text{if } A_1<1-\dfrac{v_{\rm in}}{V_o}\le A_k\end{cases} \tag{18}$$

where

$$A_k=\frac{T_{\rm ON}f_{\rm sw,max}}{1-kT_df_{\rm sw,max}},\qquad k=2v-1 \tag{19}$$

where v is the ordinal number of a valley starting from the second valley.

The line current expressions in (16) and (18) are obtained by neglecting the oscillation of the boost inductor current after the reset of the boost inductor.

Normalized line current waveforms for a 130-W, universal-input, 385-V-output DCM/CCM boundary boost PFC converter with $L_B=230$ μH and 250-kHz SFL are shown in Fig. 9 at 230-$V_{\rm rms}$ line voltage. The solid-line and dash-line waveforms are for the cases where the VS is lost and where it is maintained after the onset of the SFL, respectively. Key normalized parameters of the line current waveforms in Fig. 9 are $T_{\rm ON,norm}=T_{\rm ON}f_{\rm sw,max}=0.2825$ and $T_{d,\rm norm}=T_d/T_{\rm ON}=0.422$. The PF for the line current with VS always maintained is only slightly lower than PF for the line current with VS lost after the onset of the SFL, while the corresponding THD is only slightly higher, i.e., by 3.4%, as shown in Fig. 9.

The line current expression in (18) is obtained under the assumption that the valley skipping is monotonic. However, in a real circuit, in addition to the valley skipping, a jittering effect can be observed during a few switching cycles when the switching period is approximately equal to $T_{\rm sw,min}$, where the turn-on of switch S_B randomly happens between two consecutive valleys. Besides the line-current distortion, the valley jittering may also result in audible noise. This valley jittering, and consequently, the audible noise, can be reduced by using a sophisticated valley locking [9] (also called antijittering [18]) algorithm with a hysteresis characteristic.

III. Simulation Results

To more accurately illustrate the effect of SFL and valley skipping on the line current waveform during the entire line cycle, without neglecting the effect of the input filter and the oscillation of the boost inductor current after the reset of the boost

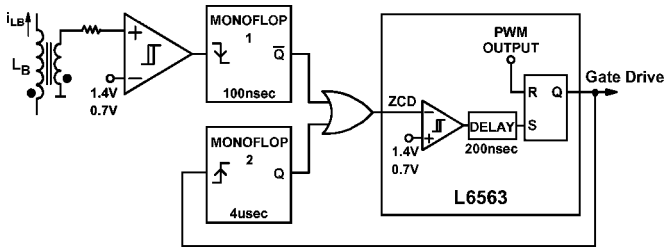

Fig. 10. Simulation subcircuit illustrating frequency limit and VS using the L6563 controller.

inductor, SIMPLIS simulations were performed. The simulation circuit was a 130-W, universal-input, 385-V-output, DCM/CCM boundary boost PFC converter with $L_B = 230\ \mu$H and with 250-kHz SFL, operating with current-mode control and VS. The control circuit is based on the L6563 controller from ST Microelectronics. Since the L6563 controller does not have an internal SFL, the control circuit is simulated, as shown in Fig. 10. The zero-current detect (ZCD) input of L6563 is connected through an OR gate to monoflops 1 and 2, where monoflop 1 receives a signal from a comparator monitoring the voltage of the auxiliary winding of boost inductor L_B, and produces a 100-ns pulse when VS is maintained and a 4.1-μs pulse when VS is not maintained. Monoflop 2 produces a 4-μs pulse when the gate drive signal goes high, which prevents the turn-on of main switch S_B until a 4-μs minimum switching period has passed. VS is obtained by sensing the change in polarity of the voltage across inductor L_B and by implementing a short delay (i.e., 200 ns) internal to L6563. Since this delay is fixed, VS can be adjusted by adding a capacitor across main switch S_B in order to change the resonant interval to match the internal delay. VS can be controlled in a more sophisticated way by sensing when the slope of the ringing voltage across the auxiliary winding approaches zero [9]. It should be noted that the 100-ns pulsewidth of monoflop 1 is shorter than a typical resonant interval, whereas the 4.1-μs pulsewidth guarantees proper operation even if the resonance becomes damped, and therefore, undetectable.

Fig. 11 shows simulation waveforms at 230-$V_{\rm rms}$ line voltage and at full load. The switching frequency variation during the entire line cycle is also included in Fig. 11. It is shown in Fig. 11 that switching frequency $f_{\rm sw}$ is not firmly clamped to its limit due to valley skipping, i.e., due to the fact that the circuit must wait for the next resonant valley before turning on. It can be seen in Fig. 11 that a discontinuity occurs in the line current waveform whenever switching frequency $f_{\rm sw}$ reaches its 250-kHz limit. For comparison with the case without SFL, the corresponding line current waveform and switching frequency variation are also presented in Fig. 11. It should be noted that in the case where the switching frequency is not limited by the control circuit, it is nevertheless limited by the effect of the filter capacitor at the output of the full-bridge rectifier, which prevents the rectified line voltage to decrease to zero.

It follows from Fig. 11 that the line current waveform with SFL is more distorted than without SFL. Calculated PF and THD values are also included in Fig. 11. It should be noted

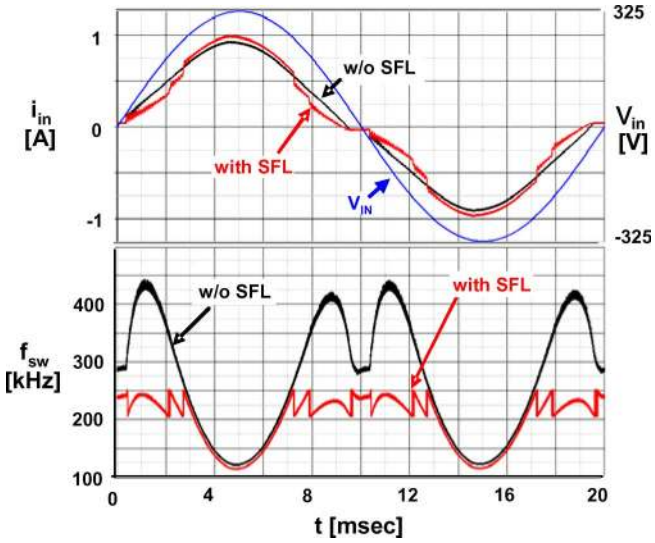

Fig. 11. Simulation waveforms of DCM/CCM boundary boost PFC with and without SFL at 230-$V_{\rm rms}$ line voltage, at full-load; without SFL: PF = 0.994, THD = 6.6%, $f_{\rm sw,avg} = 245$ kHz; with SFL: PF = 0.974, THD = 21.6%, $f_{\rm sw,avg} = 197$ kHz.

that the displacement angle between the line voltage and the fundamental component of the line current is $\theta = 5^\circ$.

The benefit of limiting the switching frequency is reduced switching loss, both the capacitive turn-on loss $P_{C_{\rm oss}}$ and gate drive loss P_G of switch S_B, as well as the core and copper losses of the inductor. Using simulation, drain–source voltage v_{DS}, a moment prior to switch S_B turn-on (i.e., $V_{C_{\rm oss}}$), can be sampled along with switching frequency $f_{\rm sw}$ and used to determine both turn-on loss $P_{C_{\rm oss}}$ and gate drive loss P_G during a line period T_L, respectively, defined as

$$P_{C_{\rm oss}} = \frac{1}{T_L}\int_0^{T_L} \frac{1}{2} f_{\rm sw}(t)\, C_{\rm oss} V_{C_{\rm oss}}^2(t)\, dt \qquad (20)$$

and

$$P_G = V_{GG} Q_G \frac{1}{T_L}\int_0^{T_L} f_{\rm sw}(t)\, dt \qquad (21)$$

where V_{GG} is the gate drive voltage and Q_G is the total gate charge. Simulation waveforms during a half-line cycle and calculation results are presented in Fig. 12 for three cases: without SFL with VS, and SFL $f_{\rm sw,max} = 250$ kHz with and without VS. The simulation was performed at 230-$V_{\rm rms}$ line voltage and full load, i.e., 130 W ($V_{GG} = 15$ V, $C_{\rm oss} = 100$ pF, and $Q_G = 60$ nC). Although gate drive loss P_G is similar in all cases, capacitive turn-on loss $P_{C_{\rm oss}}$ is nearly three times higher when VS is lost. However, performing a similar simulation at 20% load (see Fig. 13) shows that gate drive loss P_G nearly triples when the frequency is not limited, and capacitive turn-on loss $P_{C_{\rm oss}}$ nearly triples when VS is lost while operating with SFL. In addition to an increased loss, the effect of losing VS is also an increase in conducted EMI [9], which may necessitate additional filtration, which further increases the total loss.

The necessity of VS and switching-frequency limitation at light loads can be further illustrated with loss calculations with respect to the overall loss budget. For example, the Climate

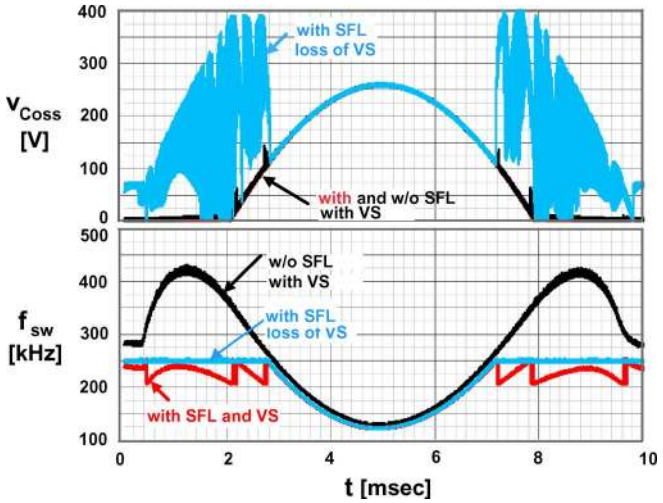

Fig. 12. Simulation of drain–source voltage just prior to switch S_B turn-on (i.e., $V_{C_{\rm oss}}$) and switching frequency $f_{\rm sw}$ with and without SFL and VS at 230-$V_{\rm rms}$ line voltage, at full-load; without SFL and VS: $f_{{\rm sw},{\rm avg}} = 245$ kHz, $P_{C_{\rm oss}} = 0.16$ W, $P_G = 0.24$ W; with SFL and VS: $f_{{\rm sw},{\rm avg}} = 197$ kHz, $P_{C_{\rm oss}} = 0.15$ W, $P_G = 0.18$ W; with SFL and loss of VS: $f_{{\rm sw},{\rm avg}} = 209$ kHz, $P_{C_{\rm oss}} = 0.41$ W, $P_G = 0.19$ W.

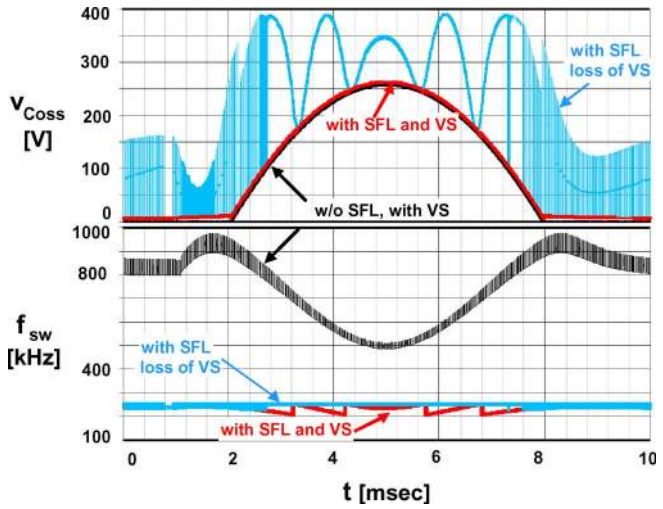

Fig. 13. Simulation of drain–source voltage just prior to switch S_B turn-on (i.e., $V_{C_{\rm oss}}$) and switching frequency $f_{\rm sw}$ with and without SFL and VS at 230-$V_{\rm rms}$ line voltage, at 20% load; without SFL and VS: $f_{{\rm sw},{\rm avg}} = 728$ kHz, $P_{C_{\rm oss}} = 0.57$ W, $P_G = 0.66$ W; with SFL and VS: $f_{{\rm sw},{\rm avg}} = 230$ kHz, $P_{C_{\rm oss}} = 0.24$ W, $P_G = 0.21$ W; with SFL and loss of VS: $f_{{\rm sw},{\rm avg}} = 243$ kHz, $P_{C_{\rm oss}} = 0.74$ W, $P_G = 0.22$ W.

Savers Computing Initiative program specifies 87% minimum efficiency at both full load and 20% load for laptop adapters and PC power supplies [16]. Since the DCM/CCM boundary boost PFC represents the front-end, and assuming that the dc–dc stage has around 92% efficiency, the efficiency of the PFC stage must be greater than 95%. For a 130-W power supply, this represents a loss budget of 6.84 W at full load and 1.37 W at 20% load. At full load, the combined capacitive turn-on loss and gate drive loss is equal to 5% of the budget when operated with VS and SFL, whereas it increases to 6% of the budget when operated with VS and without SFL, and increases further to 8.8% when operated with SFL and loss of VS, i.e., the difference when switching frequency is not limited or VS is lost is not significant. However at 20% load, the combined capacitive turn-on loss and gate drive loss is equal to 33% of the budget when operated with SFL and VS, whereas it increases to 90% of the budget when operated with VS and without SFL and to 70% of the budget when operated with SFL and loss of VS. It can be concluded that without SFL and VS, the power supply would very likely fail to meet the efficiency specifications at light load.

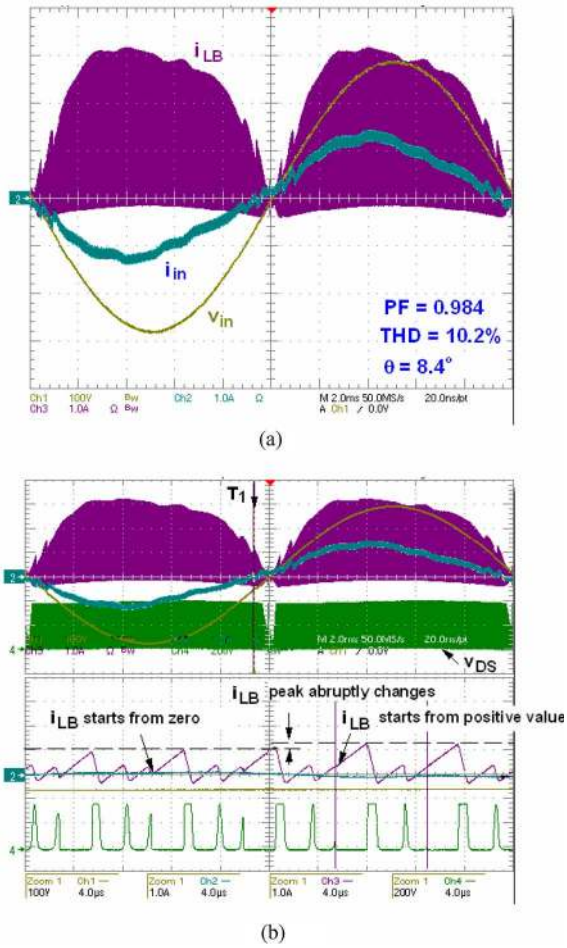

Fig. 14. Key experimental waveforms of 150-W/385-V, universal-input DCM/CCM boundary boost PFC with voltage-mode control, 133-kHz SFL, and loss of VS after the onset of SFL. (a) During a line cycle. (b) Zoomed in around instant T_1.

IV. Experimental Results

The experimental waveforms in Fig. 14 illustrate the line-current distortions when VS is not maintained and a maximum SFL is implemented with voltage-mode control. The experimental waveforms in Fig. 14 were obtained on a 150-W, universal-input, 385-V-output DCM/CCM boundary boost PFC prototype circuit controlled by the NCP1601 voltage-mode controller IC from ON Semiconductor. The line voltage was 200 $V_{\rm rms}$, where the line-current distortions are visually more profound than at

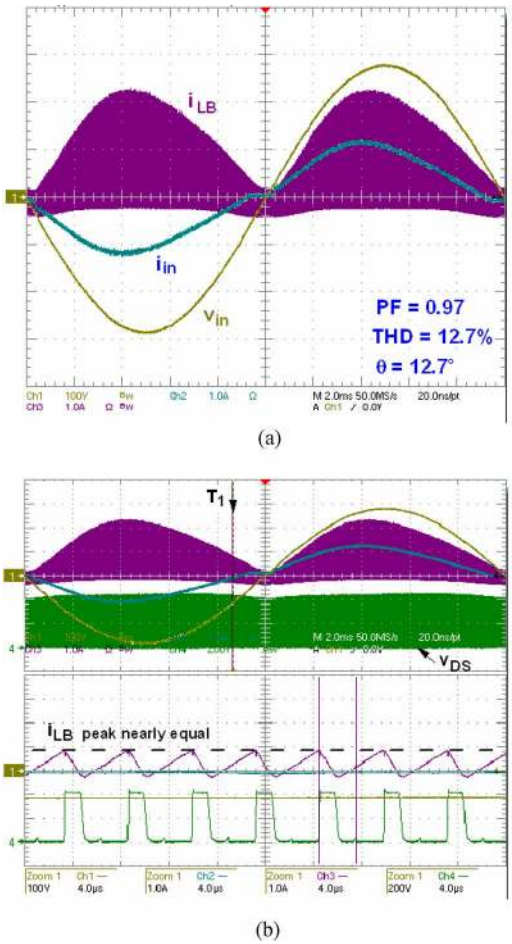

Fig. 15. Key experimental waveforms of 130-W/385-V, universal-input DCM/CCM boundary boost PFC with current-mode control, 180-kHz SFL, and loss of VS after the onset of SFL. (a) During a line cycle. (b) Zoomed in around instant T_1.

230 $V_{\rm rms}$, the SFL was 133 kHz, and VS was lost after the onset of the SFL. As shown in Fig. 14(a), the boost inductor current i_{LB} waveform, and consequently, the line current waveform, contains abrupt changes around the zero crossings of the line voltage. These nonmonotonic distortions are due to the abrupt increase in the peak of the inductor current, as illustrated in Fig. 14(b), which is a result of the inductor current increasing from zero at the start of one switching cycle, and then, increasing from a positive value at the start of the next switching cycle.

Fig. 15 shows that the line current changes monotonically when VS is not maintained, and a maximum SFL is implemented with current-mode control. The experimental waveforms in Fig. 15 were obtained on a 130-W, universal-input, 385-V-output DCM/CCM boundary boost PFC prototype circuit controlled by the MC33368 current-mode controller from ON Semiconductor. The line voltage was 200 $V_{\rm rms}$, the SFL was 180 kHz, and VS was lost after the onset of the SFL. As shown in Fig. 15(a), the boost inductor current and the line current waveforms do not have nonmonotonic distortions. In fact, the peak of the inductor current does not have any abrupt changes, as illustrated in Fig. 15(b). It should be noted that the MC33368 controller ensures a minimum off-time, which indirectly limits the switching frequency, whereas the NCP1601 controller directly limits the switching frequency.

Measured PF, THD, and displacement angle θ are also included in Figs. 14 and 15. Although the line current waveform in Fig. 14 appears more distorted than in Fig. 15, PF and THD are slightly better in Fig. 14 than in Fig. 15. This is due to the larger input filter capacitance at the output of the full-bridge rectifier in the experimental circuit with current-mode control, which results in a wider zero conduction angle around the zero crossings of the line voltage, as shown in Fig. 15, and therefore, in an increased THD. In addition, the NCP1601 controller IC used in the experimental circuit with voltage-mode control considerably reduces the crossover distortion of the line current because it artificially increases the on-time around the zero crossings of the line voltage. It should be noted that the zero conduction angle is due to the input filter capacitance at the output of the full-bridge rectifier failing to completely discharge around the zero crossings of the line voltage, resulting in reverse bias of the bridge diodes.

It can be concluded that, although the nonmonotonic distortions make the line current waveform with voltage-mode control appear more distorted, the overall effect on PF and THD is not severe.

V. Summary

A systematic analysis of line-current distortions of the DCM/CCM boundary boost PFC converter due to VS and switching-frequency limitation, where VS is either maintained or lost after the onset of switching-frequency limitation, is provided. Closed-form expressions for the line current are derived. It is shown that line-current distortions due to VS are negligible only close to full-load, whereas line-current distortions due to switching-frequency limitation can be considerable in the high-line-voltage range similar to the boost PFC converters operating in DCM. It is also shown that if the switching frequency is limited and VS is not maintained, the line current appears more distorted with voltage-mode control than with current-mode control due to the abrupt changes around the zero crossings of the line voltage. However, these nonmonotonic distortions in the line current waveform with voltage-mode control have no severe effect on PF and THD. The effects of line-current distortions are demonstrated with both simulation and experimental results.

References

[1] J. S. Lai and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Mar. 1993, pp. 267–273.

[2] J. Sebastian, J. A. Cobos, J. M. Lopera, and J. Uceda, "The determination of the boundaries between continuous and discontinuous modes in PWM dc-to-dc converters used as power factor preregulators," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 574–582, Sep. 1995.

[3] J. Zhang, J. Shao, F. C. Lee, and M. M. Jovanović, "Evaluation of input current in the critical mode boost PFC converter for distributed power systems," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 2001, pp. 130–136.

[4] M. Shen, Z. Qian, and M. Chen, "Analysis and average modeling of critical mode boost PFC converter," in *Proc. IEEE Power Electron. Drive Syst. Conf. (PEDS)*, Oct. 2001, pp. 138–141.
[5] M. Gotfryd, "Limits in boost power factor corrector operating in borderline mode," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1330–1335, Nov. 2003.
[6] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *Proc. IEEE Power Electron. Drive Syst. Conf. (PEDS)*, Nov. 2005, pp. 1542–1546.
[7] A. Abramovitz, "Effect of the ripple current on power factor of CRM boost APFC," in *Proc. CES/IEEE Int. Power Electron. Motion Control Conf. (IPEMC)*, Aug. 2006, pp. 1412–1415.
[8] Y.-K. Lo, J.-Y. Lin, and S.-Y. Ou, "Switching-frequency control for regulated discontinuous-conduction-mode boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 760–768, Apr. 2007.
[9] W. Langeslag, R. Pagano, K. Schetters, A. Strijker, and A. Zoest, "VLSI design and application of a high-voltage-compatible SoC-ASIC in bipolar CMOS/DMOS technology for AC-DC rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2626–2641, Oct. 2007.
[10] L. Huber and M. M. Jovanović, "Single-stage single-switch input current shaping technique with reduced switching loss," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 681–687, Jul. 2000.
[11] Y. Panov and M. M. Jovanović, "Adaptive off-time control for variable-frequency, soft-switched flyback converter at light loads," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 596–603, Jul. 2002.
[12] M. M. Jovanović and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
[13] K. H. Liu and Y. L. Lin, "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 1989, pp. 825–829.
[14] D. S. L. Simonetti, J. L. F. Vieira, and G. C. D. Sousa, "Modeling of the high-power factor discontinuous boost rectifier," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 788–795, Aug. 1999.
[15] Environmental Protection Agency (EPA), "Energy Star Program Requirements for Single Voltage External AC-DC and AC-AC Power Supplies, Eligibility Criteria (version 2.0)," [Online]. Available: http://www.energystar.gov/ia/partners/prod_development/revisions/downloads/eps_spec_v2.pdf
[16] "Climate Savers Computing Initiative," White paper. (2008). [Online]. Available: http://www.climatesaverscomputing.org/media/White_Paper_11.25.08.pdf
[17] K. De Gusseme, D. M. Van de Sype, A. P. M. Van Den Bossche, and J. A. Melkebeek, "Input-current distortion of CCM boost PFC converters operated in DCM," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 858–865, Apr. 2007.
[18] P. Preller, "A controller family for switch mode power supplies supporting low power standby and power factor correction," Infineon Technol. AG, Munich, Germany, Appl. Note AN-TDA 1684X, Jun. 2000.

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