Effective Dynamic Voltage Scaling through CPU-Boundedness Detection [*]

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Abstract. Dynamic voltage scaling (DVS) allows a program to execute at a non-peak CPU frequency in order to reduce CPU power, and hence, energy consumption; however, it is oftentimes done at the expense of performance degradation. For a program whose execution time is bounded by peripherals' performance rather than the CPU speed, applying DVS to the program will result in negligible performance penalty. Unfortunately, existing DVS-based power-management algorithms are *conservative* in the sense that they overly exaggerate the impact that the CPU speed has on the execution time. We propose a new DVS algorithm that detects the CPU-boundedness of a program on the fly (via a regression method on the past MIPS rate) and then adjusts the CPU frequency accordingly. To illustrate its effectiveness, we compare our algorithm with other DVS algorithms on real systems via physical measurements.

1 Introduction

Dynamic voltage and frequency scaling (DVS) is a mechanism whereby software can dynamically adjust CPU voltage and frequency. This mechanism allows systems to address the problem of ever-increasing CPU power dissipation and energy consumption, as they are both quadratically proportional to the CPU voltage. However, reducing the CPU voltage may also require the CPU frequency to be reduced and results in degraded CPU performance with respect to execution time. In other words, DVS trades off performance for power and energy reduction.

The performance loss due to running at a lower CPU frequency raises several issues. First, a user who pays to upgrade his/her computer system does not want to experience performance degradation. Second, running programs at a low CPU frequency may end up increasing total system energy usage [1–3]. In order to control (or constrain) the performance loss effectively, a model that relates performance to the CPU frequency is essential for any DVS-based power-management algorithm (shortened as DVS algorithm hereafter).

A typical model used by many DVS algorithms predicts that the execution time will double if the CPU speed is cut in half. Unfortunately, this model

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overly exaggerates the impact that the CPU speed has on the execution time. It is only in the worst case that the execution time doubles when the CPU speed is halved; in general, the actual execution time is less than double. For example, in programs with a high cache miss ratio, performance can be limited by memory bandwidth rather than CPU speed. Since memory performance is not affected by a change in CPU speed, increasing or decreasing the CPU frequency will have little effect on the performance of these programs. We call this phenomenon — *sublinear performance slowdown*. Consequently, researchers have been trying to exploit this program behavior in order to achieve better power and energy reduction [4–7].

One common technique to exploit the sublinear performance slowdown decomposes program workload into regions based on their CPU-boundedness. The decomposition can be done statically using profiling information [4] or dynamically through an auxiliary circuit [5] or through a built-in performance monitoring unit (PMU) [6, 7]. In this paper, we propose a new PMU-assisted, on-line DVS algorithm called *β-adaptation* that provides fine-grained, tight control over performance loss and takes advantage of sublinear performance slowdown. This new *β-adaptation* algorithm is based on an extension of the theoretical work developed by Yao et al. [8] and by Ishihara and Yasuura [9]. Via physical measurements, we will demonstrate the effectiveness of the *β-adaptation* algorithm when compared to several existing DVS algorithms for a number of applications.

The rest of the paper is organized as follows. Section 2 characterizes how current DVS algorithms relate performance to CPU frequency. With this characterization as a backdrop, we present a new DVS algorithm (Section 3) along with its theoretical foundation (Section 4). Then, Section 5 describes the experimental set-up, the implemented DVS algorithms, and the experimental results. Finally, Section 6 concludes and presents some future directions.

2 Related Work

There have been some attempts to exploit the sublinear performance slowdown (where increasing or decreasing the CPU frequency will have little effect on the performance of a program) to achieve more power and energy reduction. For example, Li et al. [5] propose to set the CPU to a low speed whenever an L2 cache miss occurs, whereas Hsu and Kremer [4] use off-line profiling to identify memory-bound program regions. The former approach requires an auxiliary circuit, and the latter approach needs source code and compiler support. These requirements make their approaches more difficult to implement in practice.

Another approach is to use built-in performance monitoring unit (PMU) to assist in the on-line detection of sublinear performance slowdown. Our work and Choi et al.'s recent work [6, 7] belong to this category. Both use a regression method and PMU support to perform the on-line construction of a simple performance-prediction model so as to capture the degree of CPU-boundedness. In general, the design of PMU-assisted on-line DVS algorithms is not an easy task. First, the PMU is notorious for its incomplete set of event counting and

inconsistency across generations of the CPU. Second, the correlation of event counts to power and performance is not yet clear. Hence, for now, a PMU-assisted, on-line, DVS algorithm ought to minimize its dependency on event counts and rely as much as possible on those event counts that are consistent across CPU generations.

Our work differs from Choi et al.'s work in the definition of CPU-boundedness, and thus, the detection mechanism. Choi et al.'s work is based on the ratio of the on-chip computation time to the off-chip access time. In contrast, our algorithm defines CPU-boundedness as the fraction of program workload that is CPU-bound. Because of the different definitions, the set of events monitored by the PMU for each algorithm is different. In Section 5.5, we argue that our DVS algorithm is equally effective but has a simpler implementation. Moreover, we provide a theoretical foundation of why our DVS algorithm is effective in achieving energy optimality. We believe that the same theoretical result can be applied to their work as well.

3 β-Adaptation: A New DVS Algorithm

Here we describe a new, interval-based, PMU-assisted, DVS algorithm that provides fine-grained, tight control over performance loss as well as exploits the sublinear performance scaling in memory-bound and I/O-bound programs. The theoretically-based heuristic algorithm is based on an extension of the theoretical work developed by [8] and [9] (details in Section 4):

> If the CPU power draw is a convex function of the CPU frequency, then for any program whose performance is an *affine* function of the CPU frequency, running at a constant CPU speed and meeting the deadline just in time will minimize the energy usage of executing the program. If the desired CPU frequency is not directly supported, the two immediately-neighboring CPU frequencies can be used to emulate the desired CPU frequency and result in an energy-optimal DVS schedule.

To account for the sublinear performance slowdown, the following model that relates performance to the CPU frequency is often used [6, 7, 10]:

$$T(f) = W_{cpu} \cdot \frac{1}{f} + T_{mem} \tag{1}$$

The total execution time $T(f)$ at frequency f is decomposed into two parts. The first part models on-chip workload in terms of CPU cycles. Its value is affected by the CPU speed change. The second part models the time due to off-chip accesses and is invariant to changes in the CPU speed. Note that this breakdown of the total execution time is inexact when the target processor supports out-of-order execution because on-chip execution may overlap with off-chip accesses [11]. However, in practice, the error tends to be quite small [6, 7].

The model $T(f)$ treats program performance as an affine function of the CPU frequency f and thus allows us to apply the aforementioned theoretical result.

We simply execute a program at CPU frequency f^* such that $D = T(f^*)$ where D is the deadline of the program. However, there are two challenges in using the theorem this way. First, in many cases there is no consensus on how to assign a deadline to a program, e.g., scientific computation. Second, to use $T(f)$, we need to know the values of the coefficients, W_{cpu} and T_{mem}. These coefficients are oftentimes determined by the hardware platform, program source code, and data input. Thus, calculating these coefficients statically is very difficult.

We address these challenges by defining a deadline as the relative performance slowdown and by estimating the model's coefficients on the fly (without any off-line profiling nor compiler support). The relative performance slowdown δ

$$\delta = \frac{T(f)}{T(f_{max})} - 1 \tag{2}$$

where f_{max} is the peak CPU frequency, has been used in previous work [6, 7, 11]. It is widely accepted in programs that are difficult to assign deadlines in terms of absolute execution time. It also carries more timing requirement information than CPU utilization and IPC rate. Providing this user-tunable parameter δ in our DVS algorithm allows fine-grained, tight control over performance loss.

To estimate the coefficients more efficiently, we first re-formulate the original two-coefficient model in Equation (1) as a single-coefficient model:

$$\frac{T(f)}{T(f_{max})} = \beta \cdot \frac{f_{max}}{f} + (1 - \beta) \tag{3}$$

with

$$\beta = \frac{W_{cpu}}{W_{cpu} + T_{mem} \cdot f_{max}} \tag{4}$$

The coefficient β is, by definition, a value between 0 and 1. It was introduced by one of the authors in [4] to quantify, for a program, the performance impact to the CPU speed change. The metric represents the fraction of the program workload that scales linearly with the CPU frequency. If a program has $\beta = 1$, it means the execution time of the program will double when the CPU speed is halved. In contrast, a program with $\beta \approx 0$ will have its execution time remained the same even running at the slowest CPU speed.

The coefficient β is computed at run time using a regression method on the past MIPS rates reported from the PMU. Specifically, our DVS algorithm keeps track of the average MIPS rate for each executed CPU frequency and applies the least-square fitting at each interval to dynamically re-compute the new β value:

$$\beta = \frac{\sum_i (\frac{f_{max}}{f_i} - 1)(\frac{\texttt{mips}(f_{max})}{\texttt{mips}(f_i)} - 1)}{\sum_i (\frac{f_{max}}{f_i} - 1)^2} \tag{5}$$

where $\texttt{mips}(f)$ is the average MIPS rate for CPU frequency f. Note that our mechanism assumes a constant number of total instructions in a program, regardless of the running CPU frequency. This assumption has been verified through

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For every I seconds, do the following:

1. Use Equation (5) to compute β.      4. Compute the ratio r.
2. Compute frequency f*.
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$$f^* = \max\left(f_{min}, \frac{f_{max}}{1 + \delta/\beta}\right)$$

$$r = \frac{1/f^* - 1/f_{j+1}}{1/f_j - 1/f_{j+1}}$$

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                                       5. Run r · I seconds at f_j.
3. Figure out f_j and f_{j+1}.         6. Run (1 − r) · I seconds at f_{j+1}.
                                       7. Update mips(f_j) and mips(f_{j+1}).
```

$$f_j \leq f^* < f_{j+1}$$

Fig. 1. Algorithm β-*adaptation*. Parameter δ is the relative performance slowdown and parameter I is the length of an interval in seconds.

extensive experiments. In practice, the value of β converges very quickly for the benchmarks we tested.

The rest of the algorithm simply applies the theoretical result to compute the desired CPU frequency f^* for each interval, once the coefficient β is updated, plus some bookkeeping on $\mathtt{mips}(f)$. The derivation of f^* comes by equating Equation (2) with Equation (3). Figure 1 outlines the entire algorithm.

4 Theoretical Foundation

In the previous section, we claim a theoretical result for energy-optimal DVS scheduling which extends both Yao et al.'s work in [8] and Ishihara and Yasuura's work in [9]. In this section we provide evidence to support our claim.

The energy-optimal DVS scheduling problem considered here is taken from [4]. That previous work only provides a problem formulation. In this paper we provide a theorem that characterizes the energy-optimal DVS schedule for the problem. The theorem is also closely related to previous work such as Miyoshi et al.'s "critical power slope" [2].

A DVS system is assumed to export n settings $\{(f_i, P_i)\}$, where P_i is the CPU power dissipation (in watts) at CPU frequency f_i. Without loss of generality, we assume $0 < f_{min} = f_1 < \cdots < f_n = f_{max}$. We also denote the total execution time of a program running at setting i as T_i. Finally, to facilitate discussion, we define $E_i = P_i \cdot T_i$, where E_i is the energy consumption (in joules) when running for T_i seconds at CPU frequency f_i.

The DVS scheduling problem is formulated as follows: Given a program and a deadline D (in seconds), find a DVS schedule $(t_1^*, \cdots, t_n^*)$ such that if the program is executed for t_i^* seconds at setting i, the total energy usage E is minimized, the deadline D is met, and the required work is completed. Mathematically speaking,

$$t^* = \arg\min\{E = \sum_i P_i \cdot t_i : \ \sum_i t_i \leq D, \ \sum_i t_i/T_i = 1, \ t_i \geq 0\} \qquad (6)$$

To simplify the discussion of the theorem, we handle a few corner cases first. First, the condition $D \geq \min_i T_i$ has to be satisfied so that the problem is feasible. Second, if the condition $D \geq \max_i T_i$ is satisfied, the problem becomes the classical fractional Knapsack problem [12]. In this case, the energy-optimal DVS schedule will execute the entire program at setting i^* where $i^* = \arg_i \min\{E_i\}$. For the case of $T_1 = \cdots = T_n$, the above DVS schedule is also energy-optimal. What is left is the case $\min_i T_i < D < \max_i T_i$, which we assume to be true for the following theorem.

Theorem 1. *If*

$$T_i = \frac{c_1}{f_i} + c_0, \ c_1 \neq 0$$

and

$$\frac{P_1 - 0}{f_1 - 0} \leq \frac{P_2 - P_1}{f_2 - f_1} \leq \frac{P_3 - P_2}{f_3 - f_2} \leq \cdots \leq \frac{P_n - P_{n-1}}{f_n - f_{n-1}}$$

then

$$t_i^* = \begin{cases} \frac{1/f^* - 1/f_{j+1}}{1/f_j - 1 - f_{j+1}} \cdot T_j & i = j \\ D - t_j^* & i = j + 1 \\ 0 & \text{otherwise} \end{cases}$$

where

$$f_j \leq f^* < f_{j+1}$$

Proof. (See the Appendix).

Theorem 1 says that for any program whose execution time is an *affine* function of the CPU frequency, if the DVS settings in a CPU are *well-assigned* (explained below), then we can run the program at a CPU frequency that finishes the execution right at the deadline *and* results in an energy-optimal schedule. If the desired CPU frequency is not directly supported, it can be emulated by the two immediately-neighboring CPU frequencies.

For any DVS-enabled processor whose power draw can be modeled as a convex function of its frequency, the processor's DVS settings are always well-assigned. However, some realistic processors do not have well-assigned DVS settings by default. In these processors, the lowest frequency f_1 can be emulated by the combination of frequency 0 (i.e., the CPU in sleep mode) and the second lowest frequency f_2 with a *lower* power dissipation, i.e., $\frac{P_1 - 0}{f_1 - 0} > \frac{P_2 - P_1}{f_2 - f_1}$. As a result, completing a task *before* its deadline and putting the CPU into sleep mode is more energy-efficient than completing the task at the deadline. This is the phenomenon observed by Miyoshi et al. [2] and motivated them to devise a technique called "critical power slope". The phenomenon can be eliminated by making adjustments to DVS settings so that they become well-assigned.

Finally, Theorem 1 extends the work presented by Yao et al. [8] and by Ishihara and Yasuura [9]. First, both works assume that $c_0 = 0$. Second, Ishihara and Yasuura's work assumes a fixed relationship between f and V in a DVS setting; namely,

$$f = k \cdot (V - V_T)^\alpha / V \tag{7}$$

where k, V_T, α are positive constants. Unfortunately, today's DVS processors may not be able to support such an assumption. This is because these processors only provide a discrete set of CPU frequencies and voltages, whereas the above equation requires a continuous range of CPU frequencies to be supported for a discrete set of voltages. Theorem 1 loosens these assumptions to facilitate DVS algorithms on realistic processors.

5 Experiments

In this section, we describe our experimental environment in which we evaluate and compare algorithm *β-adaptation* with several other DVS algorithms. We also present an in-depth discussion of the experimental results.

5.1 Experimental Setup

In order to acquire high-fidelity experimental data, we set-up our experiments using physical measurements, as shown in Figure 2(a). The experimental results were collected through a Yokogawa WT210 digital power meter [13]. The power meter continuously samples the instantaneous wattage at every 20 μs. The profiling and tested computer both run the Linux 2.4.18 kernel. All the benchmarks were compiled by GNU compilers with optimization level -O2. All the benchmarks were run to completion; each run took over a minute.
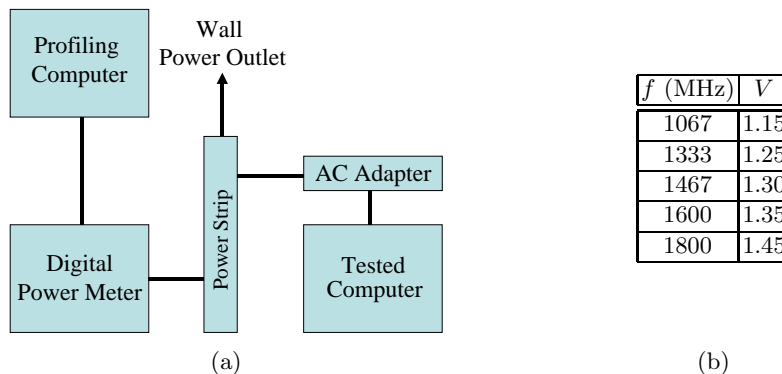
f (MHz)	V
1067	1.15
1333	1.25
1467	1.30
1600	1.35
1800	1.45

(a)   (b)

Fig. 2. The experimental setup.

The benchmarks are taken from SPEC's CPU95 benchmark suites. The SPEC benchmarks [14] emphasize the performance of the CPU and memory, but not other computer components such as I/O (disk drives), networking or graphics. We chose to use the SPEC benchmarks because they demonstrate a range of performance sensitivity to the CPU frequency change, i.e., they have a wide range of β values [4]. The experimental data are collected by running these SPEC benchmarks with the reference data input.

The hardware platform in our experiments is an HP NX9005 notebook computer. This computer includes a mobile AMD Athlon XP 2200+ processor, 256-MB DDR SDRAM, 266-MHz front-side bus, a 30-GB hard disk, and a 15-inch TFT LCD display. The mobile AMD Athlon XP processor has been used in Sun's Fire B100x blade servers [15]. It has a total of 384-KB cache space. The processor exports two registers that the software can write the target frequency and voltage values into. In our experiments, we restrict the processor to have five settings as shown in Figure 2(b). The transition time from one setting to another is 100 microseconds. During the measurements, the battery was removed, and the monitor was turned off.

Finally, when presenting the experimental results, we associate with each application its β value. Recall that the metric β represents the fraction of the program workload that is very sensitive to the CPU speed change. That is, the higher the β of a program, the more CPU-bound its performance. The β value for each benchmark was derived by profiling total execution times for all settings and then applying a least-squares fit on Equation (3).

5.2   Implemented DVS Algorithms

To evaluate the effectiveness of our DVS algorithm β-adaptation, we have implemented a number of other DVS algorithms. Though we do not claim that the implemented DVS algorithms represent a comprehensive comparison of all existing approaches, we feel that the range is wide enough to evaluate the effectiveness of our algorithm and to gain new insights from the experimental results. The following is a brief description of each algorithm we implemented.

2step: This algorithm assumes dual CPU speeds in the processor and monitors the CPU utilization percentage periodically. If the percentage is higher than a pre-defined threshold, the algorithm will set the CPU to the fast speed; if it is lower than another pre-defined threshold, the algorithm will set the CPU to the low speed. This DVS algorithm is considered to be the best algorithm in Grunwald et al.'s empirical study on several interval-based algorithms using CPU utilization [16]. In our implementation, the two thresholds are 50% and 10% and the two speeds are the maximum and the minimum CPU speeds in the processor.

nqPID: This algorithm was proposed by Varma et al. [17] as a refinement of the *2step* algorithm. Recognizing the similarity of DVS scheduling and a classical control-systems problem, the authors took the equation describing a PID

controller (Proportional-Integral-Derivative) and modified it to suit the DVS scheduling problem. This algorithm significantly improved the control over performance loss that the *2step* algorithm lacks. In addition, the authors found out that the algorithm's effectiveness does not depend on careful tuning of parameters, which is a nice feature given that *2step*'s effectiveness is critically dependent on the choice of application-specific threshold values [16].

freq: This algorithm is similar to strategies that reclaim the slack time between the actual processing time and the worst-case execution time (e.g., [18,19]). Specifically, the algorithm keeps track of the amount of remaining CPU work W_{left} and the amount of remaining time before the deadline T_{left}. The desired CPU frequency f_{new} at each interval is simply

$$f_{new} = \frac{W_{left}}{T_{left}}.$$

The algorithm assumes that the total amount of work in CPU cycles is known a priori, which, in practice, is often unpredictable [1] and not always a constant across frequencies [10].

mips: This algorithm is taken from [20] and represents a DVS strategy guided by an externally specified performance metric. Specifically, the new frequency f_{new} at each interval is computed by

$$f_{new} = f_{prev} \cdot \frac{\texttt{MIPS}_{target}}{\texttt{MIPS}_{observed}}$$

where f_{prev} is the frequency for the previous interval, $\texttt{MIPS}_{target}$ is the externally specified performance requirement, and $\texttt{MIPS}_{observed}$ is the real $\texttt{MIPS}$ rate observed in the previous interval. In our experiments, each benchmark has its own $\texttt{MIPS}_{target}$, which is derived by measuring the MIPS rate for the entire application and then dividing it by $(1 + \delta)$.

5.3 Experimental Results

Table 1 presents the experimental results for the five interval-based DVS algorithms. When a program is memory-bound or I/O-bound (β close to zero), there is substantial opportunity to reduce CPU energy consumption with negligible performance loss. In contrast, when a program is CPU-bound, there is little opportunity to reduce CPU power and energy within a tight performance-loss bound of 5%. Moreover, none of these five DVS algorithms could produce a DVS schedule that had the exact performance degradation of 5%; the actual performance loss varied from one benchmark to another.

Among the five interval-based DVS algorithms, the β-*adaptation* algorithm outperforms the others. In a sense, it verifies that our mechanism for computing CPU-boundedness on the fly is of low overhead and that the algorithm is effective in providing tight control over performance loss due to DVS as well

Table 1. The effectiveness of 5 different DVS algorithms. Each table entry is in the format of *relative-time/relative-energy* with respect to the total execution time and system energy usage when running the application at the highest setting throughout the entire execution.

program	β	*2step*	*nqPID*	*freq*	*mips*	*β-adapt.*
swim	0.02	1.00/1.00	1.04/0.70	1.00/0.96	1.00/1.00	1.04/0.61
tomcatv	0.24	1.00/1.00	1.03/0.69	1.00/0.97	1.03/0.83	1.00/0.85
su2cor	0.27	0.99/0.99	1.05/0.70	1.00/0.95	1.01/0.96	1.03/0.85
compress	0.37	1.02/1.02	1.13/0.75	1.02/0.97	1.05/0.92	1.01/0.95
mgrid	0.51	1.00/1.00	1.18/0.77	1.01/0.97	1.00/1.00	1.03/0.89
vortex	0.65	1.01/1.00	1.25/0.81	1.01/0.97	1.07/0.94	1.05/0.90
turb3d	0.79	1.00/1.00	1.29/0.83	1.03/0.97	1.01/1.00	1.05/0.94
go	1.00	1.00/1.00	1.37/0.88	1.02/0.99	0.99/0.99	1.06/0.96

as exploiting the sublinear performance slowdown for significantly more CPU power and energy savings. Algorithms *mips* and *nqPID* arguably rank second. Algorithm *mips* delivers better control over performance loss for all eight benchmarks that we tested, whereas algorithm *nqPID* performs better with respect to power and energy reduction but at the expense of more substantial performance loss. This is especially obvious for the CPU-bound benchmarks. Algorithms *freq* and *2step* clearly rank last.

So, what have we learned from this experiment? First, the number of instructions is a better metric for specifying the CPU work requirement than the number of CPU cycles. For the benchmarks we tested, we found that the number of instructions tends to remain constant across all settings. In contrast, the number of CPU cycles varies significantly depending on the executed DVS schedule. For example, the `swim` benchmark, when running at the lowest setting, has only 60% of the CPU execution cycles running at the highest setting. Typically, algorithm *freq* uses the worst-case execution cycles which in our case is the number of CPU cycles at the highest setting. This approach exaggerates the amount of the CPU work to be done and results in less effective energy reduction. This explains why algorithm *mips* performs better than algorithm *freq*.

Second, a large window size of past PMU reports is better than a small window size of past PMU reports. In the experiments we found that the MIPS rate varies significantly from interval to interval, especially for CPU-intensive applications. However, the accumulated MIPS rate converges quickly. Thus, the use of the MIPS rate in a global manner seems to be more effective than the use of the rate in a local manner. This partially explains the effectiveness of algorithm *β-adaptation* compared to algorithm *mips*. One concern, however, for using a large window size is that the DVS algorithm may be less responsive for programs that expose multiple execution phases of varying degrees of CPU-boundedness. For the SPEC benchmarks, which are known to have the aforementioned behavior, this does not seem to be a problem. More details can be found in Section 5.4.

Finally, we confirmed that CPU utilization by itself does not provide enough information about system timing requirements. As a result, the control over performance loss is unsatisfactory. This can be seen from the experimental results of algorithm *2step* and algorithm *nqPID*. Algorithm *2step* does not seem to perform any DVS scheduling. This is because the CPU for `SPEC` benchmarks is active almost all the time, i.e., its CPU utilization is always full. In this case, there exists no optimal threshold values for *2step* to make it more effective. Algorithm *nqPID* refines algorithm *2step* by removing the threshold mechanism from the end user. While it is more effective than algorithm *2step* in terms of CPU power and energy reduction, the lack of enough information about deadlines makes it impossible to provide tight control over performance loss.

5.4   The Impact of Multiple-Phase Execution Behavior

To better address the impact of multiple-phase programs to the DVS algorithm *β-adaptation*, we compare it with a profile-based, off-line DVS algorithm called *hsu* [4]. The algorithm *hsu* uses PMU-assisted off-line profiling and source code analysis to identify the most energy-profitable region in a program to slow down without causing the performance loss to surpass a pre-defined level. Off-line profiling is performed on a section-by-section basis while the DVS scheduling decisions are made in a global manner, competitively comparing the different sections. This global view of the impact of DVS on different code sections allows more effective DVS scheduling, especially for multiple-phase programs such as the `SPEC` benchmarks.

Algorithm *hsu* also uses the relative performance slowdown δ to specify control over performance loss. Thus, it allows us to compare the two algorithms on a fair basis. In the experiments we executed the profile-based algorithm *hsu* with two different training inputs, denoted as *hsu(train)* and *hsu(ref)* respectively. The two sets of training inputs are provided along with the SPEC benchmark codes. Table 2 shows the experimental results of both algorithms for the CFP95 benchmark suite.

We conclude that the effectiveness of algorithm *β-adaptation* is comparable to that of algorithm *hsu*. Both algorithms achieve a significant amount of CPU power and energy reduction with tight control over performance loss. It is interesting to note that the two algorithms seem to complement each other. Algorithm *β-adaptation* performs better in CPU-bound benchmarks from mgrid to fpppp, whereas algorithm *hsu* performs better in memory-bound benchmarks from swim to hydro2d. We are in the process of investigating the causes for this phenomenon.

As mentioned in Section 2, the effectiveness of profile-based DVS algorithms is highly determined by its training data input. In our experiments, we found that algorithm *hsu* chose different program regions to slow down in seven of the 10 benchmarks. Running the reference data input as the training input does not necessarily yield a better result, for example, apsi. We suspect that the instrumented program for profiling has somewhat altered the instruction access pattern and is considerably different from the original code. According to Hsu's

Table 2. The comparison of our new on-line DVS algorithm *β-adaptation* with an off-line DVS algorithm *hsu*. Each table entry is in the format of *relative-time/relative-energy* with respect to the total execution time and system energy usage when running the application at the highest setting throughout the entire execution.

program	β	hsu(train)	hsu(ref)	β-adapt.
swim	0.02	1.01/0.75	1.04/0.59	1.04/0.61
tomcatv	0.24	1.03/0.70	1.06/0.60	1.00/0.85
hydro2d	0.19	1.03/0.75	1.03/0.79	1.02/0.84
su2cor	0.27	1.01/0.88	1.02/0.83	1.03/0.85
applu	0.34	1.03/0.87	1.03/0.87	1.04/0.85
apsi	0.37	1.03/0.85	1.04/0.91	1.05/0.83
mgrid	0.51	1.01/1.00	1.01/1.00	1.03/0.89
wave5	0.52	1.00/1.00	1.00/1.00	1.04/0.87
turb3d	0.79	1.04/0.95	1.04/0.95	1.05/0.94
fpppp	1.00	1.00/1.00	1.00/1.00	1.06/0.95

dissertation [21], the `SUIF2` compiler infrastructure, on which algorithm *hsu* was built, also has a major impact on the experimental results.

5.5   A Comparison with Choi et al.'s Work

In this section, we compare and contrast our work with Choi et al.'s work in [6, 7]. Recall that both works are based on the same Equation (1). The difference is in the calculation of equation coefficients. Our work calculates β defined in Equation (4), whereas Choi et al.'s work calculates α_f defined as follows:

$$\alpha_f = f \cdot \frac{T_{mem}}{W_{cpu}} \tag{8}$$

Analytically, the two metrics are equivalent:

$$\beta = \frac{1}{1 + \alpha_f \cdot f_{max}/f} \tag{9}$$

However, there are several major differences in terms of implementation. First, the β metric is invariant to a CPU frequency change, whereas the α_f metric is defined with respect to a particular CPU frequency f. Thus, the number of coefficients calculated in Choi et al.'s DVS algorithm is more than the number of coefficients calculated in algorithm *β-adaptation*. Second, the formula in calculating α_f is more complex. This is due to the two-coefficient model they use, in contrast to the one-coefficient model we use. Finally, the number of PMU event counts needed for calculating β is smaller than that for calculating α_f. Since a CPU can simultaneously count a finite number of events, counting too many events may introduce a larger time overhead.

Finally, our new DVS algorithm has a simpler implementation than Choi et al.'s work. However, we cannot do an empirical comparison given the current

setting we have. Choi et al. implemented their DVS algorithms on Intel Xscale-based processors which does not provide counting for the number of *retired* instructions. On the other hand, our hardware platform, Athlon XP processor, does not provide counting for the number of *executed* instructions. In fact, this is one of the big issues in using the PMU to assist DVS scheduling — the CPU events may not be compatible nor consistent across different hardware platforms. This is also why Choi et al. presented two platform-dependent implementations [6, 7] of the same DVS algorithm [6].

5.6 Sensitivity Analysis of Algorithm Parameters

In this section, we present a sensitivity analysis of the parameters in algorithm β-*adaptation*, i.e., δ for the relative performance slowdown and I for the length of an interval, as shown in Figure 1.

For the `SPEC` CPU95 benchmarks, the average execution time increases at a pace of 3% for every 5% increase in δ, whereas the average energy consumption stays around 20% after δ passes 30%. As δ increases, the algorithm slows down CPU-bound programs which have lower performance-power ratios. Hence, setting δ at a small value such as 5% is recommended.

In terms of the interval size I, the average execution time is a U-shape curve. Since setting I to a large value, such as five seconds, did not let the program run at the converged f^* for a sufficiently long time and setting I to a small value such as 10 milliseconds introduced a significant amount of time overhead, we recommend setting I at a value between 50 milliseconds to 1 second.

6 Conclusions and Future Work

In this paper, we proposed a new, PMU-assisted, interval-based, DVS algorithm that detects the CPU-boundedness of a program on the fly and adjusts the CPU speed accordingly. The algorithm is no arbitrary heuristic. It is based on an extension of the previous theoretical work for energy-optimal DVS scheduling problem. The algorithm has also proven to be effective in comparison with a number of DVS algorithms through physical measurements. That is, the new algorithm provides fine-grained, tight control over performance loss as well as exploits the sublinear performance slowdown. Finally, the algorithm is simple to implement.

Our new DVS algorithm can be refined in various ways. One particular direction is to use compiler hints as additional scheduling support. While this idea is not new (e.g., [19, 22]), the type of hint that the compiler should provide so that the overall DVS algorithm is effective is still a research topic for general-purpose systems. To relieve the compiler from the difficulty of giving exact timing information off-line, we could have the compiler simply identify and distinguish execution phases of a program in terms of CPU-boundedness in an approximate manner. Algorithm β-*adaptation* can then be refined to compute the β value for each of these phases to further improve its effectiveness for memory-bound programs.

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Appendix

To prove Theorem 1, we first show that the following chain of inequalities is true.

$$0 \geq \frac{E_2 - E_1}{T_2 - T_1} \geq \frac{E_3 - E_2}{T_3 - T_2} \geq \cdots \geq \frac{E_n - E_{n-1}}{T_n - T_{n-1}}$$

This is not difficult to prove because

$$\frac{E_i - E_{i-1}}{T_i - T_{i-1}} - \frac{E_{i+1} - E_i}{T_{i+1} - T_i} = f_i \cdot \left(\frac{P_{i+1} - P_i}{f_{i+1} - f_i} - \frac{P_i - P_{i-1}}{f_i - f_{i-1}} \right)$$

$$+ f_i \cdot \frac{c_0}{c_1} \cdot \left(\frac{P_{i+1} - P_i}{f_{i+1} - f_i} \cdot f_{i+1} - \frac{P_i - P_{i-1}}{f_i - f_{i-1}} \cdot f_{i-1} \right) \geq 0$$

and

$$\frac{E_{i+1} - E_i}{T_{i+1} - T_i} = \frac{f_i f_{i+1}}{f_i - f_{i+1}} \cdot \left[\left(\frac{P_{i+1}}{f_{i+1}} - \frac{P_i}{f_i} \right) + \frac{c_0}{c_1} (P_{i+1} - P_i) \right] \leq 0.$$

Then we define $r_i = t_i/T_i$ and introduce a new function $E_{min}(d)$ as follows.

$$E_{min}(d) = \min\{\sum_i r_i \cdot E_i : \ \sum_i r_i \cdot T_i = d, \ \sum_i r_i = 1, \ r_i \geq 0\}$$

Since the sequence $\{\frac{E_{i+1} - E_i}{T_{i+1} - T_i}\}_{i=1,\cdots,n-1}$ is non-increasing, function $E_{min}(d)$ is equivalent to the piecewise-linear function that connects points $\{(T_i, E_i)\}$. Since the slopes of chords in this piecewise-linear function are all non-positive, $E_{min}(d)$ is non-increasing. Thus, we seek for a solution of $E_{min}(D)$ as $E_{min}(D) \equiv \min\{E_{min}(d) : \ d \leq D\}$. For $T_{j+1} < D \leq T_j$, $E_{min}(D)$ is the function value at D in the chord connecting points (T_j, E_j) and (T_{j+1}, E_{j+1}). The proof is completed by solving the linear system of $t_j^* + t_{j+1}^* = D$ and $t_j^*/T_j + t_{j+1}^*/T_{j+1} = 1$. $\quad\square$