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Effective reduction of fixed charge densities in germanium based metal-oxide-semiconductor devices

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Metal-oxide-semiconductor capacitor was fabricated using *in situ* O_2 plasma passivation and subsequent deposition of a HfO_2 high-k gate stack on Ge. By extracting flat band voltages from capacitors with different equivalent oxide thicknesses (EOT), the effect of forming gas annealing (FGA) and O_2 ambient annealing on the fixed charge was systematically investigated. The O_2 ambient annealing is more effective than FGA as it reduced fixed charge density to 8.3×10^{11} cm^{-2} compared to 4.5×10^{12} cm^{-2} for at the same thermal budget and showed no degradation of EOT. Further, the distribution of fixed charges in gate stack was discussed in detail. *© 2011 American Institute of Physics*. [doi:10.1063/1.3622649]

High mobility Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs) are considered to be a promising substitute for current state of the art Si-based MOSFETs.[1] The main problem for the application of Ge is the effective surface passivation before the deposition of the gate dielectric.[2] Many attempts have been proposed to solve this problem such as introducing sulfurization,[3] NH_3 plasma,[4] thermal oxidation,[5–7] $H_2/N_2/Ar$ plasma,[8] atomic O,[9] ozone,[10] and so on for the Ge surface passivation. Among all these techniques, the introduction of an interlayer (IL) formed by GeO_2 gave the lowest density of interface states (D_{it}) and highest comprehensive performance.[11–13] But at the same time, a large amount of fixed charge was introduced at the interface, which caused flat band voltage (V_{FB}) shifting that has not been systematically investigated yet.[6,14–16] Fixed charges of high density would cause lower mobility by strong coulombic scattering and shift of the threshold voltage.[17,18] High temperature (450 °C) oxygen annealing was tried to improve the performance of metal-oxide-semiconductor (MOS) capacitor.[19] Even though noticeable V_{FB} shift appeared after annealing, the cost was serious degradation of equivalent oxide thicknesses (EOT). In this work, we present O_2 annealing as an effective method to largely neutralize the fixed charges GeO_2 IL based MOS capacitors at relatively low temperatures.

Ge (100) wafers were first cleaned by a 2% HF solution for 1 min at room temperature and then rinsed by a large amount of de-ionized water for 5 min to remove the remaining F ions on the surface. Before the deposition of HfO_2, the wafer was heated to 200 °C in a homemade atomic layer deposition (ALD) system with a base pressure of 6 * 10^{-8} mbar.[20] An *in situ* passivation of the surface of Ge wafer prior to the dielectric deposition was carried out by an O_2 plasma treatment.[21] Following this, HfO_2 was deposited on the germanium oxide by plasma enhanced atomic layer deposition (PEALD) using Tetrakis-(ethylmethylamido) hafnium (TEMAH) and O_2. 40 nm Pt as top gate electrode formed by shadow mask and 20nmTi/40nmPt as back contact were sputtered on the two sides of the device separately. Two types of post metal annealing (PMA) were conducted in a forming gas ambient and in an oxygen/nitrogen mixed ambient with 10% atomic concentration of oxygen. The thickness of the HfO_2 was measured by x-ray reflectivity (XRR). The chemical composition of the passivated Ge wafer was characterized by x-ray photoelectron spectroscopy (XPS) using Al Kα x-rays. Capacitance-voltage measurements were conducted using a HP 4192A impedance analyzer while the actual applied voltage on the MOS structure was read out by HP 3478A multimeter.

Completely oxidized Ge was widely considered to be the best IL with lowest interface states.[6] To analyze the oxidation of the Ge in germanium oxide formed by O_2 plasma passivation, XPS characterization was applied on the IL. To protect the surface from air, a 1 nm Al_2O_3 capping layer was deposited on the passivated Ge by ALD prior to XPS measurement. In Fig. 1, the Ge 3d peak

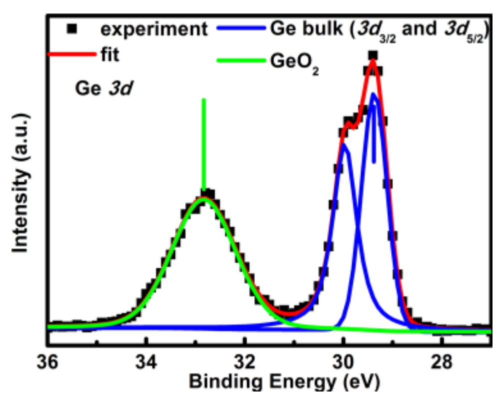

FIG. 1. (Color online) XPS Ge 3d spectra for the $Al_2O_3/HfO_2/GeO_2/Ge$ sample.

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TABLE I. Variety of V_{FB} and D_{it} after FGA or O_2 annealing at 300 and 350 °C.

Annealing ambient/temperature	V_{FB} EOT = 1.3 nm	V_{FB} EOT = 1.8 nm	V_{FB} EOT = 3.1 nm	D_{it}
FGA 300 °C	0.5 V	0.35 V	0.2 V	$7 * 10^{11}$ eV^{-1} cm^{-2}
FGA 350 °C	0.5 V	0.35 V	0.2 V	$4 * 10^{11}$ eV^{-1} cm^{-2}
O_2 annealing 300 °C	NA	0.55 V	NA	$6 * 10^{11}$ eV^{-1} cm^{-2}
O_2 annealing 350 °C	0.72 V	0.70 V	0.65 V	$2 * 10^{11}$ eV^{-1} cm^{-2}

shifted from 29.4 to 32.8 eV, indicating that the oxidation state of Ge is 4+. Simultaneously, no obvious doublets in the fitting curve can be seen between the peak of Ge4+ and bulk Ge, which implies very limited existence of a suboxidation state of Ge. The XPS result of Ge 3d indicates that Ge was completely oxidized by O_2 plasma passivation and exhibited a Ge^{4+} oxidation state.

MOS capacitors experienced forming gas annealing (FGA) at 300 and 350 °C and oxygen annealing at 300, 350, and 400 °C were studied. Among the MOS capacitors after annealing, the one after 400 °C oxygenic annealing, the results showed a 0.2 nm increase of EOT, then limiting further scaling. V_{FB} and D_{it} as a function of EOT after FGA or O_2 annealing at 300 and 350 °C without EOT degradation are listed in Table I. The two capacitors after 300 °C FGA and 300 °C oxygen annealing show relatively high D_{it} (around $7 * 10^{11}$ eV^{-1} cm^{-2}), even though the V_{FB} of the MOS capacitor after 300 °C oxygen annealing shifted from 0.35 to 0.55 V. Only the MOS capacitor after 350 °C annealing has relative high V_{FB} shift from 0.35 to 0.7 V and no degradation of EOT. Therefore, 350 °C annealing in O_2 ambient was selected for further investigation. C-V characterizations as illustrated in the Figs. 2(a) and 2(b) show the electrical properties of the MOS capacitors with 5.5 nm HfO_2 on n type Ge after FGA and O_2 annealing at 350 °C for 30 min. After O_2 annealing, the stretch out of the C-V curve is less than after FGA annealing while the EOT of these capacitors are both 1.8 nm. Using the high-low frequency method, the calculated D_{it} after 350 °C FGA and O_2 ambient annealed are 4×10^{11} eV^{-1} cm^{-2} and 2×10^{11} eV^{-1} cm^{-2} at $V_{FB,}$ respectively. The voltage of the mid gap of the capacitor shifts from 0 V for FGA to around 0.5 V after O_2 annealing. This shift is related to the large amount of fixed charges introduced during O_2 plasma passivation or HfO_2 growth. Bellenger's work showed that the density of this fixed charge was about 2-3 $\times 10^{12}$ cm^{-2} in the case of a HfO_2/GeO_2 gate stack,[6] i.e., in the range lower than 1% compared to the surface density of Ge (100). This is far below the detection limit of most physical characterization techniques, e.g., XPS.

The fixed charges could be present at the interface of HfO_2/GeO or GeO_2/Ge, at the bulk of GeO_2 or $HfO_{2.}$ Therefore, the V_{FB} of the $Pt/HfO_2/GeO_2/Ge$ structure can be expressed as below

$$V_{FB} = \phi_{ms} - \frac{Q_{fixed1}}{C_{fixed1}} - \frac{Q_{fixed2}}{C_{fixed2}} - \int_0^{t_{GeO_2}} \frac{Q_{GeO_2bulk}(x)}{\dfrac{\dfrac{\varepsilon_0\varepsilon_{HfO_2}}{t_{HfO_2}} \times \dfrac{\varepsilon_0\varepsilon_{GeO_2}}{x}}{\dfrac{\varepsilon_0\varepsilon_{HfO_2}}{t_{HfO_2}} + \dfrac{\varepsilon_0\varepsilon_{GeO_2}}{x}}} dx - \int_0^{t_{HfO_2}} \frac{Q_{HfO_2bulk}(y)}{\dfrac{\varepsilon_0\varepsilon_{HfO_2}}{y}} dy, \quad (1)$$

where in the first three terms, ϕ_{ms}, Q_{fixed1}, C_{fixed1}, Q_{fixed2}, C_{fixed2} are the differences in work function between gate electrode and Ge, the density and the capacitance of the fixed charge at the HfO_2/GeO_2 interface, and the density and the capacitance of the fixed charge at the GeO_2/Ge interface, respectively. In the last two terms, t_{GeO_2}, t_{HfO_2}, $Q_{GeO_2bulk}(x)$, $Q_{HfO_2bulk}(y)$, ε_{SiO_2}, ε_{HfO_2}, ε_0 are the physical thicknesses of GeO_2 and HfO_2, the densities of the fixed charge in bulk GeO_2 and bulk HfO_2, the permittivities of SiO_2, HfO_2, and vacuum. X is the distance from the interface of HfO_2/GeO_2. Y is the distance from the interface of Pt/HfO_2. Here, the effect of D_{it} has been ignored due to the very low D_{it} (2×10^{11} eV^{-1} cm^{-2}) compared to the density of the fixed charges in these MOS capacitors.

Each term of Eq. (1) will have a specific contribution to the total V_{FB}. To find out the distribution of the fixed charges and quantitatively evaluate the effect of O_2 annealing and FGA on the fixed charges, three types of capacitors with 3.9, 5.5, 13 nm HfO_2 were fabricated with the same processing as stated above, using 350 °C annealing temperature. After C-V characterization, it is found that due to the high quality passivation and HfO_2, the D_{it} of the capacitors after FGA

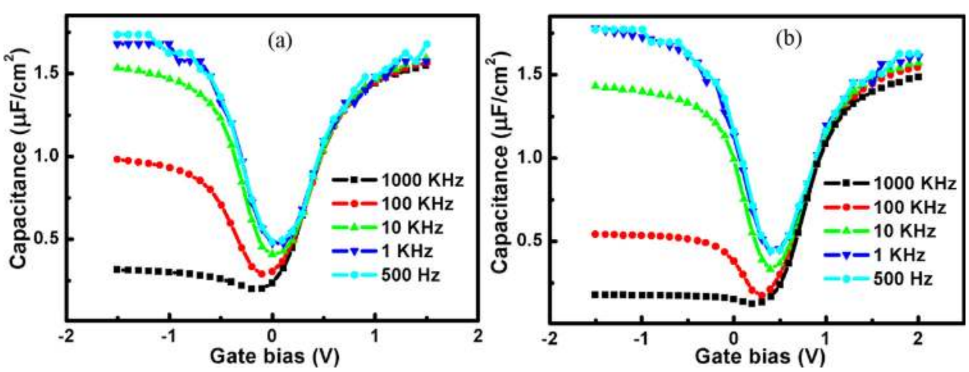

FIG. 2. (Color online) The C-V characterization of MOS capacitors with $Pt/HfO_2/GeO_2/Ge$ after (a) 350 °C FGA and (b) 350 °C oxygen ambient annealing.

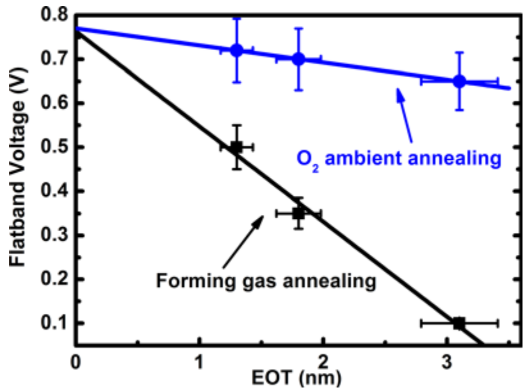

FIG. 3. (Color online) Flatband voltages vs EOT after 350 °C FGA and oxygenic ambient annealing.

and O_2 annealing do not vary with the EOT. The V_{FB} was plotted in Fig. 3 as a function of EOT. According to the linear shape of the fitting line, the distribution of the fixed charges could be located at the GeO_2/Ge interface, but not in the bulk GeO_2 or at the HfO_2/GeO_2 interface. Otherwise, the integration of the third and fourth term in Eq. (1) would result in a non linear function of EOT which does not agree with the fitting. In addition, regarding the contribution from bulk HfO_2 in the fourth term, we also fabricated Pt/HfO_2/IL/Si MOS capacitors for control samples and found that the V_{FB} is also a linear function of EOT. The extracted density of fixed charges is below 5×10^{11} cm^{-2}. Accordingly, the fixed charges in the bulk of HfO_2 are under the detection limit of electrical measurements as the ones in bulk GeO_2. Therefore, the fourth term of the Eq. (1) can be ignored. Considering the first term in Eq. (1), we further studied the intercepts of these two fitting lines in Fig. 3. These intercepts on Y axis are both 0.77 V, which implies that the work function of Pt on HfO_2 is about 4.9 eV which is consistent with the reported data.[22] Thereby, the distribution of the fixed charges would not be at the HfO_2/GeO_2 interface. Otherwise the intercepts would not be the same and result in different effective work functions of Pt, because the V_{FB} will not be the function of EOT but the function of the equivalent oxide thickness of HfO_2. Simultaneously, the very low CV hysteresis of 50 mV also implies limited intermixing between HfO_2 and GeO_2.[23] Therefore, the interface of HfO_2/GeO_2 is probably intact. According to the above calculation and reasoning, the Eq. (1) can be consequently written as

$$V_{FB} = \phi_{ms} - \frac{Q_{fixed2}}{C_{fixed2}} \quad (2)$$

which only counts in the contribution of ϕ_{ms} and the fixed charges at the GeO_2/Ge interface.

The negative slope of the fitting lines also elucidates that the sign of fixed charges introduced by using TEMAH as Hafnium precursor in ALD is positive. This agrees well with Sreenivasan's report on the sign of fixed charges in Si based MOS capacitor by using different types of Hf precursors in the ALD process.[24] From the plot the fixed charge densities after two types of annealing were calculated individually by extracting the slope of the Eq. (2). The fixed charges density of the capacitor after FGA is 4.5×10^{12} cm^{-2} while the density is 8.2×10^{11} cm^{-2} after O_2 annealing. This significant reduction of fixed charges can be interpreted by the assumption that O_2 annealing introduces extra oxygen into the gate stack and reduce the number of the oxygen vacancies or Ge dangling bonds. Henkel *et al.* reported that only very thin Pt electrode with thickness of 5 nm could act as an assistant media in O_2 annealing at 450 °C for D_{it} reduction, but it was at the price of large compromising EOT.[19] However, in our processing, the oxygen annealing still influences the performance of the MOS capacitor even when the top Pt electrode is 40 nm. Of more importance, due to the lower annealing temperature in our process, the EOT is not affected, while both the D_{it} and the density of fixed charges decrease significantly. This is consistent with slow growth rate of GeO_2 in pure oxygen at 350 °C reported in Ref. 6.

In summary, the O_2 ambient annealing not only amends the D_{it} of Ge based MOS capacitor but also effectively reduces the density of fixed charges located at the interface of GeO_2/Ge. Without compromising the EOT of the capacitors, the benefits of O_2 annealing at 350 °C suggest that it is a promising process to enhance the performance of Ge based MOS devices and offers the possibility for device scaling down.

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