# Effectiveness of Reverse Body Bias for Leakage Control in Scaled Dual Vt CMOS ICs

A. Keshavarzi, S. Ma, S. Narendra, B. Bloechel, K. Mistry*, T. Ghani*, S. Borkar and V. De
Microprocessor Research Labs, Intel Corporation, Hillsboro, OR
*Portland Technology Development, Intel Corporation, Hillsboro, OR
ali.keshavarzi@intel.com

## ABSTRACT

We examine the effectiveness of opportunistic use of reverse body bias (RBB) to reduce leakage power during active operation, burn-in, and standby in 0.18µm single-$V_t$ and 0.13µm dual-$V_t$ logic process technologies. We investigate its dependencies on channel length, target $V_t$, temperature and technology generation. We show that RBB becomes less effective for leakage reduction at shorter channel lengths and lower $V_t$ at both high and room temperatures, especially when target intrinsic leakage currents are high. RBB effectiveness also diminishes with technology scaling primarily because of worsening short-channel effects (SCE), particularly when target $V_t$ values are low. We present a model that relates different transistor leakage components to full-chip leakage current, and validate the model through testchip measurements across a range of RBB values.

## 1. Introduction

In order to sustain historical improvements in both energy and delay as we scale technology, $V_{dd}$ and $V_t$ must be reduced simultaneously. $V_t$ scaling causes the subthreshold leakage current of the transistor to increase exponentially, resulting in unacceptably large leakage power. In order to minimize the standby leakage power of a chip, application of reverse body bias (RBB) to the transistors has been proposed [1-4]. It has also been shown that for 0.35µm and 0.18µm single-$V_t$ logic process technologies, an optimal RBB voltage exists that yields maximum standby leakage reduction [5-7].

In this paper, we investigate applications of RBB to reduce leakage power during active operation and burn-in, as well as during standby, in a 0.18µm single-$V_t$ and a 0.13µm dual-$V_t$ logic technology. Chip performance is dictated by target $V_t$ or the intrinsic subthreshold leakage of nominal length devices with zero body bias (NBB). During active operation, RBB is applied to idle portions of the chip to reduce overall chip leakage power, without impacting performance. RBB can be applied to the whole chip during burn-in to reduce leakage power since the chip is required to operate at very low frequency during burn-in. Reducing leakage power during burn-in is needed to prevent thermal runaway. We use transistor leakage measurements at 110°C (junction temperature during active operation and burn-in) and 27°C (junction temperature during standby) to study leakage reduction achievable by RBB. We also examine its dependencies on channel length, target $V_t$, temperature and technology generation.

These dependencies are explained using device physics principles. We assess the impact of RBB on full-chip leakage current using models which relate individual device leakage current components to circuit leakage. The models are validated by measurements of device and circuit leakage currents on a testchip. Results in this paper are applicable for opportunistic usage of body bias in a microprocessor logic technology optimized for high performance without applying body bias. Technologies that are not targeted for high performance or optimized for body bias application may show different results.


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## 2. Effectiveness of RBB for Leakage Reduction

Full chip leakage current is the aggregate sum of leakage currents of "OFF" NMOS and PMOS transistors in the design. Subthreshold leakage current of a transistor depends strongly on gate length. The actual gate lengths of identically drawn minimum length ($L_{nom}$) transistors vary across a die. These within-die gate length variations cause different transistors of the same drawn length and width to contribute different amounts of leakage current to the total chip leakage. Transistors with shorter lengths contribute exponentially more to the overall chip leakage current. Therefore, to understand the impact of RBB on full-chip leakage from individual transistor leakage current measurements, we examine leakage currents of not only the $L_{nom}$ devices, but also the expected shortest length ($L_{wc}$) devices.

Components of transistor leakage and their mechanisms were discussed earlier in [5]. In this paper, we focus on intrinsic subthreshold leakage ($I_{int}$), extrinsic leakage ($I_{ext}$), drain-body junction leakage ($I_j$), and source-body junction leakage ($I_B$) components to examine and understand leakage control achievable by RBB (Fig. 1). $I_{ext}$ is measured at the transistor drain terminal for $V_{ds}=V_{dd}=1V$ and $V_{GS}=0V$. It contains various transistor leakage components such as subthreshold, drain-induced barrier lowering (DIBL), and junction leakages including gate-induced drain leakage (GIDL). $I_{int}$ is simply the transistor subthreshold leakage. It is obtained by subtracting the source-body junction current from the total source-terminal leakage current ($I_{source}$). $I_j$ is the difference between $I_{ext}$ and $I_{int}$.

Fig. 2 shows that as we reduce channel length, the intrinsic leakage increases. In addition, we see that applying 1V RBB reduces transistor leakage by more than an order of magnitude at nominal transistor channel lengths. However, the effectiveness of RBB diminishes at shorter lengths. Fig. 2 also allows us to select a nominal length transistor and its leakage value, and a transistor of worst-case shortest length and its leakage. We assume that leakage of a transistor with $L_{wc}$ length is 10X higher than that of a device with $L_{nom}$ length. Fig. 3 shows that there is a minimum in extrinsic

leakage of the $L_{nom}$ transistor which occurs at an optimum RBB value of ~0.5V. This optimum RBB value exists because of two competing factors - reduction in intrinsic subthreshold leakage with increasing RBB and simultaneously larger drain-body junction leakage. As shown in Fig. 3, junction leakage is much smaller than intrinsic leakage at zero body bias. As we increase RBB, intrinsic subthreshold leakage reduces and junction leakage increases. $I_j$ and $I_{int}$ are comparable around the optimum RBB, leading to a minimum $I_{ext}$. For the $L_{wc}$ device, on the other hand, $I_j$ is always much smaller than $I_{int}$ for RBB values up to 1.5V. Therefore, no optimum RBB is observed up to 1.5V for the $L_{wc}$ transistor.

Different mechanisms contribute to junction leakage [5,7]. We measured drain-body junction leakage currents at high and low temperatures. The ratios of junction leakage at 110°C to 27°C, shown in Fig. 4, suggest that the dominant junction leakage mechanism changes with increasing RBB value. For RBB values up to 0.5V, the dominant mechanism is thermal emission, which causes junction leakage to increase strongly with temperature. Beyond 0.5V RBB, the dominant mechanism is band-to-band tunneling (BTBT), at surface and/or bulk, and hence the junction leakage is weakly dependent on temperature.

Fig. 5 shows intrinsic leakage reduction achievable with 0.5V RBB as a function of target zero body bias leakage current for low-$V_t$ and high-$V_t$ transistors in a 0.13µm dual-$V_t$ logic technology. We examine the effectiveness of RBB over a range of transistor lengths spanning both different drawn lengths and natural length variations typical of a process technology. Transistors with shorter lengths have lower $V_t$ and higher $I_{int}$, primarily due to worse DIBL and short-channel $V_t$ roll-off (SCE). This is true regardless of whether the target $V_t$ values of the transistors are high or low. Reduction in $I_{int}$ achievable using RBB depends primarily on the amount of body effect. Body effect depends strongly on transistor length or the degree of SCE, and target $V_t$ (or channel doping). As we reduce the transistor length for a particular target $V_t$ in a specific technology generation, body effect becomes weaker because SCE worsens. Body effect also becomes weaker as we reduce target $V_t$ by reducing channel doping, while keeping the target gate length unchanged in a particular technology generation. Therefore, as seen from Fig. 5, the effectiveness of RBB for intrinsic leakage reduction diminishes in both cases. Thus, the higher the intrinsic leakage, the smaller is the leakage reduction achievable by RBB.

A specific zero body bias intrinsic leakage, needed for meeting a target circuit performance, can be achieved by targeting a smaller gate length and/or by reducing channel doping to get a lower target $V_t$. The data in Fig. 5 suggests that if length is reduced to achieve a target intrinsic leakage (and circuit performance), then RBB is not as effective for leakage reduction as in the case where the target leakage (and performance) is achieved by reducing channel doping to lower $V_t$. However, targeting smaller channel length has the additional advantage of reducing capacitance, and hence might allow a specific circuit performance target to be met at a slightly smaller intrinsic leakage target to begin with. We see similar behaviors with respect to temperature at 110°C and 27°C (Figs. 5a and 5b).

Fig. 6 shows the effectiveness of RBB for reducing extrinsic leakage over a range of channel lengths and a corresponding range of intrinsic leakage currents at zero body bias. Clearly, for very small and very large target intrinsic leakage currents, the effectiveness of RBB for extrinsic leakage reduction becomes small. For devices with small intrinsic leakage, one does not achieve much extrinsic leakage reduction with RBB because junction leakage is comparable to intrinsic leakage. For devices with large intrinsic leakage currents, extrinsic leakage reduction by RBB is comparable to intrinsic leakage reduction. This is because intrinsic subthreshold leakage is the dominant component of the total leakage and junction leakage contribution is negligible. The hump in the extrinsic leakage reduction by RBB vs. intrinsic leakage (Figs. 6a and 6b) behavior is wider at lower temperature because intrinsic leakage currents are smaller and the junction leakage current has weak temperature dependence at large RBB values.

Degradation of SCE also manifests itself through a larger variation in transistor leakage. Leakage currents of transistors having worse SCE are more susceptible to changes in critical dimensions. Since applying RBB degrades SCE [5-8], leakage current variation increases with RBB. Figs. 7 and 8 show that standard deviation of the leakage current distribution becomes a larger portion of the mean leakage with larger RBB values for both NMOS and PMOS transistors.

## 3. Scaling Trends of RBB Effectiveness

Impact of transistor scaling on the effectiveness of RBB for leakage control at 110°C is shown in Figs. 9 and 10. Two technologies are compared: a single-$V_t$ 0.18µm technology and a dual-$V_t$ 0.13µm technology. In both technologies, leakage currents are measured at $V_{ds}=V_{dd}=1V$. Thus, we neglect the impact of $V_{dd}$ scaling from one technology generation to next. Note in Fig. 9 that achievable intrinsic leakage reduction using RBB degrades with channel length reduction in a stronger fashion for low-$V_t$ devices in 0.13µm technology when compared to devices in 0.18µm technology. This means that as we scale the transistors from one technology generation to next, keeping SCE under control becomes more challenging. This problem is also manifested in the diminishing leakage reduction achievable by RBB as we scale technology. As seen from Fig. 9, for a 10nA/µm target NBB intrinsic leakage (at 110°C) in a 0.18µm technology, 4-5X leakage reduction is achieved by applying 0.5V RBB. In a 0.13µm technology, 0.5V RBB reduces leakage of the high-$V_t$ device (with 30nA/µm target NBB intrinsic leakage at 110°C) by 3-3.5X, and that of the low-$V_t$ device (with 300nA/µm target NBB intrinsic leakage at 110°C) by 2.5-3X. Since low-$V_t$ devices dominate the total chip leakage current for dual-$V_t$ designs in 0.13µm technology [11], leakage current reduction by RBB goes down from 4X for 0.18µm technology to 2.5X. It is clear that worsening SCE is the primary reason why RBB becomes less effective for leakage reduction with scaling, especially when target $V_t$ values are low. Well doping and halo implants can be further optimized to improve SCE. However, both of these techniques cause the doping levels in the vicinity of source-body and drain-body junctions to increase significantly. As the doping level approaches the tunneling limit, the junction current increases exponentially, and becomes the dominant leakage component [10]. Also, it causes junction breakdown voltage to reduce significantly. This further renders the application of RBB for leakage reduction virtually ineffective especially for burn-in where the stress voltage is higher than $V_{dd}$.

## 4. Full-Chip Leakage Reduction by RBB

The leakage current $I_{dd}$ in the $V_{dd}$ rail of a chip can be related to the different transistor leakage current components as follows (as illustrated in Fig. 1):

$$I_{dd} = 1/k\ [W_p \times (|I_{intP}| - |I_{BP}|) + W_n \times (|I_{intN}| + |I_{jN}|)]$$

where $W_p$ and $W_n$ are the total PMOS and NMOS transistor widths, respectively. 1/k represents width of "OFF" NMOS and PMOS devices as a fraction of the total device width. We see from the above equation that intrinsic leakages of both NMOS and PMOS devices contribute to full-chip leakage $I_{dd}$, and reduce monotonically with increasing RBB. $I_j$ of PMOS does not contribute to $I_{dd}$, whereas $I_j$ of NMOS does. PMOS $I_B$ contributes to $I_{dd}$, but causes it to reduce with increasing RBB. Therefore, a minimum in $I_{dd}$ with increasing RBB can occur only if the drain-body junction leakage of the NMOS is dominant. Thus, while the optimum RBB values that minimize extrinsic leakage currents of individual NMOS and PMOS devices are governed by their respective drain-body junction currents, optimum RBB which minimizes full-chip leakage current is determined by the junction leakage of NMOS only, not PMOS. Therefore, device designs that reduce drain-body junction leakages of NMOS transistors only should enhance the effectiveness of RBB for full-chip leakage current reduction.

Since $I_{source} = |I_{int}| - |I_B|$ and $I_{ext} = |I_{int}| + |I_j|$, $I_{dd}$ can be obtained in terms of direct transistor leakage current measurements at source terminal of PMOS ($I_{sourceP}$) and drain terminal of NMOS ($I_{extN}$) as,

$$I_{dd} = 1/k\ [W_p \times I_{sourceP} + W_n \times I_{extN}]$$

The full-chip leakage current of a testchip in a 0.18µm technology with 20000 transistors and different types of logic gates is estimated using this equation. k = 2 is used because approximately half of the devices on the chip are OFF when the chip is in standby mode. The upper and lower bounds of $I_{dd}$ are estimated for different RBB values using leakage current measurements of $L_{wc}$ and $L_{nom}$ devices, respectively. As shown in Figs. 11 and 12, the measured full-chip leakage current is within these upper and lower leakage current bounds over a range of RBB values. This validates the chip leakage current estimation procedure based on direct device leakage measurements. In addition, as seen from Figs. 11 and 12, the optimum RBB value derived from the measured chip leakage is close to that obtained by the model calculations at both 110°C and 27°C.

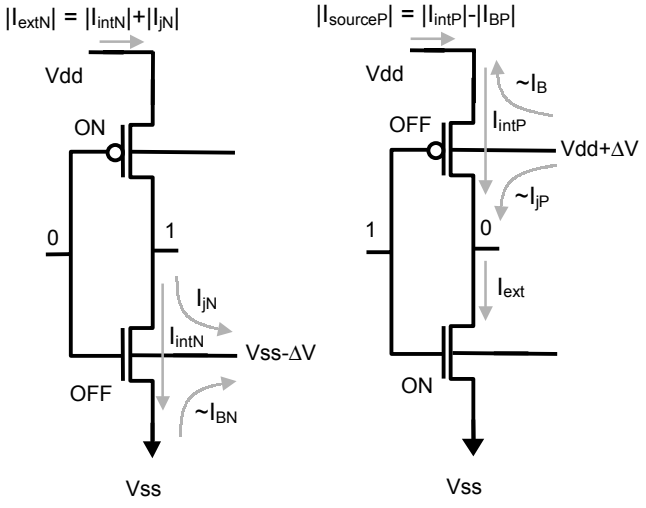


**Fig. 1** Components of NMOS and PMOS transistor leakage contributing to chip $I_{dd}$ leakage i.e. the current in the $V_{dd}$ pin.

## 5. Conclusions

We have examined the effectiveness of RBB to reduce leakage power during active operation, burn-in, and standby in 0.18µm single-$V_t$ and 0.13µm dual-$V_t$ logic technologies for high performance microprocessors. We have studied RBB dependencies on channel length, target $V_t$, temperature and technology generation. We have shown that RBB becomes less effective for leakage reduction at shorter channel lengths and lower $V_t$ at both high and room temperatures when target leakage currents are large. RBB effectiveness also diminishes with technology scaling primarily because of worsening SCE. This is especially true when the target $V_t$ value is low. We have presented a model that relates different transistor leakage components to full-chip leakage current, and have validated the model through measurements on a testchip across a range of RBB values.

## 6. Acknowledgments

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## 7. References

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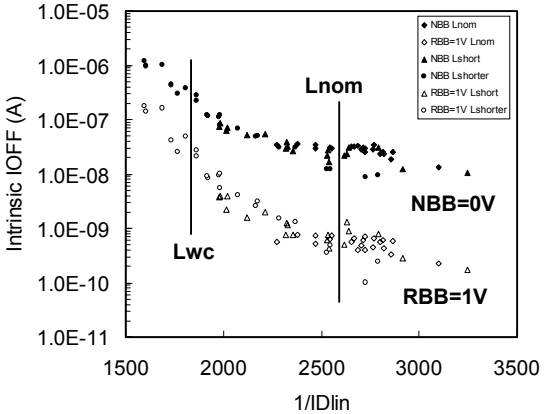


**Fig. 2** Transistor leakage as a function of transistor channel length L for NBB and 1V RBB. A plot of NMOS intrinsic IOFF at $V_{DS}=V_{dd}=1V$ versus 1/IDlin representing transistor L at T=110°C. Data from 3 drawn L's in a 0.18 µm technology. Diamonds for $L_{nom}$, Triangles for L short, and Circles for L even shorter. IDlin is measured at $V_{DS}=50$ mV and $V_{GS}=V_{dd}=1V$. Assumption: $L_{wc}$ transistor has 10X higher leakage than $L_{nom}$.

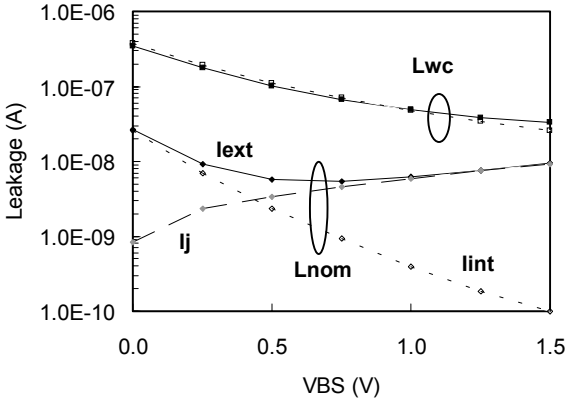


**Fig. 3** Components of transistor leakage as a function of Reverse Body Bias (RBB). A plot of intrinsic (dashed lines), extrinsic (solid lines), and junction leakage components versus RBB for $L_{nom}$ and $L_{wc}$ selected die from Fig. 1. Plot for NMOS transistors at T=110°C. RBB (VBS) voltage in absolute value.

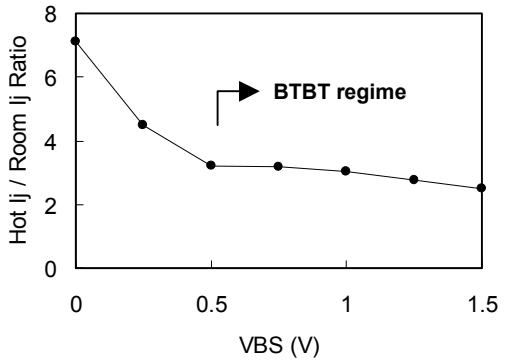


**Fig. 4** Ratio of hot (T=110°C) to room (T=27°C) temperature junction leakage as a function of RBB. $I_j$ mechanisms change from emission over a barrier to BTBT by increasing RBB.

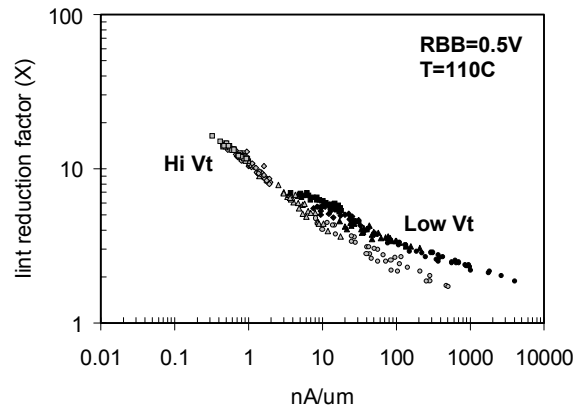


**Fig. 5a** Ratio X of NBB to RBB intrinsic leakage current as a function of original leakage current without applying any RBB (i.e NBB) at T=110°C. This represents the leakage reduction by applying 0.5V of RBB for a 0.13µm dual-$V_t$ technology. Intrinsic PMOS transistor leakage ($I_{int}$) measured at $V_{DS}=V_{dd}=1V$. Data from 4 drawn L's. Diamonds for $L_{nom}$, Triangles for L short, Circles for L even shorter, and Squares for L long.

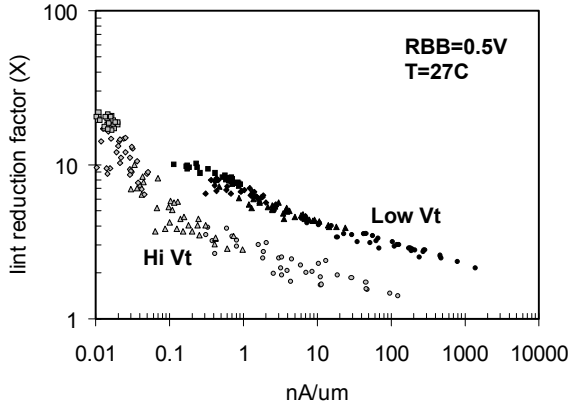


**Fig. 5b** Ratio X of NBB to RBB intrinsic leakage current as a function of original leakage current without applying any RBB (i.e NBB) at T=27°C. This represents the leakage reduction by applying 0.5V of RBB for a 0.13µm dual-$V_t$ technology. Intrinsic PMOS transistor leakage ($I_{int}$) measured at $V_{DS}=V_{dd}=1V$. Data from 4 drawn L's. Diamonds for $L_{nom}$, Triangles for L short, Circles for L even shorter, and Squares for L long.

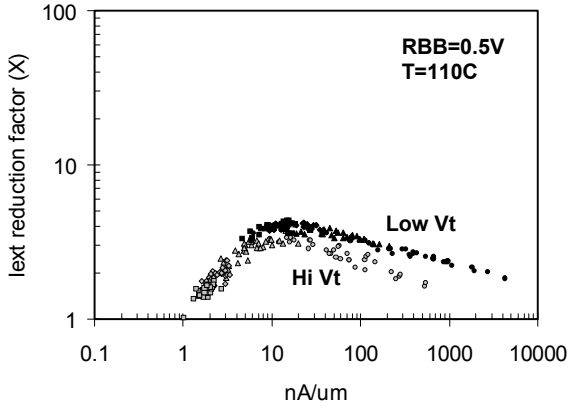


**Fig. 6a** Ratio X of NBB to RBB extrinsic leakage current as a function of original leakage current without applying any RBB (i.e NBB) at T=110°C. This represents the leakage reduction by applying 0.5V of RBB for a 0.13µm dual-$V_t$ technology. Extrinsic PMOS transistor leakage ($I_{ext}$) measured at $V_{DS}$=$V_{dd}$=1V. Data from 4 drawn L's. Diamonds for $L_{nom}$, Triangles for L short, Circles for L even shorter, and Squares for L long.

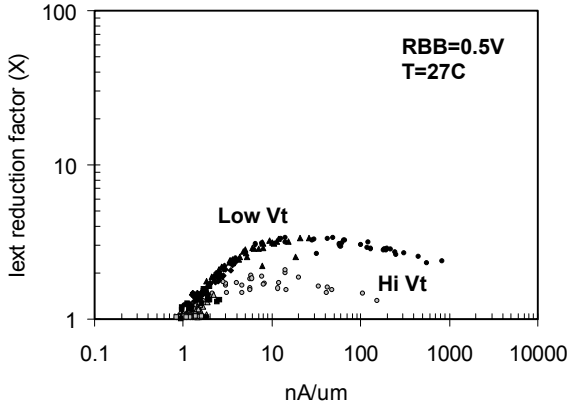


**Fig. 6b** Ratio X of NBB to RBB extrinsic leakage current as a function of original leakage current without applying any RBB (i.e NBB) at T=27°C. This represents the leakage reduction by applying 0.5V of RBB for a 0.13µm dual-$V_t$ technology. Extrinsic PMOS transistor leakage ($I_{ext}$) measured at $V_{DS}$=$V_{dd}$=1V. Data from 4 drawn L's. Diamonds for $L_{nom}$, Triangles for L short, Circles for L even shorter, and Squares for L long.

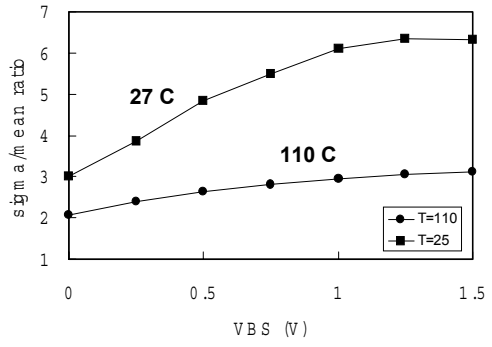


**Fig. 7** Ratio of standard deviation (sigma) to mean of measured NMOS intrinsic transistor leakage ($I_{int}$) as a function of increasing magnitude of RBB. Data from 0.18µm technology at two different temperatures at $V_{DS}$=$V_{dd}$=1V.

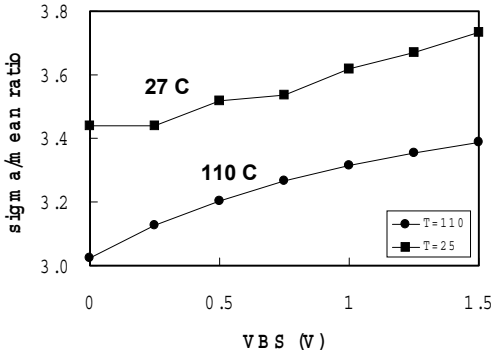


**Fig. 8** Ratio of standard deviation (sigma) to mean of measured PMOS intrinsic transistor leakage ($I_{int}$) as a function of increasing magnitude of RBB. Data from 0.18µm technology at two different temperatures at $V_{DS}$=$V_{dd}$=1V.

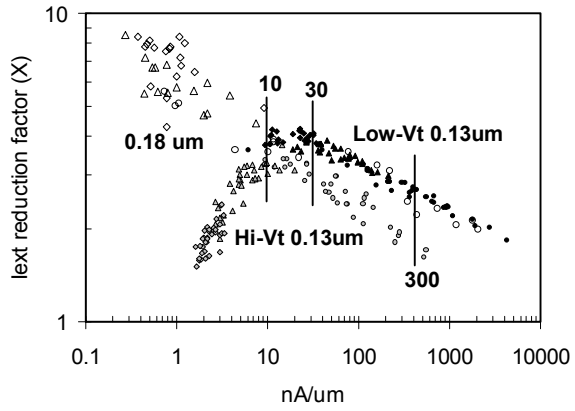


**Fig. 9** Scaling trends by Ratio X of NBB to RBB extrinsic leakage current ($I_{ext}$) as a function of original NBB leakage current. Data for 0.5V of RBB at T=110°C at $V_{DS}=V_{dd}=1V$ across two generations of technologies. Note 0.18µm data is shown by not filled symbols, hi-$V_t$ 0.13µm with gray symbols, and low-$V_t$ 0.13µm by black symbols. Studying $I_{ext}$ reduction at 10 nA/µm for 0.18 µm technology, 30 nA/µm for hi-$V_t$ 0.13 µm technology, and 300 nA/µm for low-$V_t$ 0.13µm technology.

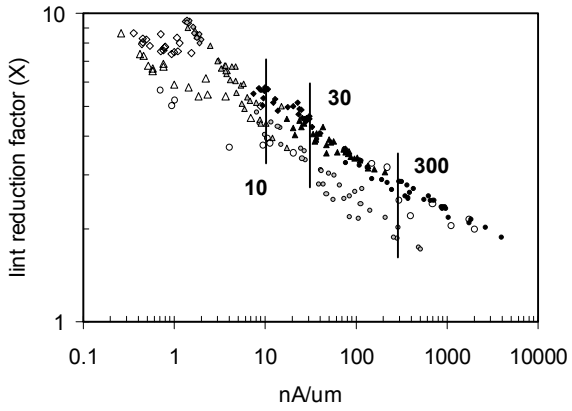


**Fig. 10** Scaling trends by Ratio X of NBB to RBB intrinsic leakage current ($I_{int}$) as a function of original NBB leakage current. Data for 0.5V of RBB at T=110°C at $V_{DS}=V_{dd}=1V$ across two generations of technologies. Note 0.18µm data is shown by not filled symbols, hi-$V_t$ 0.13µm with gray symbols, and low-$V_t$ 0.13µm by black symbols. Studying $I_{int}$ reduction at 10 nA/µm for 0.18 µm technology, 30 nA/µm for hi-$V_t$ 0.13 µm technology, and 300 nA/µm for low-$V_t$ 0.13µm technology.

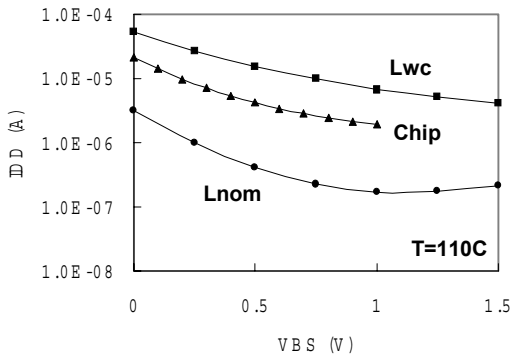


**Fig. 11** Comparing actual chip $I_{dd}$ leakage with estimated chip leakage from $L_{nom}$ and $L_{wc}$ transistor measurements as a function of RBB at T=110°C. Data from 0.18µm technology.

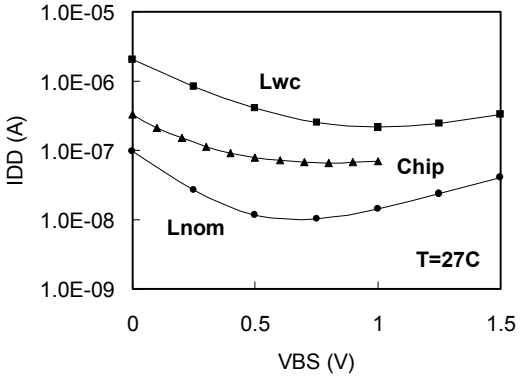


**Fig. 12** Comparing actual chip $I_{dd}$ leakage with estimated chip leakage from $L_{nom}$ and $L_{wc}$ transistor measurements as a function of RBB at T=27°C. Data from 0.18µm technology.