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V. Kaushal, Ignacio Iniguez-de-la-Torre, Tomas Gonzalez, Javier Mateos ...+3 more authors

Institutions: University of Massachusetts Lowell, North Carolina State University

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Effect of high-k dielectric on the performance of III-V Ballistic Deflection Transistors

Vikas Kaushal, Ignacio Íñiguez-de-la-Torre, Tomás González, *Senior Member, IEEE*, Javier Mateos, *Member, IEEE*, Bongmook Lee, Veena Misra, and Martin Margala, *Senior Member, IEEE*

***Abstract*— This letter presents a first successful integration of a high-k dielectric, Al_2O_3, with III-V semiconductors in ballistic deflection transistors (BDT). The Al_2O_3 is deposited by means of atomic layer deposition allowing the formation of uniform layers along the walls of etched trenches. The BDT transfer characteristic shows a strong dependence on the dielectric permittivity of the material filling the etched trenches. The transconductance of the BDT is enhanced and shifted to lower gate bias when the Al_2O_3 is deposited in the trenches. Moreover, the ratio between output and leakage currents was also enhanced.**

***Index Terms*— high-k dielectric, III-V semiconductors, nanodevices.**

I. Introduction

Rroom temperature (RT) ballistic devices have emerged as possible candidate to fabricate high speed circuits for analog and digital applications [1]. Advance methods like focused ion beam and e-beam lithography (EBL) allow us to “write” insulating lines to strategically define shapes and edges in semiconductor heterostructures [2, 3]. Two devices which exhibit nonlinear electrical properties at RT are: Ballistic Rectifier [4] and Y-Branch Junction [5, 6]. In the same context, based on the pioneer work [7], we proposed a novel Ballistic Deflection Transistor (BDT) [8]. BDT has positive and negative transconductance regions, which enable inverting or non-inverting circuits depending only on gate offset voltage [9]. The non-linear transfer characteristic makes the BDT an ideal frequency doubler [10] and it provides logic capability [11, 12]. Monte Carlo (MC) simulations estimated a maximum operation of 400 GHz at RT as frequency doubler [12].

In the BDT, the presence of a confined electric field parallel to the 2DEG can be used to improve the electrostatic coupling between gate and the channel through the dielectric trenches. In this letter, we integrate InGaAs/InAlAs/InP with Al_2O_3, a high-k dielectric, and study the performance of the BDT in terms of its transconductance (g_m) and leakage. The deposition of Al_2O_3 in the trenches enhances the capacitive coupling, which increases the gate control over the channel conduction. Gate control can also be increased by reducing the trench width, but it increases the gate leakage significantly.

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II. BDT Description and Importance of High-k

Fig. 1(a) shows the heterostructure of BDT. BDT consists of lattice matched InGaAs and InAlAs layers on an InP substrate. In particular, a 450 nm InAlAs buffer layer, a 50 nm InGaAs channel layer, 20 nm of InAlAs spacer layer followed by a planar silicon δ-doped ($N_\delta=2\times10^{12}$ cm^{-2}) InAlAs layer, a 30 nm Schottky barrier layer and finally a 10 nm InGaAs undoped cap layer. The measured RT mobility μ and sheet electron density n_s of 2DEG were 1.1×10^4 cm^2/Vs and 1×10^{12} cm^{-2}, respectively. The BDT is a six-terminal coplanar structure fabricated by etching into an InGaAs 2DEG with dimensions of the order of the mean free path (~ 200 nm [1] at RT), so that transport exhibits quasi-ballistic features. It consists of a grounded source, left and right gates, and three biased drains depicted in the 3D image of Fig. 1(a). The gate control over the channel can be attributed to three effects, classic channel pinch-off due to field effect, electron steering due to gate bias and deflection due to a deflector. A detailed explanation of the principle of operation can be found in Ref. 13.

The functionality of in-plane gates has already been demonstrated [7]. Recently incorporation of high-k dielectrics into III-V heterostructure devices has been reported [14]. A very recent work shows that by spin-coating a high-k dielectric material onto nanodevices (based on ZnO) enables a higher degree of control over the channel conductance [15]. In addition, MC and TCAD-Medici simulations have shown that the device performance is very sensitive to the depth of insulating trenches and the presence of dielectric layers on the device surface [16, 17]. However, experimentally, high-k dielectric has never been used to fill the trenches in III-V ballistic planar devices. Based on our previous MC results on BDTs [9], we expect that the use of high-k dielectrics (Al_2O_3, HfO_2 or HfAlO) will result in a significant drop in the pinch off voltage and improved transconductance due to higher capacitance in the trenches and better gate-channel coupling.

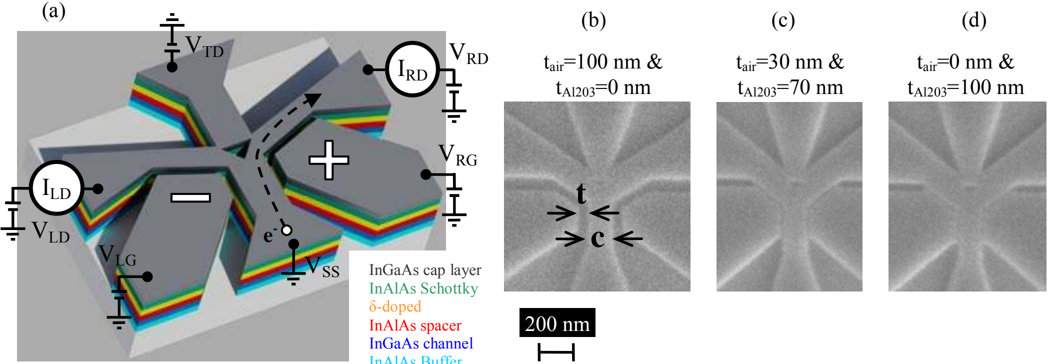

Fig. 1. (a) 3D "artistic" topology and heterostructure of a typical BDT. The top-left (V_{LD}) and top-right (V_{RD}) contacts are drain terminals, bottom-left (V_{LG}) and bottom-right (V_{RG}) terminals are gates, top contact (V_{TD}) is a bias terminal that controls gain, and the bottom terminal (V_{SS}) is the source. Inset: Schematic showing electrons trajectory for positive right gate bias condition ($V_{RG} = -V_{LG}$). SEM image (with scale indicator) of the top view of BDT with channel width c= 140 nm and trench width (b) t_{Al2O3}=0 nm, t_{air}=100 nm (c) t_{Al2O3}=70 nm, t_{air}=30 nm and (d) t_{Al2O3}=100 nm, t_{air}=0 nm.

III. Fabrication Process

For the realization of a BDT, a two step EBL is employed. For the first step, a positive resist 950K PMMA (~170 nm) is spun over a 40 nm Si_3N_4 hard mask before the EBL. After writing the pattern and stripping off the resist, ICP-RIE was done to define the active region of 2DEG layer. The resulting mesa typically has a step height of 130 nm so that all the layers above InAlAs buffer are completely etched away. For the second step of fabrication, EBL is used again to pattern contacts, which are formed using a standard Ni-Ge-Au stack that was annealed at 420°C for 30 sec. The metal layer thickness and the annealing temperature have been optimized, giving an acceptably low contact resistance (~0.2 Ω·mm). Finally, Ti/Au probe pads are patterned and deposited by usual lift-off technique. For this letter, two sets of BDTs are fabricated and measured. One has a channel width, c, of 140 nm [SEM image in Fig 1(b)] and the second is 200 nm wide.

Al_2O_3 dielectric film was deposited by Atomic Layer Deposition (ALD) at 200°C of substrate temperature. ALD Al_2O_3 is a high-quality dielectric on III-V compound semiconductors widely used due to its excellent dielectric properties, strong adhesion to dissimilar materials, high thermal / chemical stabilities and low defect density. Al_2O_3 has a high band gap (~9 eV), a high breakdown electric field (5–30 MV/cm) and a high permittivity (8.6–10). The base pressure of ALD chamber was 400 mTorr with constantly flowing N_2 carrier gas. Trimethylaluminum was used as Al precursor and water was used as a reactant. The ALD Al_2O_3 film can be uniformly deposited at the bottom and at the side walls of the trenches, thus modulating the air trench width. The resulting width of the trench (initially t) after Al_2O_3 deposition (d at both sides) is t–2×d. The idea is to study the coupling effect on the device performance by depositing different thicknesses of Al_2O_3 in the trenches of devices with diverse trench and channel widths. The air trench width chosen is 100 nm. 35 nm and 50 nm of Al_2O_3 layers were deposited atomically, which resulted into 30 nm and 0 nm of air trenches and 70 nm and 100 nm of Al_2O_3 trenches, respectively. SEM images of the devices are shown in Fig. 1(b), (c) and (d).

IV. Experimental Results

Two main effects occur when a high-k dielectric is deposited in the trenches of BDT. First is the generation of surface states at the interface of Al_2O_3 and III-V, which degrades mobility due to an increase in the interface traps, and second is the increase of gate-channel coupling due to an increase in the capacitance in the trenches. Both of these effects reduce the channel current (I_{LD}). The generation of surface states start depleting the channel and an increase in gate-channel coupling results into an earlier channel pinch-off due to a stronger lateral electric field generated by applied gate voltages. This originates a more pronounced variation of the channel current with the applied gate bias, thus leading to an enhanced g_m. Fig. 2(a) confirms that when the trench is filled with Al_2O_3 (t_{Al2O3}=100 nm, t_{air}=0 nm), the current reduces by 29% in c=140 nm devices, and the channel pinches off at smaller gate voltage. Due to the above mentioned effects, it is noticed from Fig. 2(b) that the peak of negative and positive g_m shifts from 3 V to 1 V and the magnitude of g_m gets doubled when the trench is filled with Al_2O_3 as compared to air-trench, confirming the enhanced performance when the high-k dielectric is deposited in the trenches of BDT. Finally, it is also observed from Fig. 2(a) that downscaling BDT from c=200 nm to 140 nm increases the output current per unit length and leads to an earlier pinch off. Fig. 2(b) shows a slight increase in g_m from c=200 nm to c=140 nm. It is thus confirmed that an increase in g_m can be achieved by either depositing high-k dielectrics in the trenches or by downscaling the devices.

The two main leakage sources in the BDT are the gate leakage (I_{LG}) and the top drain leakage (I_{TD}). We saw from the inset of Fig. 2(a) that the deposition of Al_2O_3 in the trenches does not increase the gate leakage significantly. To enhance the performance of BDT, it is imperative that the leakage through the top drain doesn't increase with Al_2O_3 deposition. Therefore, we studied the influence of high-k dielectric on the performance of BDT in terms of I_{TD}. In Fig. 3 we plot the ratio between the output currents and I_{TD} (I_{LD}/I_{TD}) against the top

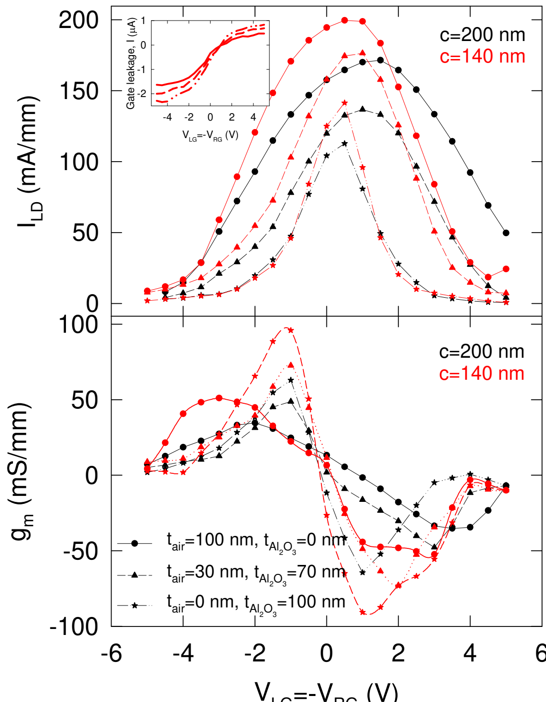

Fig. 2. (a) Transfer characteristics and (b) transconductance of BDT normalized to the channel width c=200 nm and c=140 nm. Deposition of 35 nm and 50 nm of Al_2O_3 along both walls of the trench resulted into 70 nm and 100 nm of net effective Al_2O_3 in the trenches. V_{LD}=V_{RD}=V_{TD}=1 V. Inset in (a) shows the gate leakage current for a BDT with c=140 nm.

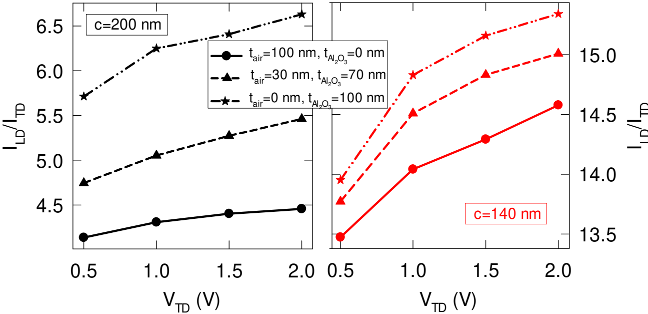

Fig. 3. I_{LD}/I_{TD} ratio vs V_{TD} for BDTs with (a) c=200 nm and (b) c=140 nm for different deposition thickness of Al_2O_3. (V_{LD}=V_{RD}=1 V).

drain voltage (V_{TD}). Since there is no high-k – III-V interface at the top drain boundary and the gates are still controlling the channel conduction through Al_2O_3 filled trenches, the distribution of the electric field leads electrons to steer more towards the drain terminals. Thus the Al_2O_3 filled trenches resulted into higher I_{LD} and reduced I_{TD}, leading to improved I_{LD}/I_{TD} ratio by about 6% in c=140 nm and about 30% in c=200 nm at a V_{TD}=V_{LD}=V_{RD}=1 V. It is also observed that the I_{LD}/I_{TD} ratio in c=140 nm devices is 2.5× bigger than in c=200 nm for V_{TD}=V_{LD}=V_{RD}=1 V and for Al_2O_3 filled trenches, which is attributed to an improved steering of electrons towards the side output drains. Also, an increase in V_{TD} increases the I_{LD}/I_{TD} ratio, which shows the functionality of top drain and deflector. Increase in V_{TD} attracts more electrons towards itself, but deflector in the middle pushes these electrons more efficiently towards the output side drains.

V. Conclusion

We have fabricated BDTs and successfully integrated a high-k dielectric, Al_2O_3, with III-V semiconductors. This is the first successful deposition of Al_2O_3 into the trenches of any ballistic devices to enhance its performance, to the best of our knowledge. It is confirmed that g_m can be increased (×2) by depositing high-k dielectric in the trenches and by downscaling the devices. It is also observed that the improvement in the I_{LD}/I_{TD} ratio could be up to 30% with high-k dielectric. Smaller devices showed a 2.5x improvement in the I_{LD}/I_{TD} ratio.

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