EFFECTS OF BANDPASS SIGMA-DELTA MODULATION ON OFDM SIGNALS

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Abstract - This paper presents a behavioural analysis of bandpass OFDM signals sampled and quantized by means of a sigma-delta A/D architecture. It describes the direct effects of sigma-delta modulation on OFDM signals with a variable number of subcarriers by measuring bit-error-rate degradations. Due to the gaussian characteristic of OFDM signals, the study has been approached from a statistical point of view.

1. INTRODUCTION

Currently, several efforts can be identified in the signal-processing field. On the one hand, RF engineers try to approach the baseband domain by designing cells that integrate as many functions as a front-end must assume such as downconversion, amplification and filtering. On the other hand electrical engineers intend to increase the speed of their baseband integrated circuits, especially that of ADCs (analogue-to digital converters), DACs (digital-to-.analogue converters), DSPs (digital signal processors) or FPGAs (Field Programmable Gate Arrays).

As a result, a new way of thinking and designing is emerging, where the analogue and digital domains mix up to give rise to the mixed-signal technology. The main consequence of these trends is the development of the digitally programmable wireless terminals. The way to achieve this target is designing efficient ADC converters capable of digitising IF (Intermediate Frequency) signals with sufficient linearity and accuracy in time and amplitude. Among the A/D techniques, we find that sigma-delta (Σ–Δ) is interesting for this purpose, since it allows digitising weak IF signals with relatively low cost, low consumption and very high precision [1].

In a parallel way, system engineers intend to integrate not only technologically but also operatively, several services on a unique signal. Thus, multicarrier modulations such as OFDM (Orthogonal Frequency Division Multiplex) are being intensively studied not only for their characteristic immunity to propagation effects and their spectral efficiency, but also for their advantageous use in multimedia applications [2].

This paper presents a contribution to the study of OFDM signals. In particular, we analyse the behaviour of an OFDM signal subject to the non-linearity of an ADC converter based on a sigma-delta architecture. Previous general studies can be founded related to this topic [3], but the analysis considering a bandpass OFDM input has not yet been done.

The remainder of this paper is organised as follows: after reviewing some properties of OFDM signals and sigma-delta modulation, the design of a bandpass sigma-delta converter is presented and optimised in terms of stability, minimum quantization error and minimum SNR degradation. Finally, we illustrate some advantages of sigma-delta structures in comparison with conventional flash ADCs and how their performance can be improved by increasing the order of modulation.

2. ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (OFDM)

OFDM (Orthogonal Frequency Division Multiplexing) is a multicarrier modulation that is finding many recent applications due to its ability to combat impulsive noise and multipath effects and make fuller use of the system available bandwidth. It has been adopted for the European Digital Audio Broadcasting (DAB) [4] and Digital Video Terrestrial Broadcasting (DVB) [5] standards, it has been proposed for UMTS (Universal Mobile Telecommunication Systems) [6] and it is under study for new wireless LAN generations (HIPERLAN: High Performance Radio LAN) [7].

OFDM allows the integration of multiple services on a constant bandwidth making use of

Fast Fourier Transforms (inverse and direct FFT in the transmitter and receiver respectively). A serial bit stream is distributed in parallel over different subcarriers by means of some digital modulation (typically QPSK, N-QAM). The number of subcarriers can be selected depending on the system requirements and scenario, although, in practice, due to the FFT implementation, a power of 2 is chosen.

Among the properties of an OFDM signal, we may point out the great dynamic range of its amplitude, making it very sensitive to non-linearities [8] such as those present in an RF amplifier or in an ADC converter. Furthermore, according to the central limit theorem, we may approximate the OFDM probability density function to a gaussian pdf [8].

In the following, we will take profit of this property in order to simplify the study of the effects of sigma-delta ADC conversion in OFDM signals.

3. Σ–Δ MODULATION

Sigma-Delta is an oversampling A/D technique, which allows digitising signals with very low resolution in amplitude (1 bit) and high resolution in time. The main result is a robust architecture (figure 1) with a very low degradation of the input signal-to-noise ratio (SNR). The analogue input is compared with an analogue version of the last quantized sample, and the error is integrated in an accumulator. The signal is then digitised following the time variations from the input. If the system is designed to work at rates greatly above the signal bandwidth, low input time variations can be expected and then high accuracy is obtained in the quantization error.

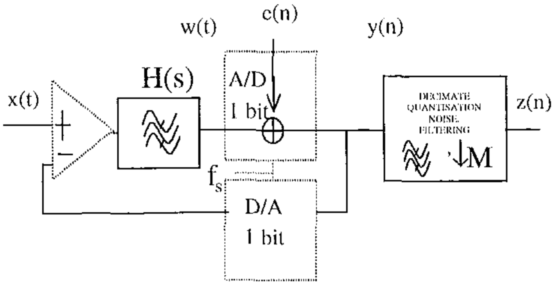


Figure 1. A Σ–Δ single stage architecture

Linear theory, which separates quantization noise from the original signal, has proved to be a good analysis tool for sigma-delta performance predictions, specially for zero-mean gaussian stochastic inputs [3]. According to the latter, a single stage Σ–Δ structure can be analysed from its equivalent discrete model shown in figure 2.

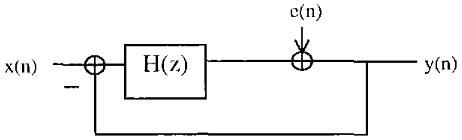


Figure 2. Equivalent model of Σ–Δ

Equations associated to the discrete feedback loop are given below:

$$H(z) = \frac{z^{-1}}{1 - P_0 z^{-1}} \qquad (1)$$

$$Y(z) = \frac{H(z)}{H(z)+1} X(z) + \frac{1}{H(z)+1} E(z) \qquad (2)$$

In an ideal case, the integrator has infinite DC gain (P_0=1) and the output is

$$Y(z) = z^{-1} X(z) + (1 - z^{-1}) E(z) \qquad (3)$$

so that quantization noise is swept off baseband. It can be shown that a Σ–Δ architecture is sensitive to the OSR (oversampling ratio) defined as the sampling frequency related to the signal bandwidth f_s/B. Authors in [9] have shown that for a single stage architecture, the sensitivity of quantization SNR (SNR_q) to OSR is OSR $^{3/2}$, increasing this value in 9 dB (1.5 bits in a uniform quantization law) for every time we double the sampling frequency. The use of oversampling will require implementing a decimation process after the modulator, so as to recover amplitude resolution from time resolution.

4. DESIGN OF A BANDPASS Σ–Δ ARCHITECTURE

The design of a bandpass architecture firstly requires determining the frequency plan for the A/D converter, i.e., the intermediate frequency for which the modulator performance is optimum. To derive a structure for a bandpass signal, we can take advantage of the equivalent discrete model and apply a frequency transformation in the z-domain. A relationship between the sampling frequency and the carrier centre frequency can be obtained. It can be anticipated that it is very important to situate the quantization noise null resulting from noise shaping in the central intermediate frequency of the signal. A frequency baseband-bandpass translation has to be designed [10, pp. 430-438]. It can be shown that the most suitable frequency plan in terms of linearity and spectrum symmetry is that using an IF/f_s ratio equal to 4 corresponding to a discrete frequency of $\pi/2$ rad.

Figure 3 shows how when moving away from $\pi/2$ rad, spectral asymmetries become more significative and the quantization noise filter phase is not linear any more.

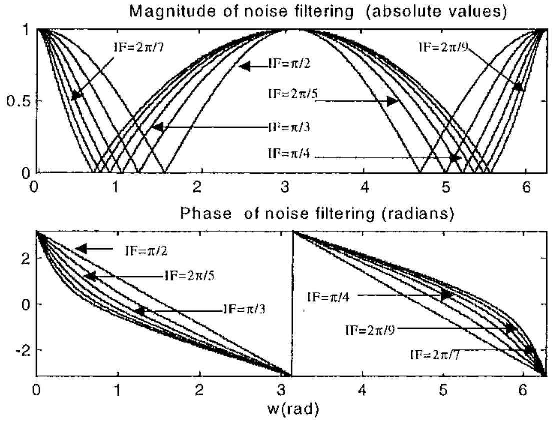


Figure 3. Frequency characterisation of noise filtering for different frequency plans

The equations resulting from substituting z^{-1} by $-Z^{-2}$ are the following [10]:

$$z^{-1} = -Z^{-2} \Leftrightarrow \mathrm{IF}\,(Hz) = f_s\,(Hz)/4 \qquad (4)$$

$$H(z) = \frac{-z^{-2}}{1+P_0 z^{-2}} \qquad (5)$$

$$H_{\Sigma\text{-}\Delta}(z) = -z^{-2}X(z)+(1+z^{-1})^2E(z) \qquad (6)$$

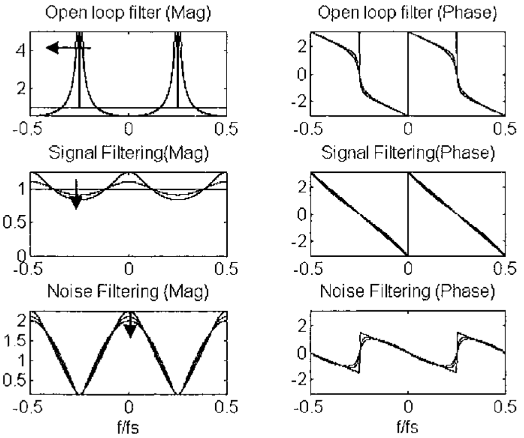


Figure 4. Spectral characterisation of the filtering implied in the modulator

With the design described above, we keep most of the simplicity of the architecture and we avoid compensating non-linear phase effects (given by H(z)/(H(z)+1)) from the feedback loop response on the input to be digitised. For the latter frequency translation, the input signal is just delayed and only distorted by additive frequency-shaped quantization noise. The overall response for both components, signal and quantized noise, is shown in figure 4.In the figure above, the arrow indicates how the filtering is modified by increased the IF losses in the bandpass feedforward filter (P_o).

5. STABILITY ANALYSIS OF THE BANDPASS CONVERTER

The stability analysis [11] is very important in order to prevent the modulator from oscillating. We may use the discrete equivalent model in order to fix critical values within the converter. Without loss of generality, we may consider the quantizer as a variable gain G amplifier and as a result the transfer function of the $\pi/2$ modulator is:

$$Y(z) = \frac{H(z)}{H(z)+1}X(z)$$

$$\text{with } H(z) = \frac{-Gz^{-2}}{1+z^{-2}} \; (P_o = 1, \text{ideal case})$$

The oscillation condition is given by:

$$H(z) = -1 \Rightarrow z^{-2} = G-1$$

The circuit remains stable if $|z| \leq 1$. We may distinguish two limit cases for $|z|=1$:

$$G=2 \Rightarrow w_{osc}=0 \text{ or } \pi \text{ rad} \Rightarrow f=0 \text{ or } f_s$$

$$G=0 \Rightarrow w_{osc}= \pm\pi/2 \text{ rad} \Rightarrow f= \pm f_s/2 \; (z=e^{jw})$$

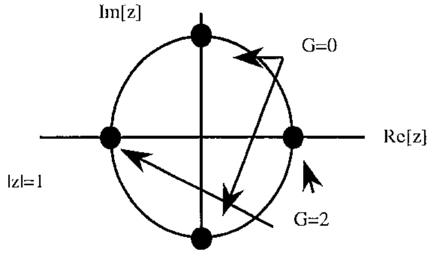


Figure 5. Pole-Zero Analysis

This is illustrated in figures 5 and 6. The first plot in figure 6 corresponds to a case where the quantizer level is too small in comparison with the signal dynamic range (G>2) whereas in the last plot the quantizer level is too large to follow the signal variations (G<0). The central plot represents a stable situation (0<G<2). In the latter the bandpass signal can be distinguished from the quantization noise, swept out of band.

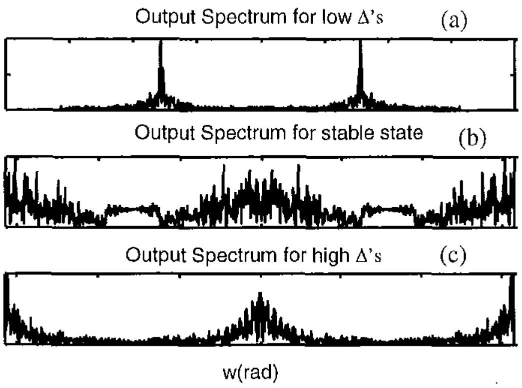


Figure 6. Spectral Analysis for stable (b) and unstable states (a,c)

6. OPTIMISATION OF THE BANDPASS CONVERTER

In order to obtain an optimum performance of the sigma-delta modulator, we may characterise how the OFDM input signal induces changes inside the architecture and we may select parameters such as the optimum output level and bounds based upon stability conditions for the feedback loop.

It has been shown in [3] that for a zero-mean gaussian input signal and a stable state of the feedback loop, the distribution of signals w(n) and y(n) (see figure 1) can be approximated by gaussian and binomial pdfs respectively under the condition that the input power is high enough (approaching instability) or in case the input signal to the converter is white. For a stable situation, the pdfs associated to all signals have been illustrated in figure 7 when an input OFDM signal is applied.

Due to the difficulty to give analytical results referring to cross-correlations and autocorrelations of the processes in the sigma-delta conversion, the modulator has been numerically optimised (simulations) in terms of the optimum input power level for a quantizer step already fixed. The main difficulty in obtaining analytical results concerns the assumptions on the 1 bit quantizer pdf, the dependency of its variance with the quantizer step (feedback system) shown in figure 8 and the non-linearity of the conversion process, linearised here with equations 2-3.

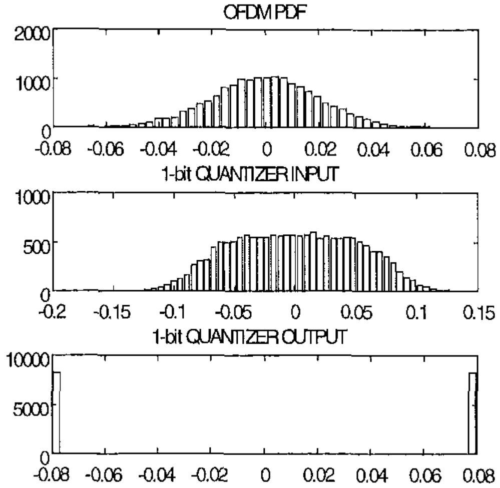


Figure 7.PDFs of signals involved in the Σ–Δ process

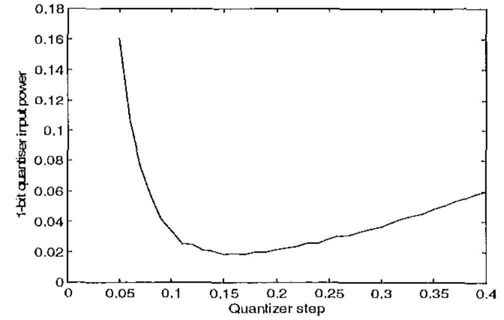


Figure 8. Dependency of the 1-bit quantizer input variance with the quantizer step (constant OFDM signal power equal to 0.082)

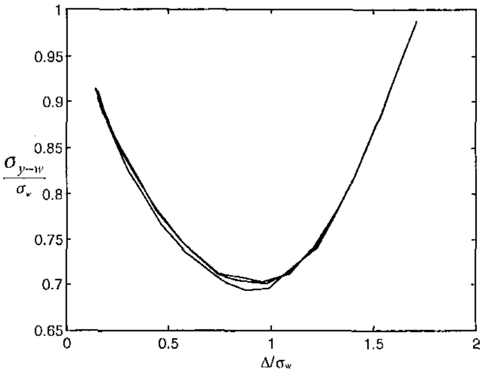


Figure 9. Determination of the optimum performance of the 1-bit quantizer (128, 2048 and 8192 subcarriers)

Figures 9 and 10 show the simulation results concerning the optimum quantiser step level that reduces the quantization error power. We may outline that an optimum value for A/σ_w is approximately 0.9 whereas an optimum A/σ_x relationship is 1.7, both giving minimum quantization error power. An analytical value for the latter relationships is obtained in [3] assuming a gaussian distribution for w(n) process.

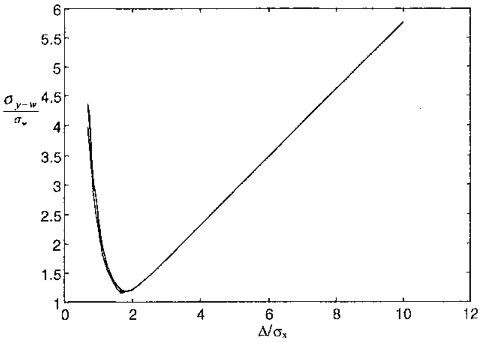


Figure 10. Determination of the optimum performance of the whole Σ–Δ converter (128, 2048 and 8192 subcarriers)

7. OPTIMISATION OF THE BANDPASS CONVERTER UNDER AWGN CHANNEL

The latter analysis has been illustrated with signals not affected by channel noise. Having suffered the effects of an AWGN channel, the statistics remain since a sum of gaussian processes is also a gaussian process. The input power, represented by the input variance σ_x^2 may change but the optimisation results will be the same (figure 11).

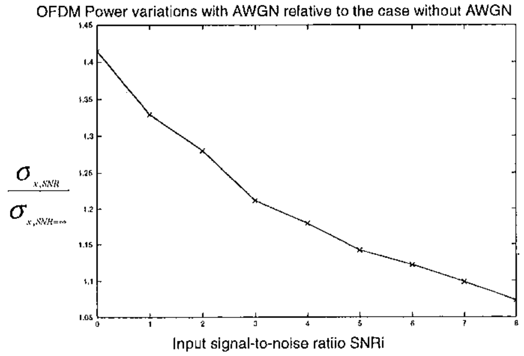


Figure 11. OFDM statistics affected by AWGN channel

When corrupted by white gaussian noise, we may be interested in the Bit Error Rate degradation introduced in the digitisation process. A simulation model has been built (figure 12) in order to estimate the SNR losses induced by the use of Σ–Δ modulation.

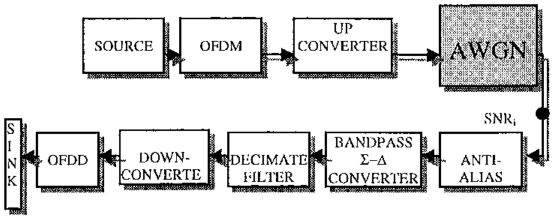


Figure 12. Simulation model for a AWGN channel

A serial bit stream contains the symbol information of a set of orthogonal subcarriers, each modulated in QPSK and the whole is up-converted to an intermediate frequency. The bandpass generated signal is then passed through an AWGN channel, band-pass filtered and digitised in a Σ–Δ architecture. The signal is then filtered to eliminate quantisation noise, decimated and demultiplexed. For each OFDM symbol, an analysis of BER is done via Montecarlo simulations. Some results are presented in figures 13 and 14.

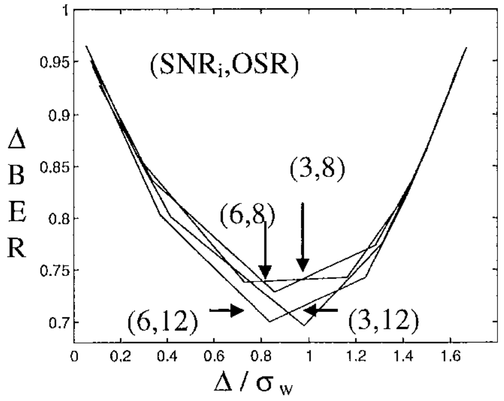
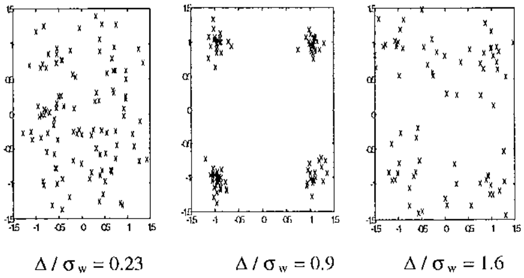


Figure 13. BER performance of the system in figure 12



$\Delta/\sigma_w = 0.23$ $\Delta/\sigma_w = 0.9$ $\Delta/\sigma_w = 1.6$

Figure 14. Constellation analysis of the system in figure 12

Optimisation of the converter proves to be determinant in order to reduce distorsion in the QPSK constellation which is used for each subcarrier. For an optimum relationship Δ/σ_x, quantisation noise power is minimum and this translates into a reduction of the symbol state dispersion in the scattering diagram. For values distant from the latter, not only the risk of instability increases but also the in-band quantisation power as well. Note that the subcarriers which are situated far from the intermediate frequency will always be more damaged and their contribution to the OFDM symbol degradation will be higher.

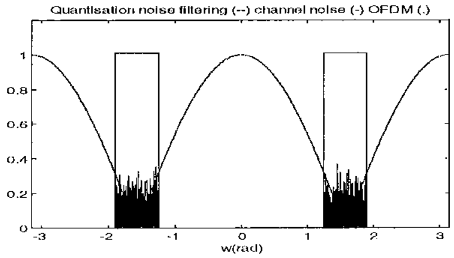


Figure 15. Effects of Σ–Δ spectral conformation in BER

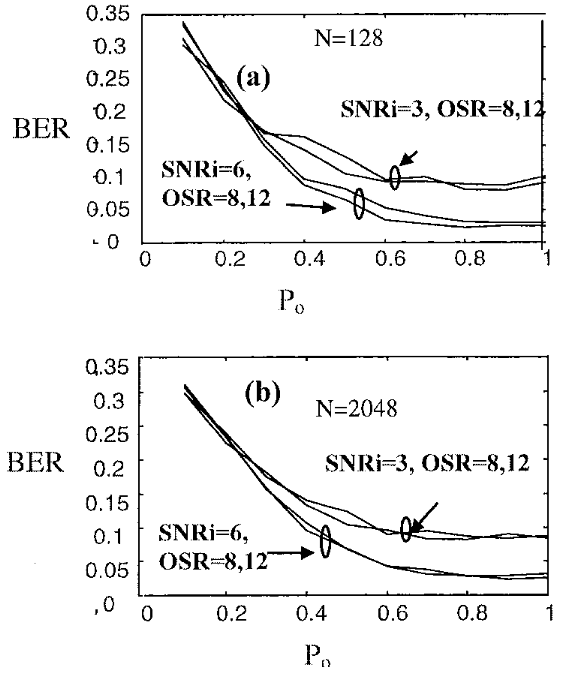
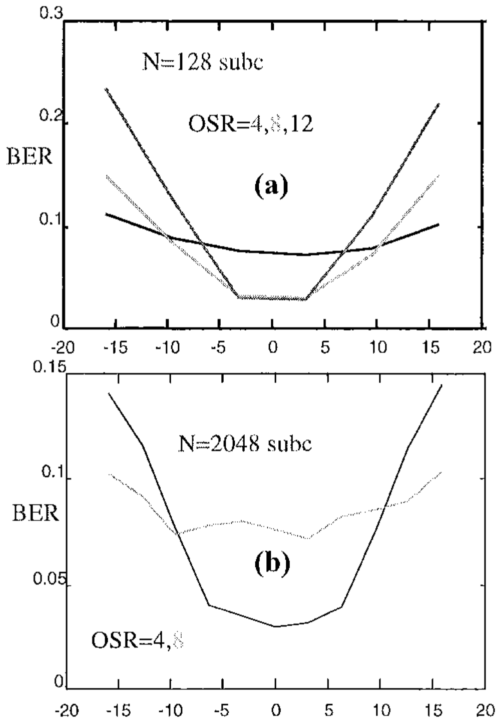


Figure 16. Influence of P_0 in the BER of system in figure 12 (N=128 subcarriers (a) and N=2048 subcarriers (b))

Until now, we have assumed ideal characteristics for the bandpass filter. In practice [9,12,13], the filter may suffer from spectral imperfections. For instance, the IF gain cannot be infinite and will be bounded, resulting in a degradation of the Σ–Δ performance. Special interest has been taken in determining how far the BER could be affected by this phenomenon and simulation results shown in figure 16 reveal that forcing P_0 to keep within the range $P_0 \geq 0.6$ does not introduce excessive degradation in the input SNR.

Another point of interest is synchronisation. Earlier in this section, we have mentioned how the subcarrier spectral allocation could increase the impact of quantisation noise. If the sampling frequency suffers from constant jitter with a relationship IF/f_s different from 4, this will shift this dependence and worsen in any case the SNR degradation due to the spectral asymmetries. This is equivalent to consider that the bandpass filter is not centred at IF [12]. Furthermore, the higher the number of subcarriers in the OFDM spectrum, the more the latter sensitivity is sharpened (figure 17).



$$\Delta\ IF(\%) = 100 * \frac{IF\ (rad) - \frac{\pi}{2}}{\frac{\pi}{2}}$$

Figure 17. BER degradation under frequency-shifted bandpass signals. (N=128 subcarriers (a) and N=2048 subcarriers (b))

Random jitter, also known as time uncertainty, also proves to be very damaging despite the hard-quantisation noise which may absorb the effects of some timing inaccuracies. An IF signal sampled with clock jitter will suffer from phase and additive noise. Furthermore, for an OFDM signal, phase noise will introduce intercarrier interference (ICI) [2]. A bandpass

$\Sigma-\Delta$ architecture is increasingly vulnerable to clock jitter by raising the OSR since the frequency plan is related to the sampling frequency. Thus, the higher OSR, the higher IF and the higher sampling frequency, increasing the probability of a higher clock jitter. Figure 18 illustrates the direct impact of clock jitter in the BER performance of the system shown in figure 12.

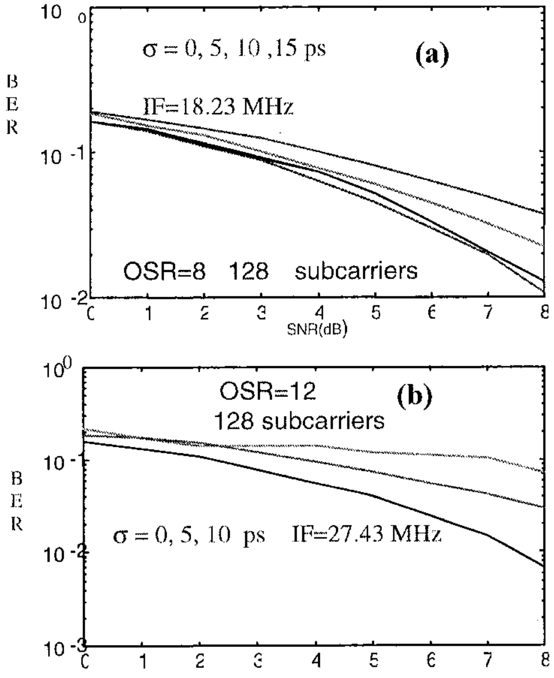


Figure 18. $\Sigma-\Delta$ Performance under the effects of clock jitter (additive jitter with N(0,σ) pdf) with two different oversampling ratios: OSR=8 (a) and OSR=12 (b)

8. COMPARISON WITH A UNIFORM QUANTIZATION LAW

Alternative fast architectures such as flash A/D converters can also be used instead of $\Sigma-\Delta$ modulators but the dynamic range (measured in mV) may be critical to obtain enough resolution [11,14].

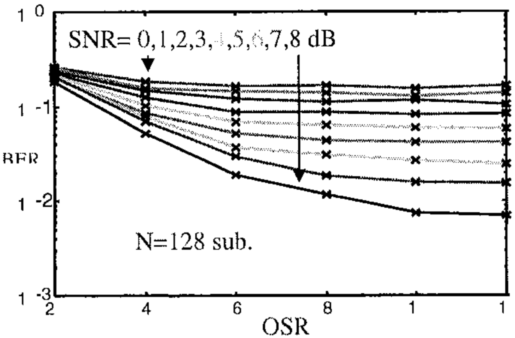


Figure 19. Sensitivity to OSR for a 1-bit $\Sigma-\Delta$

We have compared both structures in terms of sensitivity to oversampling ratio and the BER performance (figures 19 and 20).

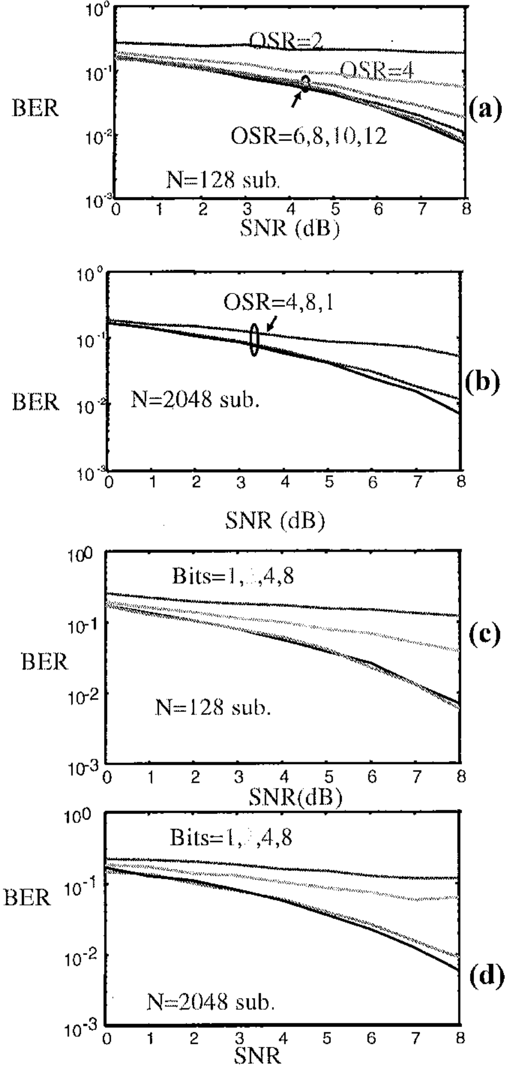


Figure 20. BER degradation with n-bits uniform quantization law (c and d) and 1-bit $\Sigma-\Delta$. (a and b) for both N=128 and N=2048 subcarriers

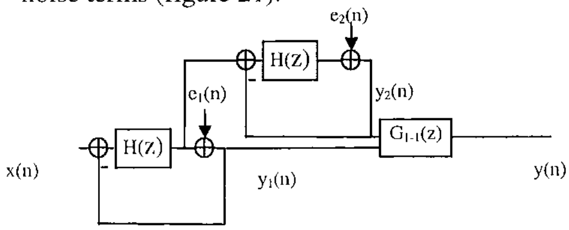
Figure 19 plots the sensitivity of a $\Sigma-\Delta$ converter to oversampling ratio. In terms of BER, the performance does not improve much for OSR above 10 for a 0-8 dB SNR_i range. With reference to a multi-bit flash converter, simulations reveal that there is not much improvement with OSR above 4 (and 1 bit quantisation law). The latter result is interesting from a spectral point of view. Indeed, the 1 bit quantisation error bandwidth is not much wider than 4 times the one from the signal to be quantised.

Figure 20 shows that sigma-delta introduces a higher sensitivity to OSR than conventional n bits A/D architecture. For a single-stage modulator, doubling f_s is equivalent to adding 1.5 bits and this can be verified by means of simulation results. Whereas it is convenient to use an 8-bit quantization law in a flash A/D, a lower bound for the OSR of a Σ–Δ structure could be 10 (aprox. 1.5*10/2=7.5 bits). On the other hand, as mentioned earlier, it can be verified in this figure that no improvement can be obtained in a 1-bit flash A/D by raising OSR above 4, giving us information about the bounded quantisation noise bandwidth of a hard quantisation law.

9. HIGHER ORDER Σ–Δ ARCHITECTURES

Until now, we have considered a single-stage structure with just one bandpass filter and one feedback loop. However, when dealing with wideband systems, accurate oversampling is a price sometimes too high to pay and, in that case, increasing the complexity of the ADC in order to improve sensitivity to OSR is advised.

There are several ways to approach this increase of complexity [9]. We may nest single-stage modulators, by taking the input 1-bit quantiser as the input to the next stage; then all single-stages' outputs are combined to cancel noise terms (figure 21).



$G^{\text{baseband}}_{1-1}(z)=z^{-2}\,Y_1(z) + (1-z^{-1})Y_2(z)$

Figure 21. Example of a 2nd order Σ–Δ obtained by combining two single-stages (equivalent model)

We may also include several feedback loops within the converter including several bandpass filters that may increase the order of quantisation noise filtering (figure 22).

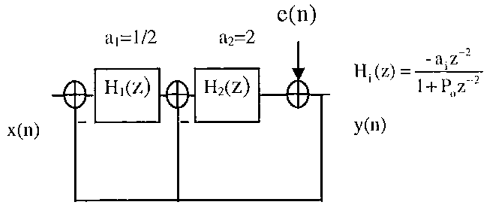


Figure 22. Example of a 2nd order Σ–Δ with two feedback loops (equivalent model)

The main drawback in increasing the Σ–Δ order, besides the implementation complexity, is the increased risk of instability. For a single stage it was recommended to work within the range 0 ≤ G ≤ 2. For a 2nd order, it can be shown that the stable range is 0 ≤ G ≤ 1.333 and for a third order converter 0 ≤ G ≤ 1.16 (see section 5).

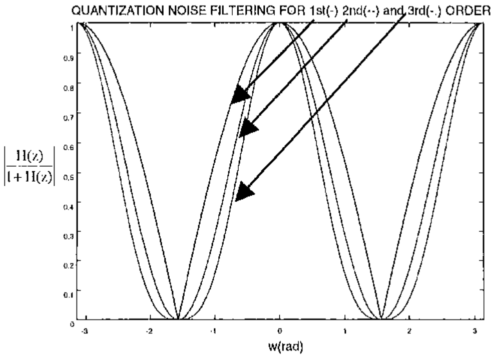


Figure 23. Quantisation noise filtering for different order structures

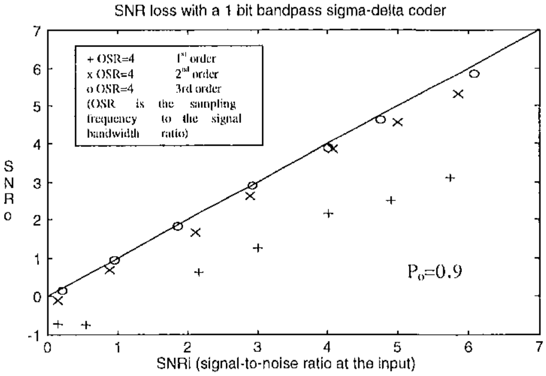


Figure 24. SNR losses introduced by different Σ–Δ architectures

Among the multiple advantages that result from increasing the Σ–Δ order, we may mention a higher sensitivity to the oversampling ratio (in figure 23 we appreciate how the quantisation noise filtering bandwidth is broadened by increasing the modulator order). This will result not only in relaxing the speed conversion, but also in higher synchronisation immunity (constant and random jitter).

Figure 23 shows how a higher sigma-delta order introduces wider quantisation filtering, resulting in a lower SNR degradation.

Figure 24 shows how the requirements on the OSR can be relaxed by increasing the converter order (on detriment of a higher risk of instability). Thus, an oversampling ratio equal to 4 in a third order structure gives a similar performance as a first order structure with OSR=12.

10. CONCLUSIONS

This article has exhaustively described the behaviour of OFDM signals within a bandpass Σ–Δ converter, that has been previously designed and optimised. Due to the gaussian properties, it has been possible to deduce an analytical approach besides simulation results.

It has been shown how a single-stage bandpass structure is critical from a synchronisation point of view as well as oversampling requirements. Use of higher order Σ–Δ architectures is advised not only to relax the latter considerations but also to improve the quantisation noise filtering and the risk of ICI.

Futrure work will be devoted to the theoretical justification of simulation results and to implementation aspects.

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